SBAS282D − JUNE 2003 − REVISED MARCH 2004

16-Bit Analog-to-Digital Converter with Input Multiplexer and Onboard Reference

FEATURES

- **COMPLETE DATA ACQUISITION SYSTEM IN THE MSOP-10 AND LEADLESS QFN-STYLE PACKAGES**
- **MEASUREMENTS FROM TWO DIFFERENTIAL CHANNELS OR THREE SINGLE-ENDED CHANNELS**
- **I^2C™INTERFACE—EIGHT ADDRESSES PIN-SELECTABLE**
- **ONBOARD REFERENCE:**
  Accuracy: 2.048V ±0.05%
  Drift: 5ppm/°C
- **ONBOARD PGA**
- **ONBOARD OSCILLATOR**
- **16 BITS, NO MISSING CODES**
- **INL: 0.01% of FSR max**
- **CONTINUOUS SELF-CALIBRATION**
- **SINGLE-CYCLE CONVERSION**
- **PROGRAMMABLE DATA RATE: 15SPS to 240SPS**
- **POWER SUPPLY: 2.7V to 5.5V**
- **LOW CURRENT CONSUMPTION: 240μA**

APPLICATIONS

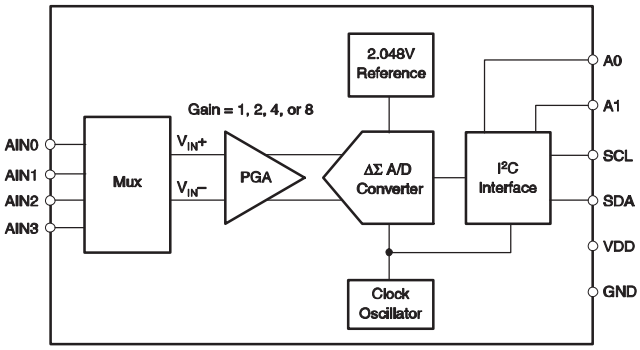
- **PORTABLE INSTRUMENTATION**
- **INDUSTRIAL PROCESS CONTROL**
- **SMART TRANSMITTERS**
- **CONSUMER GOODS**
- **FACTORY AUTOMATION**
- **TEMPERATURE MEASUREMENT**

DESCRIPTION

The ADS1112 is a precision, continuously self-calibrating Analog-to-Digital (A/D) converter with two differential or three single-ended channels and up to 16 bits of resolution in the small MSOP-10 and leadless QFN-style (small-outline, no-lead) packages. The onboard 2.048V reference provides an input range of ±2.048V differentially. The ADS1112 uses an I^2C-compatible serial interface and has two address pins that allow a user to select one of the eight I^2C Slave addresses. The ADS1112 operates from a single power supply ranging from 2.7V to 5.5V.

The ADS1112 can perform conversions at rates of 15, 30, 60, or 240 samples per second (SPS). The onboard programmable gain amplifier (PGA), which offers gains of up to eight, allows smaller signals to be measured with high resolution. In single-conversion mode, the ADS1112 automatically powers down after a conversion, greatly reducing current consumption during idle periods.

The ADS1112 is designed for applications requiring high-resolution measurement, where space and power consumption are major considerations. Typical applications include portable instrumentation, industrial process control, and smart transmitters.



ABSOLUTE MAXIMUM RATINGS(1)

VDD to GND	−0.3V to +6V
Input Current	100mA, Momentary
Input Current	10mA, Continuous
Analog Inputs, A0, A1, Voltage to GND	−0.3V to VDD + 0.3V
SDA, SCL Voltage to GND	−0.5V to 6V
Maximum Junction Temperature	+150°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

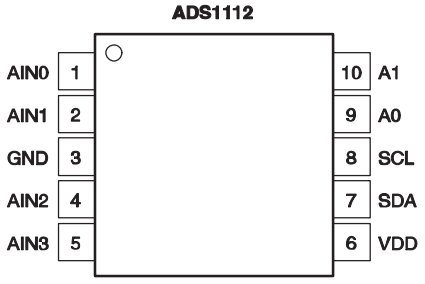
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

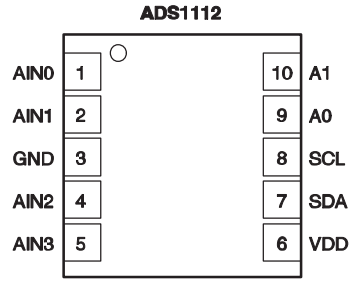
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1112	MSOP-10	DGS	−40°C to +85°C	BHU	ADS1112IDGST	Tape and Reel, 250
					ADS1112IDGSR	Tape and Reel, 2500
ADS1112	SON-10	DRC	−40°C to +85°C	BHV	ADS1112IDRCT	Tape and Reel, 250
					ADS1112IDRCR	Tape and Reel, 3000

(1) For the most current specification and package information, refer to our web site at www.ti.com.

Top View MSOP-10



Top View SON-10



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AIN0	1	Differential Channel 1; Positive Input Single-ended Channel 1 Input
AIN1	2	Differential Channel 1; Negative Input Single-ended Channel 2 Input
GND	3	Ground
AIN2	4	Differential Channel 2; Positive Input Single-ended Channel 3 Input
AIN3	5	Differential Channel 2; Negative Input Single-ended Common Input
VDD	6	Power Supply: 2.7V to 5.5V
SDA	7	Serial Data: Transmits and receives data
SCL	8	Serial Clock Input: Clocks output data on SDA
A0	9	I^2C Slave Address Select
A1	10	I^2C Slave Address Select

ELECTRICAL CHARACTERISTICS

All specifications at −40°C to +85°C, VDD = 5V, and all PGAs, unless otherwise noted.

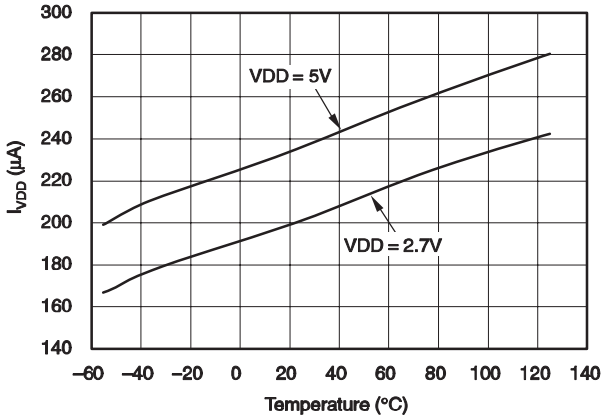
PARAMETER	CONDITIONS	ADS1112 MIN	ADS1112 TYP	ADS1112 MAX	UNIT
ANALOG INPUT					
Full-Scale Input Voltage	$(V_{IN+}) - (V_{IN-})$		±2.048/PGA		V
Analog Input Voltage	V_{IN+} to GND or V_{IN-} to GND	GND − 0.2		VDD + 0.2	V
Differential Input Impedance			2.8/PGA		MΩ
Common-Mode Input Impedance	PGA = 1		3.5		MΩ
	PGA = 2		3.5		MΩ
	PGA = 4		1.8		MΩ
	PGA = 8		0.9		MΩ
SYSTEM PERFORMANCE					
Resolution and No Missing Codes	DR = 00	12		12	Bits
	DR = 01	14		14	Bits
	DR = 10	15		15	Bits
	DR = 11	16		16	Bits
Data Rate	DR = 00	180	240	308	SPS
	DR = 01	45	60	77	SPS
	DR = 10	22	30	39	SPS
	DR = 11	11	15	20	SPS
Output Noise		See Typical Characteristic Curves			
Integral Nonlinearity	DR = 11, PGA = 1, End Point Fit(1)		±0.004	±0.010	% of FSR(2)
Offset Error	PGA = 1		1.2	8	mV
	PGA = 2		0.7	4	mV
	PGA = 4		0.5	2.5	mV
	PGA = 8		0.4	1.5	mV
Offset Drift	PGA = 1		1.2		µV/°C
	PGA = 2		0.6		µV/°C
	PGA = 4		0.3		µV/°C
	PGA = 8		0.3		µV/°C
Offset vs VDD	PGA = 1		800		µV/V
	PGA = 2		400		µV/V
	PGA = 4		200		µV/V
	PGA = 8		150		µV/V
Channel Offset Match	Match between any two channels		30		µV
Gain Error(3)			0.05	0.40	%
PGA Gain Error Match(3)	Match between any two PGA gains		0.02	0.10	%
Gain Error Drift(3)			5	40	ppm/°C
Gain vs VDD			80		ppm/V
Channel Gain Match	Match between any two channels		0.01		%
Common-Mode Rejection	At DC and PGA = 8	95	105		dB
	At DC and PGA = 1		100		dB
DIGITAL INPUT/OUTPUT					
Logic Level					
V_{IH}		0.7 • VDD		6	V
V_{IL}		GND − 0.5		0.3 • VDD	V
V_{OL}	I_{OL} = 3mA	GND		0.4	V
Input Leakage					
I_H	V_{IH} = 5.5V			10	µA
I_L	V_{IL} = GND	−10			µA
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage	VDD	2.7		5.5	V
Supply Current	Power-Down		0.05	2	µA
	Active Mode		240	350	µA
Power Dissipation	VDD = 5.0V		1.2	1.75	mW
	VDD = 3.0V		0.675		mW

(1) 99% of full-scale.
(2) FSR = full-scale range = 2 × 2.048V/PGA = 4.096V/PGA.
(3) Includes all errors from onboard PGA and reference.

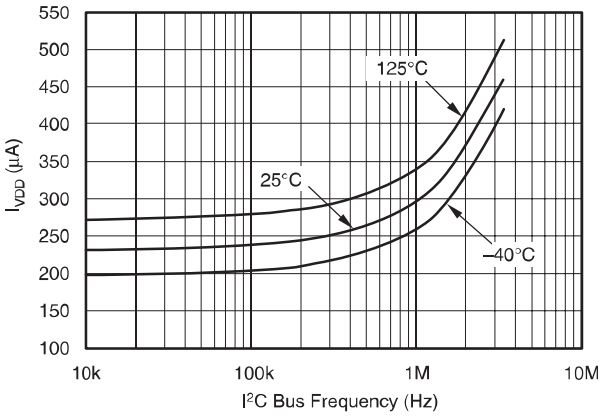
TYPICAL CHARACTERISTICS

At T_A = 25°C and VDD = 5V, unless otherwise noted.

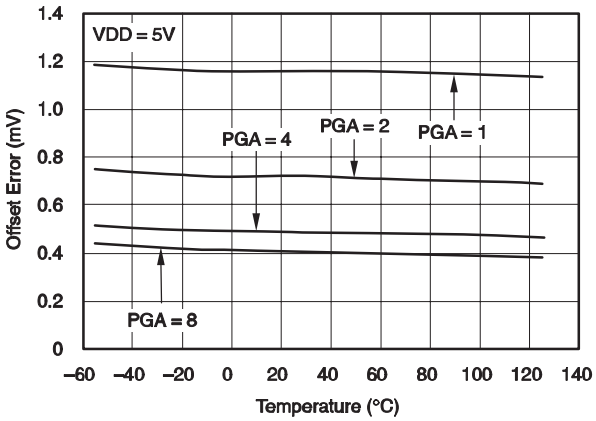
SUPPLY CURRENT vs TEMPERATURE



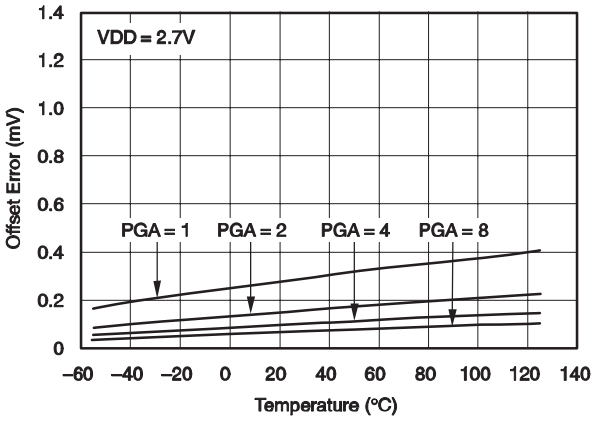
SUPPLY CURRENT vs I²C BUS FREQUENCY



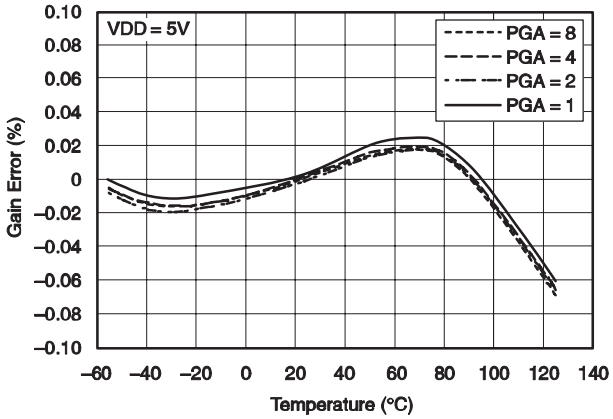
OFFSET ERROR vs TEMPERATURE



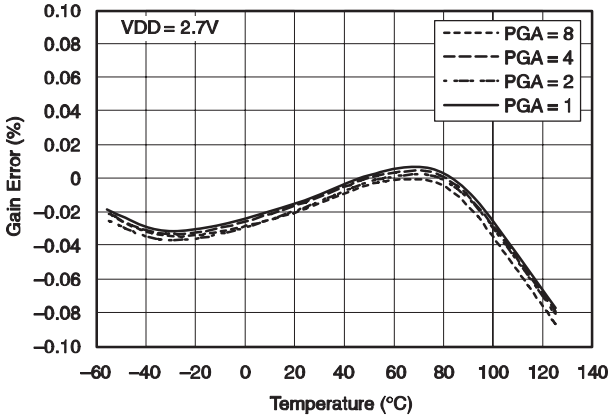
OFFSET ERROR vs TEMPERATURE



GAIN ERROR vs TEMPERATURE



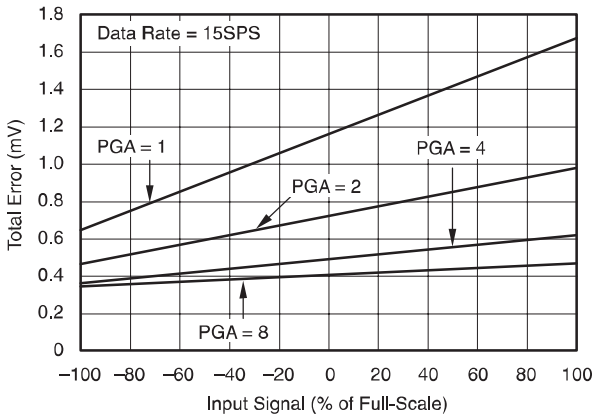
GAIN ERROR vs TEMPERATURE



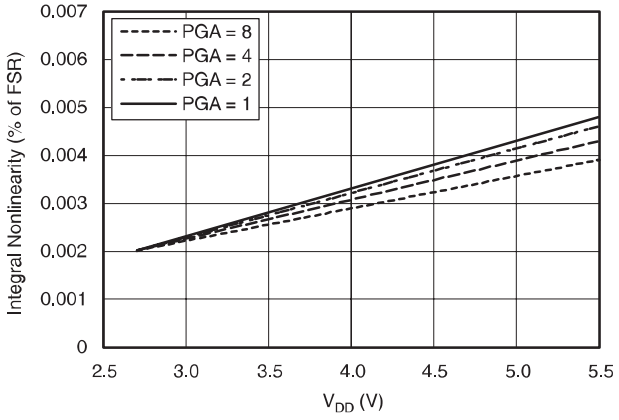
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C and VDD = 5V, unless otherwise noted.

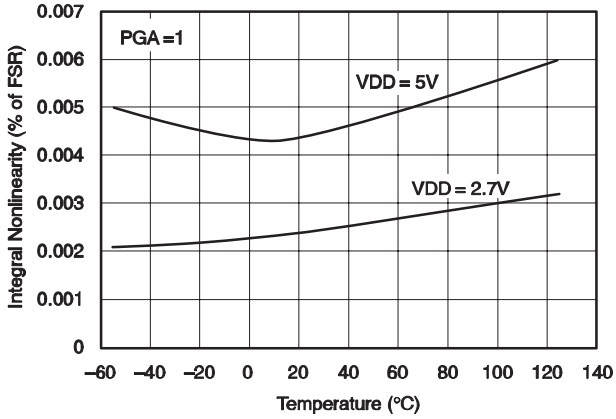
TOTAL ERROR vs INPUT SIGNAL



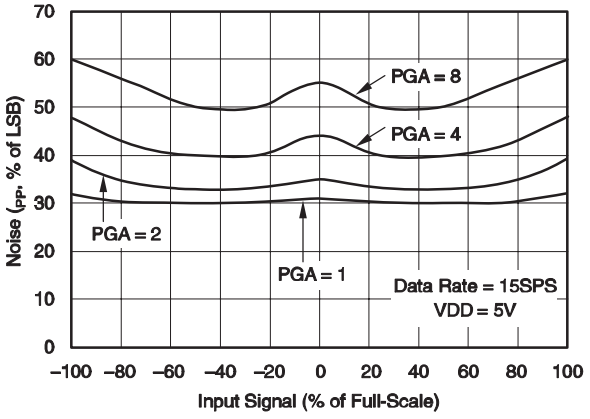
INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE



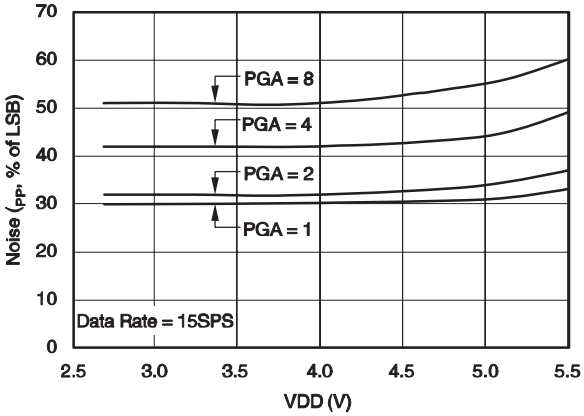
INTEGRAL NONLINEARITY vs TEMPERATURE



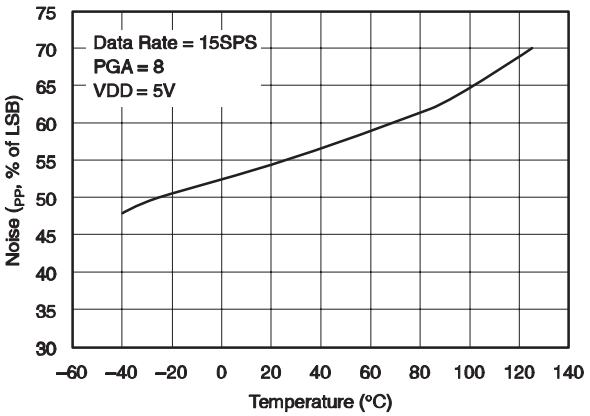
NOISE vs INPUT SIGNAL



NOISE vs SUPPLY VOLTAGE

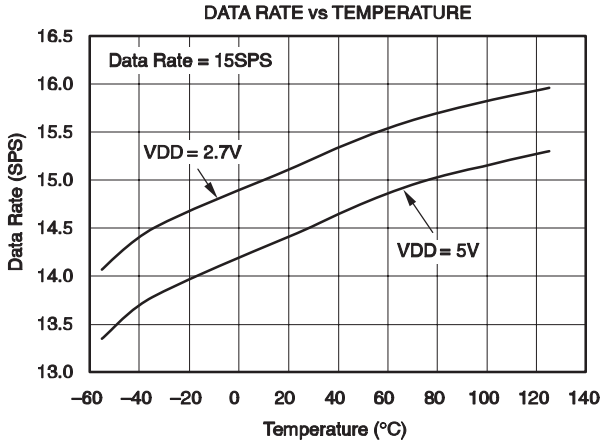


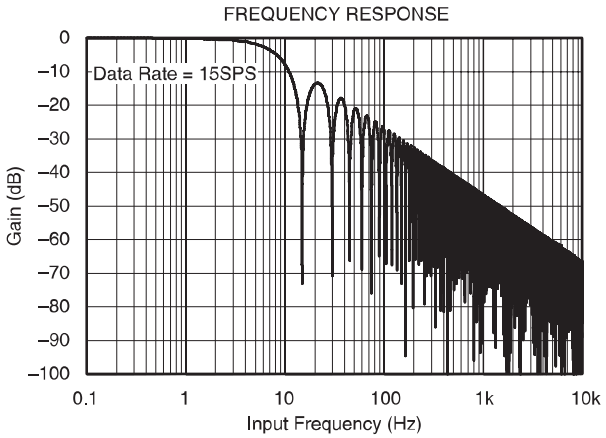
NOISE vs TEMPERATURE



TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C and VDD = 5V, unless otherwise noted.





THEORY OF OPERATION

The ADS1112 is a 16-bit, self-calibrating, delta-sigma A/D converter with an input multiplexer. Extremely easy to design with and configure, the ADS1112 allows precise measurements to be obtained with a minimum of effort.

The ADS1112 consists of a delta-sigma A/D converter core with adjustable gain, a 2.048V reference, a clock oscillator, and an I^2C interface. Each of these blocks are described in detail in the sections that follow.

ANALOG-TO-DIGITAL CONVERTER

The ADS1112 A/D converter core consists of a differential switched-capacitor delta-sigma modulator followed by a digital filter. The modulator measures the voltage difference between the positive and negative analog inputs selected by the input multiplexer and compares it to a reference voltage, which, in the ADS1112, is 2.048V. The digital filter receives a high-speed bitstream from the modulator and outputs a code, which is a number proportional to the input voltage.

MULTIPLEXER

The ADS1112 has an input multiplexer that provides for two differential or three single-ended input channels. Two bits in the configuration register control the multiplexer setting.

VOLTAGE REFERENCE

The ADS1112 contains an onboard 2.048V voltage reference. This reference is always used as the ADC voltage reference; an external reference cannot be connected. The ADS1112 voltage reference is internal only, and cannot be measured directly or used by external circuitry.

The onboard reference specifications are part of the overall gain and drift specifications of the ADS1112. The converter drift and gain error specifications reflect the performance of the onboard reference as well as the performance of the A/D converter core. There are no separate specifications for the onboard reference itself.

OUTPUT CODE CALCULATION

The output code is a scaled value that is proportional, except for clipping, to the voltage difference between the two analog inputs. The output code is confined to a finite range of numbers; this range depends on the number of bits needed to represent the code. The number of bits needed to represent the output code for the ADS1112 depends on the data rate, as shown in Table 1.

DATA RATE	NUMBER OF BITS	MINIMUM CODE	MAXIMUM CODE
15SPS	16	−32,768	32,767
30SPS	15	−16,384	16,383
60SPS	14	−8192	8191
240SPS	12	−2048	2047

Table 1. Minimum and Maximum Codes

For a minimum output code of Min Code, gain setting of the PGA, and positive and negative input voltages of V_{IN+} and V_{IN-}, the output code is given by the expression:

$$\text{Output Code} = -1 \times \text{Min Code} \times \text{PGA} \times \frac{(V_{IN+}) - (V_{IN-})}{2.048V}$$

In the previous expression, it is important to note that the *negated minimum* output code is used. The ADS1112 outputs codes in binary two's complement format, so the

absolute values of the minima and maxima are not the same; the maximum n-bit code is $2^{n-1} - 1$, while the minimum n-bit code is $-1 \times 2^{n-1}$.

For example, the ideal expression for output codes with a data rate of 16SPS and PGA = 2 is:

$$\text{Output Code} = 16384 \times 2 \times \frac{(V_{IN+}) - (V_{IN-})}{2.048V}$$

The ADS1112 outputs all codes right-justified and sign-extended. This feature makes it possible to perform averaging on the higher data rate codes using only a 16-bit accumulator.

Table 2 shows the output codes for various input levels.

SELF-CALIBRATION

The previous expressions for the ADS1112 output code do not account for the gain and offset errors in the modulator. To compensate for these, the ADS1112 incorporates self-calibration circuitry.

The self-calibration system operates continuously and requires no user intervention. No adjustments can be made to the self-calibration system, and none need to be made. The self-calibration system cannot be deactivated.

The offset and gain error figures shown in the Electrical Characteristics include the effects of calibration.

CLOCK OSCILLATOR

The ADS1112 features an onboard clock oscillator, which drives the operation of the modulator and digital filter. The Typical Characteristics show variations in data rate over supply voltage and temperature.

It is not possible to operate the ADS1112 with an external system clock.

INPUT IMPEDANCE

The ADS1112 uses a switched-capacitor input stage. To external circuitry, it looks roughly like a resistance. The resistance value depends on the capacitor values and the rate at which they are switched. The switching frequency is the same as the modulator frequency; the capacitor values depend on the PGA setting. The switching clock is generated by the onboard clock oscillator, so its frequency (nominally 275kHz) is dependent on supply voltage and temperature.

The common-mode and differential input impedances are different. For a gain setting of the PGA, the differential input impedance is typically:

$$2.8M\Omega/PGA$$

The common-mode impedance also depends on the PGA setting. See the Electrical Characteristics for details.

The typical value of the input impedance often cannot be neglected. Unless the input source has a low impedance, the ADS1112 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Bear in mind, however, that active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances will also drift. For many applications, this input impedance drift can be neglected, and the expression given above for typical input impedance can be used.

ALIASING

If frequencies are input to the ADS1112 that exceed half the data rate, aliasing will occur. To prevent aliasing, the input signal must be bandlimited. Some signals are inherently bandlimited. For example, the output of a thermocouple, which has a limited rate of change, may nevertheless contain noise and interference components. These nuisance factors can fold back into the sampling band just as with any other signal.

The ADS1112 digital filter provides some attenuation of high-frequency noise, but the digital filter $Sinc^1$ frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed; in such instances, a simple RC filter will suffice.

When designing an input filter circuit, remember to take into account the interaction between the filter network and the input impedance of the ADS1112.

DATA RATE	DIFFERENTIAL INPUT SIGNAL				
	−2.048V(1)	−1LSB	ZERO	+1LSB	+2.048V
15SPS	8000_H	$FFFF_H$	0000_H	0001_H	$7FFF_H$
30SPS	$C000_H$	$FFFF_H$	0000_H	0001_H	$3FFF_H$
60SPS	$E000_H$	$FFFF_H$	0000_H	0001_H	$1FFF_H$
240SPS	$F800_H$	$FFFF_H$	0000_H	0001_H	$07FF_H$

(1) Differential input only; do not drive the ADS1112 inputs below −200mV.

Table 2. Output Codes for Different Input Signals

USING THE ADS1112

OPERATING MODES

The ADS1112 operates in one of two modes: continuous-conversion or single-conversion.

In continuous-conversion mode, the ADS1112 continuously performs conversions. Once a conversion has been completed, the ADS1112 places the result in the output register and immediately begins another conversion.

In single-conversion mode, the ADS1112 waits until the ST/$\overline{\text{DRDY}}$ bit in the conversion register is set to 1. When this happens, the ADS1112 powers up and performs a single conversion. After the conversion completes, the ADS1112 places the result in the output register, resets the ST/$\overline{\text{DRDY}}$ bit to 0, and powers down. Writing a 1 to ST/$\overline{\text{DRDY}}$ while a conversion is in progress has no effect.

When switched from continuous-conversion mode to single conversion mode, the ADS1112 completes the current conversion, resets the ST/$\overline{\text{DRDY}}$ bit to 0, and powers down.

RESET AND POWER-UP

When the ADS1112 powers up, it automatically performs a reset. As part of the reset process, the ADS1112 sets all of the bits in the configuration register to their default settings.

The ADS1112 responds to the I^{2}C General Call Reset command. When the ADS1112 receives a General Call Reset, it performs an internal reset, exactly as though it had just been powered on.

I^{2}C INTERFACE

The ADS1112 communicates through an I^{2}C (inter-integrated circuit) interface. I^{2}C is a two-wire open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^{2}C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pull-up resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^{2}C bus always takes place between two devices, one acting as the master and the other as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^{2}C devices can act as masters or slaves, but the ADS1112 can only act as a slave device.

An I^{2}C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I^{2}C bus in groups of eight bits. To send a bit on the I^{2}C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero; a HIGH indicates the bit is one). Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

The I^{2}C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. The master always drives the clock line. The ADS1112 never drives SCL, because it cannot act as a master. On the ADS1112, SCL is an input only.

Most of the time the bus is idle; no communication occurs place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start a communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition occurs when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition occurs when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on an I^{2}C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^{2}C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^{2}C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (The master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not-acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

A timing diagram for an ADS1112 I^2C transaction is shown in Figure 1. The parameters for this diagram are given in Table 3.

SERIAL BUS ADDRESS

To program the ADS1112, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The ADS1112 features two address pins, A0 and A1, that set the I^2C address. These pins can be set to a logic low, logic high, or left unconnected (floating), allowing eight addresses to be selected with only two pins as shown in Table 4. The state of pins A0 and A1 is sampled on power-up or after an I^2C general call, and should be set prior to any activity on the interface.

I^2C GENERAL CALL

The ADS1112 responds to the I^2C General Call address (0000000) if the eighth bit is 0. The device will acknowledge the General Call address and respond to commands in the second byte. If the second byte is 00000100 (04h), the ADS1112 will latch the status of the address pins, A0 and A1, but not perform a reset. If the second byte is 00000110 (06h), the ADS1112 will latch the status of the address pins and reset the internal registers.

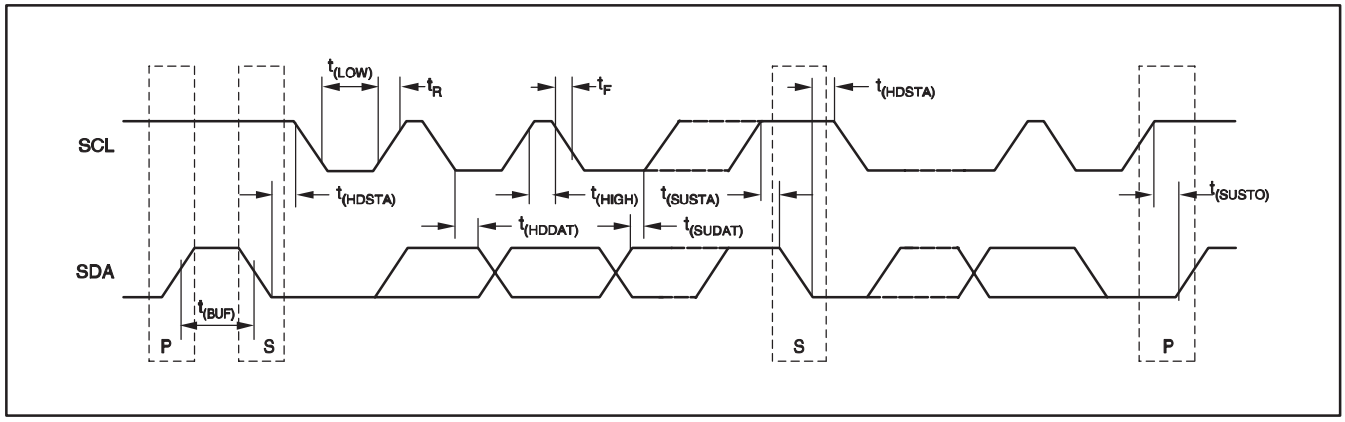


Figure 1. I^2C Timing Diagram

PARAMETER		FAST MODE MIN	FAST MODE MAX	HIGH-SPEED MODE MIN	HIGH-SPEED MODE MAX	UNITS
SCLK operating frequency	$t_{(SCLK)}$		0.4		3.4	MHz
Bus free time between START and STOP condition	$t_{(BUF)}$	600		160		ns
Hold time after repeated START condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	600		160		ns
Repeated START condition setup time	$t_{(SUSTA)}$	600		160		ns
Stop condition setup time	$t_{(SUSTO)}$	600		160		ns
Data hold time	$t_{(HDDAT)}$	0		0		ns
Data setup time	$t_{(SUDAT)}$	100		10		ns
SCLK clock LOW period	$t_{(LOW)}$	1300		160		ns
SCLK clock HIGH period	$t_{(HIGH)}$	600		60		ns
Clock/data fall time	t_F		300		160	ns
Clock/data rise time	t_R		300		160	ns

Table 3. Timing Diagram Definitions

A0	A1	SLAVE ADDRESS
0	0	1001000
0	Float	1001001
0	1	1001010
1	0	1001100
1	Float	1001101
1	1	1001110
Float	0	1001011
Float	1	1001111
Float	Float	Invalid

Table 4. Address Pins and Slave Address for the ADS1112.

I²C DATA RATES

The I²C bus operates in one of three speed modes. Standard mode allows a clock frequency of up to 100kHz; fast mode permits a clock frequency of up to 400kHz; and high-speed mode (also called Hs mode), which allows a clock frequency of up to 3.4MHz. The ADS1112 is fully compatible with all three modes.

No special action needs to be taken to use the ADS1112 in standard or fast modes, but high-speed mode must be activated. To activate high-speed mode, send a special address byte of 00001*xxx* following the START condition, where *xxx* are bits unique to the Hs-capable master. This byte is called the Hs master code. (Note that this is different from normal address bytes; the low bit does not indicate read/write status.) The ADS1112 will not acknowledge this byte; the I²C specification prohibits acknowledgment of the Hs master code. On receiving a master code, the ADS1112 will switch on its Hs mode filters, and communicate at up to 3.4MHz. The ADS1112 will switch out of Hs mode with the next STOP condition.

For more information on high-speed mode, consult the I²C specification.

REGISTERS

The ADS1112 has two registers that are accessible via its I²C port. The output register contains the result of the last conversion; the configuration register allows the user to change the ADS1112 operating mode and query the status of the device.

OUTPUT REGISTER

The 16-bit output register contains the result of the last conversion in binary two's complement format. Following reset or power-up, the output register is cleared to zero, and remains zero until the first conversion is completed.

The output register format is shown in Table 5.

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 5. Output Register

CONFIGURATION REGISTER

The 8-bit configuration register can be used to control the ADS1112 operating mode, input selection, data rate, and PGA settings. The configuration register format is shown in Table 6. The default setting is $8C_H$.

BIT	7	6	5	4	3	2	1	0
NAME	ST/$\overline{\text{DRDY}}$	INP1	INP0	SC	DR1	DR0	PGA1	PGA0
DEFAULT	1	0	0	0	1	1	0	0

Table 6. Configuration Register

Bit 7: ST/$\overline{\text{DRDY}}$

The meaning of the ST/$\overline{\text{DRDY}}$ bit depends on whether it is being written to or read from.

In single conversion mode, writing a 1 to the ST/$\overline{\text{DRDY}}$ bit causes a conversion to start, and writing a 0 has no effect. In continuous conversion mode, the ADS1112 ignores the value written to ST/$\overline{\text{DRDY}}$.

When read, ST/$\overline{\text{DRDY}}$ indicates whether the data in the output register is new data. If ST/$\overline{\text{DRDY}}$ is 0, the data just read from the output register is new, and has not been read before. If ST/$\overline{\text{DRDY}}$ is 1, the data just read from the output register has been read before.

The ADS1112 sets ST/$\overline{\text{DRDY}}$ to 0 when it writes data into the output register. It sets ST/$\overline{\text{DRDY}}$ to 1 after any of the bits in the configuration register have been read. (Note that the read value of the bit is independent of the value written to this bit.)

In continuous-conversion mode, use ST/$\overline{\text{DRDY}}$ to determine when new conversion data is ready. If ST/$\overline{\text{DRDY}}$ is 1, the data in the output register has already been read, and is not new. If it is 0, the data in the output register is new, and has not yet been read.

In single-conversion mode, use ST/$\overline{\text{DRDY}}$ to determine when a conversion has completed. If ST/$\overline{\text{DRDY}}$ is 1, the output register data is old, and the conversion is still in process; if it is 0, the output register data is the result of the new conversion.

Note that the output register is returned from the ADS1112 before the configuration register. The state of the ST/$\overline{\text{DRDY}}$ bit applies to the data just read from the output register, and not to the data from the next read operation.

Bits 6-5: INP

INP controls which two of the four analog inputs are used to measure data in the ADC. This is shown in Table 7. By selecting these bits, the ADS1112 can be used to measure two differential channels or three single ended channels referenced to AIN3.

INP1	INP0	V_{IN+}	V_{IN-}
0(1)	0(1)	AIN0	AIN1
0	1	AIN2	AIN3
1	0	AIN0	AIN3
1	1	AIN1	AIN3

(1) Default setting.

Table 7. INP Bits.

Bit 4: SC

SC controls whether the ADS1112 is in continuous conversion or single conversion mode. When SC is 1, the ADS1112 is in single conversion mode; when SC is 0, it is in continuous conversion mode. The default setting is 0.

Bits 3-2: DR

Bits 3 and 2 control the ADS1112 data rate, as shown in Table 8.

DR1	DR0	DATA RATE	RESOLUTION
0	0	240SPS	12 Bits
0	1	60SPS	14 Bits
1	0	30SPS	15 Bits
1(1)	1(1)	15SPS(1)	16 Bits(1)

(1) Default setting.

Table 8. INP Bits.

Bits 1-0: PGA

Bits 1 and 0 control the ADS1112 gain setting, as shown in Table 9.

PGA1	PGA0	GAIN
0(1)	0(1)	1(1)
0	1	2
1	0	4
1	1	8

(1) Default setting.

Table 9. PGA Bits

READING FROM THE ADS1112

To read the output register and the configuration register from the ADS1112, first address the ADS1112 for reading, then read three bytes. The first two bytes will be the output register's contents, and the third will be the configuration register's contents.

It is not required to read the configuration register byte. It is permissible to read fewer than three bytes during a read operation.

Reading more than three bytes from the ADS1112 has no effect. All bytes following the third will be FF_H.

It is possible to ignore the ST/$\overline{DRDY}$ bit and read data from the ADS1112 output register at any time, without regard to whether a new conversion is complete. If the output register is read more than once during a conversion cycle, it will return the same data each time. New data will be returned only when the output register has been updated.

A timing diagram of a typical ADS1112 read operation is shown in Figure 2.

WRITING TO THE ADS1112

To write to the configuration register, first address the ADS1112 for writing, and send one byte. The byte will be written to the configuration register. Note that data cannot be written to the output register.

Writing more than one byte to the ADS1112 has no effect. The ADS1112 will ignore any bytes sent to it after the first one, and it will only acknowledge the first byte.

A timing diagram of a typical ADS1112 write operation is shown in Figure 3.

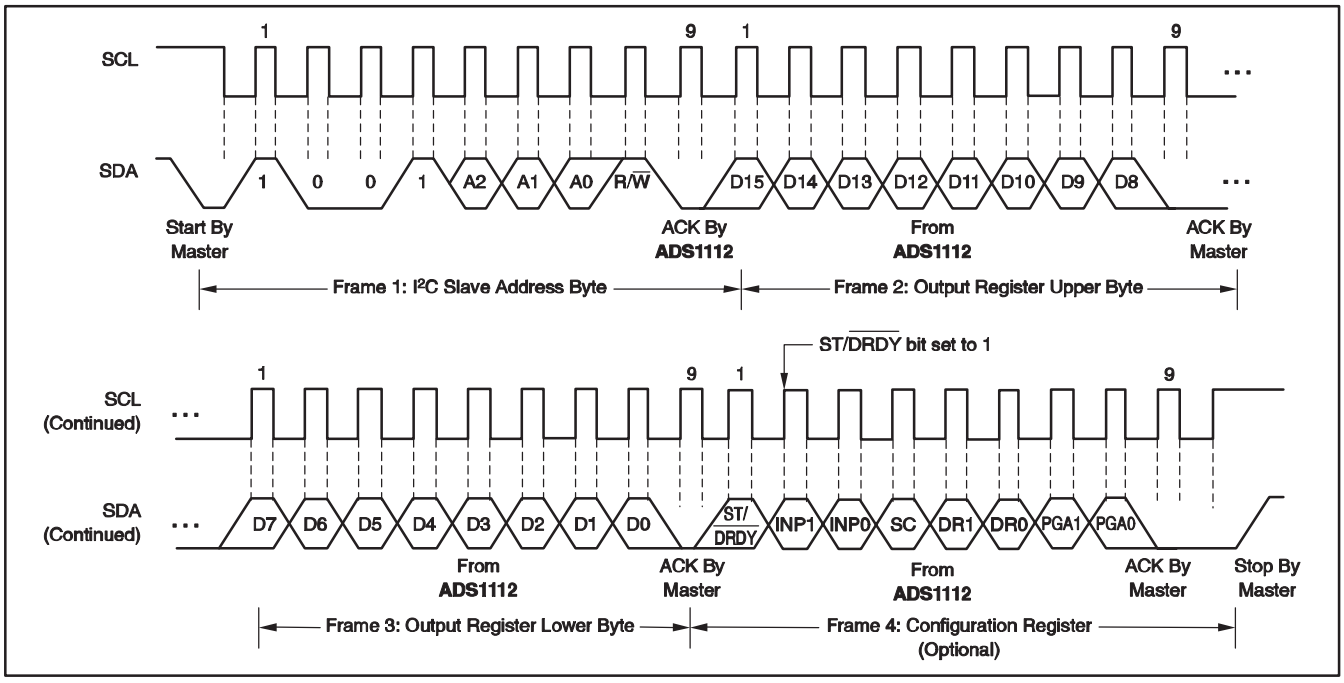


Figure 2. Timing Diagram for Reading From the ADS1112

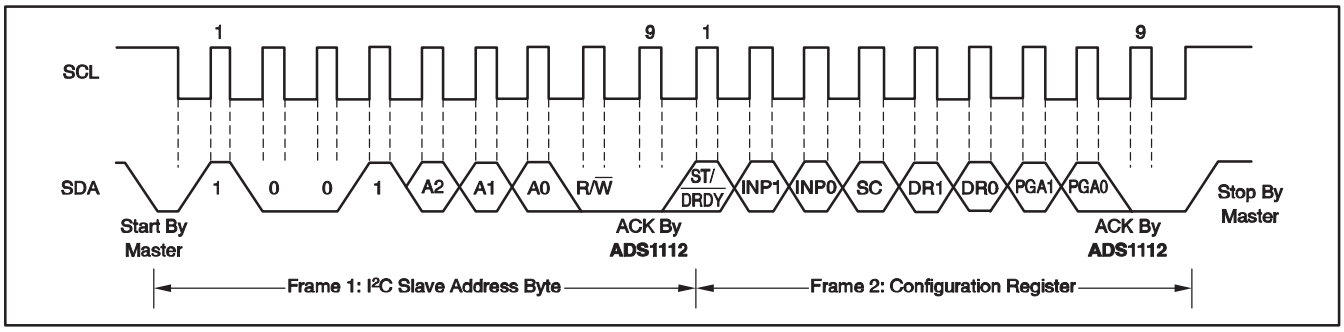


Figure 3. Timing Diagram for Writing To the ADS1112

APPLICATIONS INFORMATION

The sections that follow give example circuits and tips for using the ADS1112 in various situations.

BASIC CONNECTIONS

For many applications, connecting the ADS1112 is extremely simple. A basic connection diagram for the ADS1112 is shown in Figure 4.

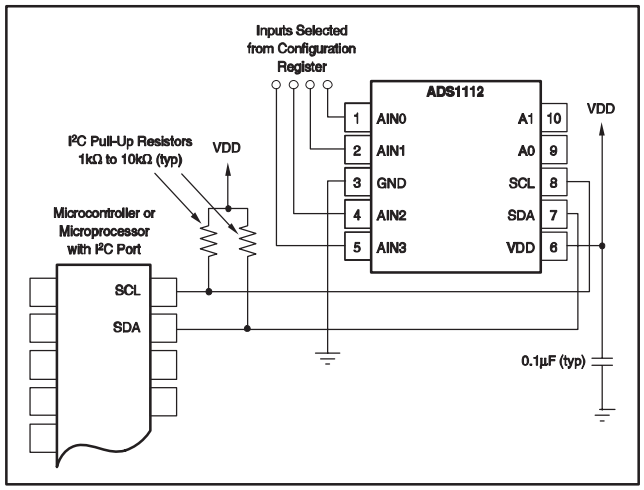


Figure 4. Typical Connections of the ADS1112

The fully differential voltage input of the ADS1112 is ideal for connection to differential sources with moderately low source impedance, such as bridge sensors and thermistors. Although the ADS1112 can read bipolar differential signals, it cannot accept negative voltages on either input. It may be helpful to think of the ADS1112 positive voltage input as non−inverting, and of the negative input as inverting.

When the ADS1112 is converting, it draws current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply.

The ADS1112 interfaces directly to standard mode, fast mode, and high-speed mode I^2C controllers. Any microcontroller's I^2C peripheral, including master-only and non-multiple-master I^2C peripherals, will work with the ADS1112. The ADS1112 does not perform clock-stretching (that is, it never pulls the clock line low), so it is not necessary to provide for this unless clock-stretching devices are on the same I^2C bus.

Pull-up resistors are required on both the SDA and SCL lines because I^2C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pull-up resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

CONNECTING MULTIPLE DEVICES

Connecting multiple ADS1112s to a single bus is trivial. Using pins A1 and A0, the ADS1112 can be set to one of eight different I^2C addresses. An example showing three ADS1112s is given in Figure 5. Up to eight ADS1112s (using different states of pins A1 and A0) can be connected to a single bus.

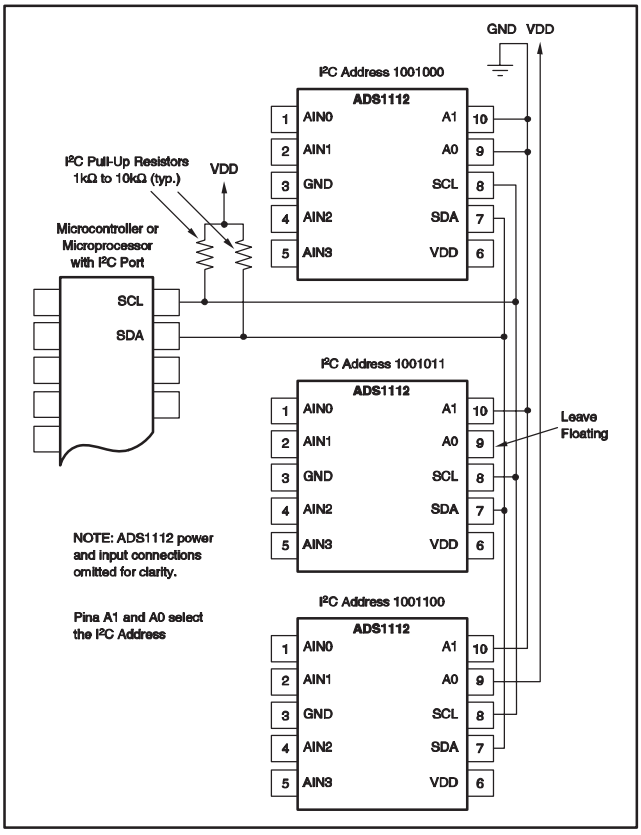


Figure 5. Connecting Multiple ADS1112s

Note that only one set of pull-up resistors is needed per bus. The pull-up resistor values may need to be lowered slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

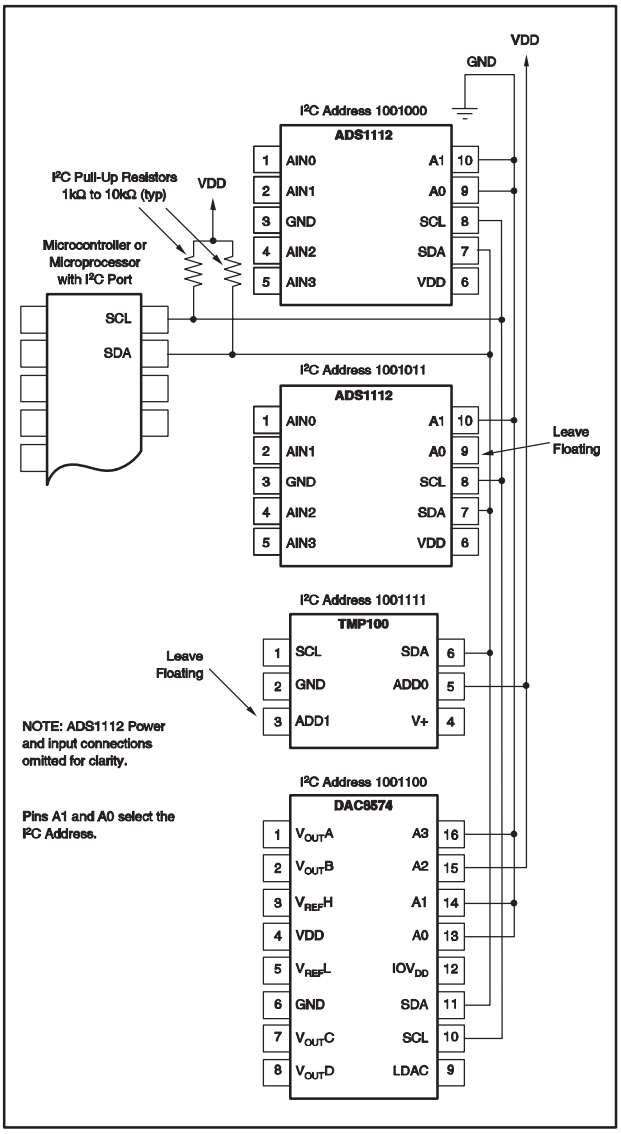


Figure 6. Connecting Multiple Device Types

The TMP100 and DAC8574 devices detect their I²C bus addresses based on the states of pins. In the example, the TMP100 has the address 1001111, and the DAC8574 has the address 1001100. Consult the DAC8574 and TMP100 data sheets, located at www.ti.com, for further details.

USING GPIO PORTS FOR I²C

Most microcontrollers have programmable input/output pins that can be set in software to act as inputs or outputs. If an I²C controller is not available, the ADS1112 can be connected to GPIO pins and the I²C bus protocol simulated, or "bit-banged," in software. An example of this for a single ADS1112 is shown in Figure 7.

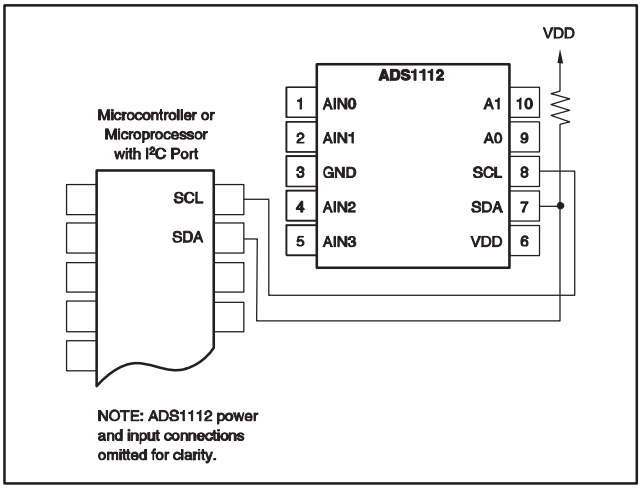


Figure 7. Using GPIO with a Single ADS1112

Bit-banging I²C with GPIO pins can be done by setting the GPIO line to zero and toggling it between input and output modes to apply the proper bus states. To drive the line LOW, the pin is set to output a zero; to let the line go HIGH, the pin is set to input. When the pin is set to input, the state of the pin can be read; if another device is pulling the line low, this will read as a zero in the port's input register.

Note that no pull-up resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to one or zero as appropriate. It can do this because the ADS1112 never drives its clock line LOW. This technique can also be used with multiple devices, and has the advantage of lower current consumption due to the absence of a resistive pull-up.

If there are any devices on the bus that may drive their clock lines LOW, the above method should not be used; the SCL line should be high-Z or zero and a pull-up resistor provided as usual. Note also that this cannot be done on the SDA line in any case, because the ADS1112 does drive the SDA line LOW from time to time, as do all I²C devices.

Some microcontrollers have selectable strong pull-up circuits built in to their GPIO ports. In some cases, these can be switched on and used in place of an external pull-up resistor. Weak pull-ups are also provided on some microcontrollers, but usually these are too weak for I²C communication. If there is any doubt about the matter, test the circuit before committing it to production.

SINGLE-ENDED INPUTS

Although the ADS1112 has two differential inputs, it can easily measure three single-ended signals. A single-ended connection scheme is shown in Figure 8. The ADS1112 is configured for single-ended measurement by grounding the AIN3 pin and applying the input signals to any of AIN0, AIN1, or AIN2. Then the data is read out of one of the inputs based on the selection on the configuration register. The single-ended signal can range from 0V to 2.048V. The ADS1112 loses no linearity anywhere in its input range. Negative voltages cannot be applied to this circuit because the ADS1112 can only accept positive voltages.

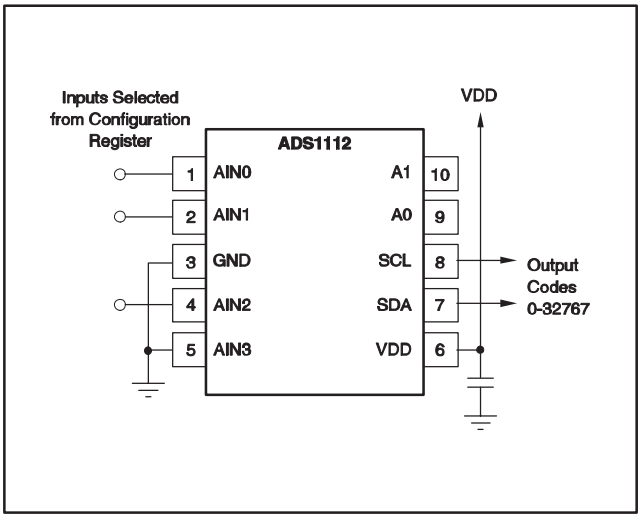


Figure 8. Measuring Single-Ended Inputs

The ADS1112 input range is bipolar differential with respect to the reference, that is, 2.048V. The single-ended circuit shown in Figure 8 covers only half the ADS1112 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost. If AIN3 is set to a higher voltage, negative single-ended voltage can be measured.

LOW-SIDE CURRENT MONITOR

Figure 9 shows a circuit for a low-side shunt-type current monitor. The circuit reads the voltage across a shunt resistor, which is sized as small as possible while still giving a readable output voltage. This voltage is amplified by an OPA335 low-drift op amp, and the result is read by the ADS1112.

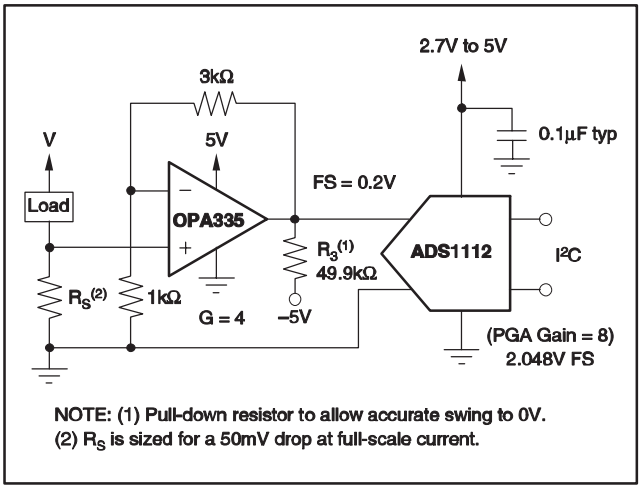


Figure 9. Low-Side Current Measurement

It is suggested that the ADS1112 be operated at a gain of 8. The gain of the OPA335 can then be set lower. For a gain of 8, the op amp should be set up to give a maximum output voltage of no greater than 0.256V. If the shunt resistor is sized to provide a maximum voltage drop of 50mV at full-scale current, the full-scale input to the ADS1112 is 0.2V.

The ADS1112 is fabricated in a small-geometry, low-voltage process. The analog inputs feature protection diodes to the supply rails. However, the current-handling ability of these diodes is limited, and the ADS1112 can be permanently damaged by analog input voltages that remain more than approximately 300mV beyond the rails for extended periods. One way to protect against overvoltage is to place current-limiting resistors on the input lines. The ADS1112 analog inputs can withstand momentary currents of as large as 10mA.

The previous paragraph does not apply to the I^2C ports, which can both be driven to 6V regardless of the supply.

If the ADS1112 is driven by an op amp with high-voltage supplies, such as ±12V, protection should be provided, even if the op amp is configured so that it does not output out-of-range voltages. Many op amps seek to one of the supply rails immediately when power is applied, usually before the input has stabilized; this momentary spike can damage the ADS1112. This incremental damage results in slow, long-term failure—which can be disastrous for permanently installed, low-maintenance systems.

If an op amp or other front-end circuitry is used with the ADS1112, its performance characteristics must be taken into account.

PACKAGE OPTION ADDENDUM

30-Sep-2014

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1112IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BHU	Samples
ADS1112IDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BHU	Samples
ADS1112IDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BHU	Samples
ADS1112IDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BHU	Samples
ADS1112IDRCR	ACTIVE	VSON	DRC	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BHV	Samples
ADS1112IDRCRG4	ACTIVE	VSON	DRC	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BHV	Samples
ADS1112IDRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BHV	Samples
ADS1112IDRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BHV	Samples

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

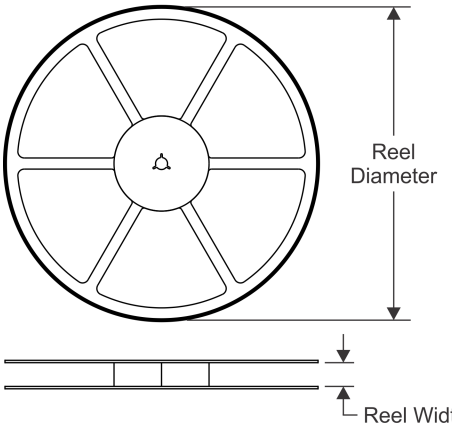
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

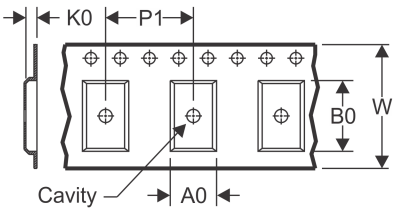
1-Oct-2014

TAPE AND REEL INFORMATION

REEL DIMENSIONS

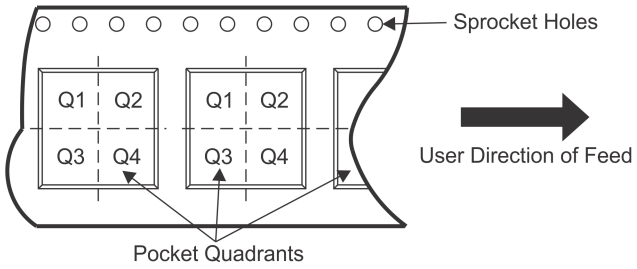


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



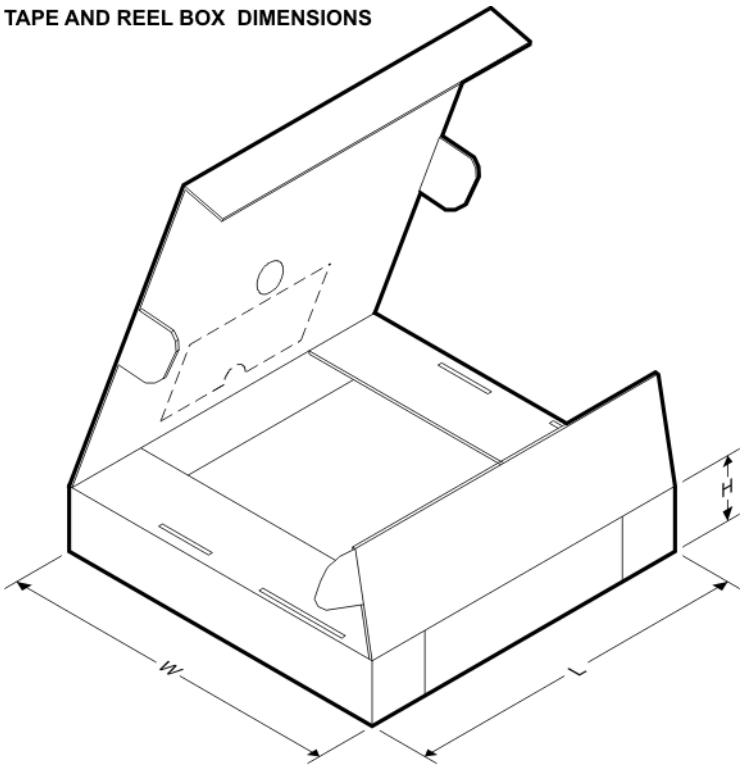
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1112IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS1112IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS1112IDRCR	VSON	DRC	10	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS1112IDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

PACKAGE MATERIALS INFORMATION

1-Oct-2014

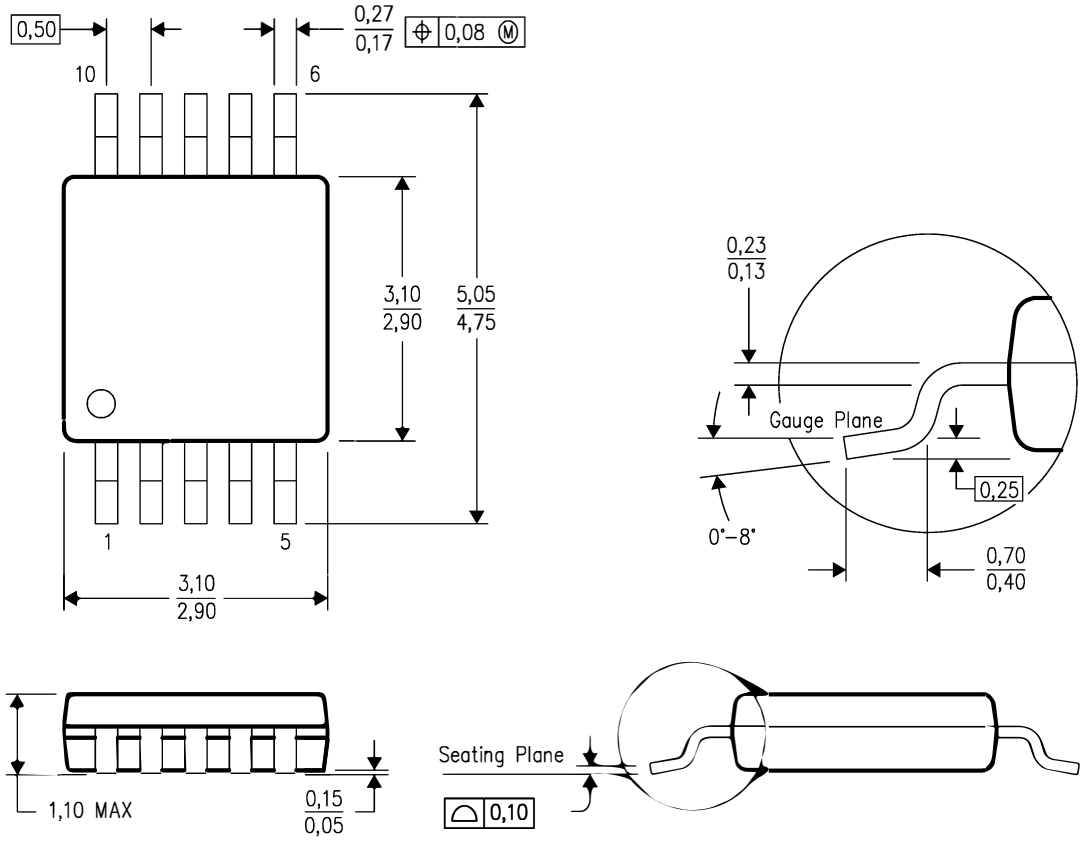
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1112IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
ADS1112IDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
ADS1112IDRCR	VSON	DRC	10	2500	367.0	367.0	35.0
ADS1112IDRCT	VSON	DRC	10	250	210.0	185.0	35.0

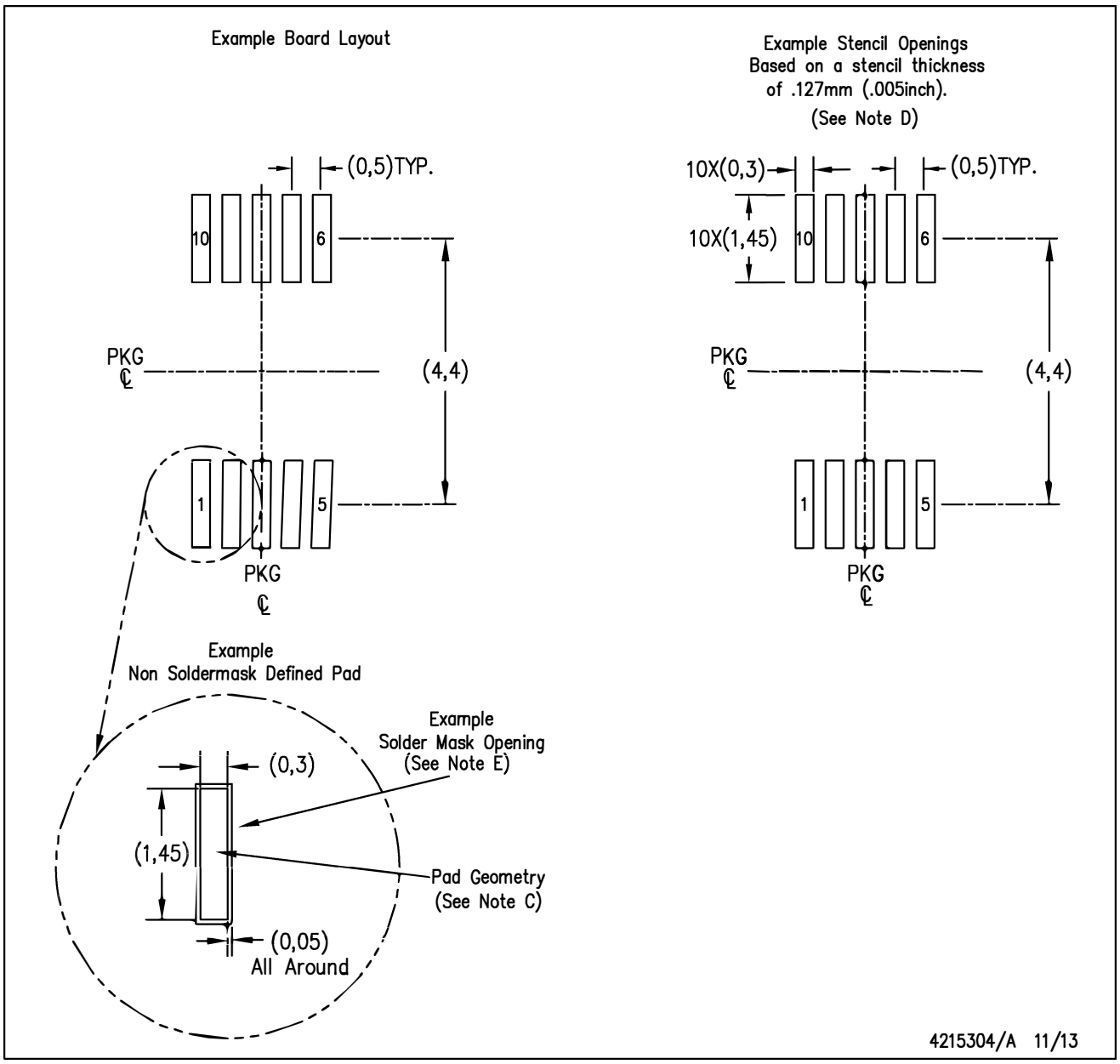
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

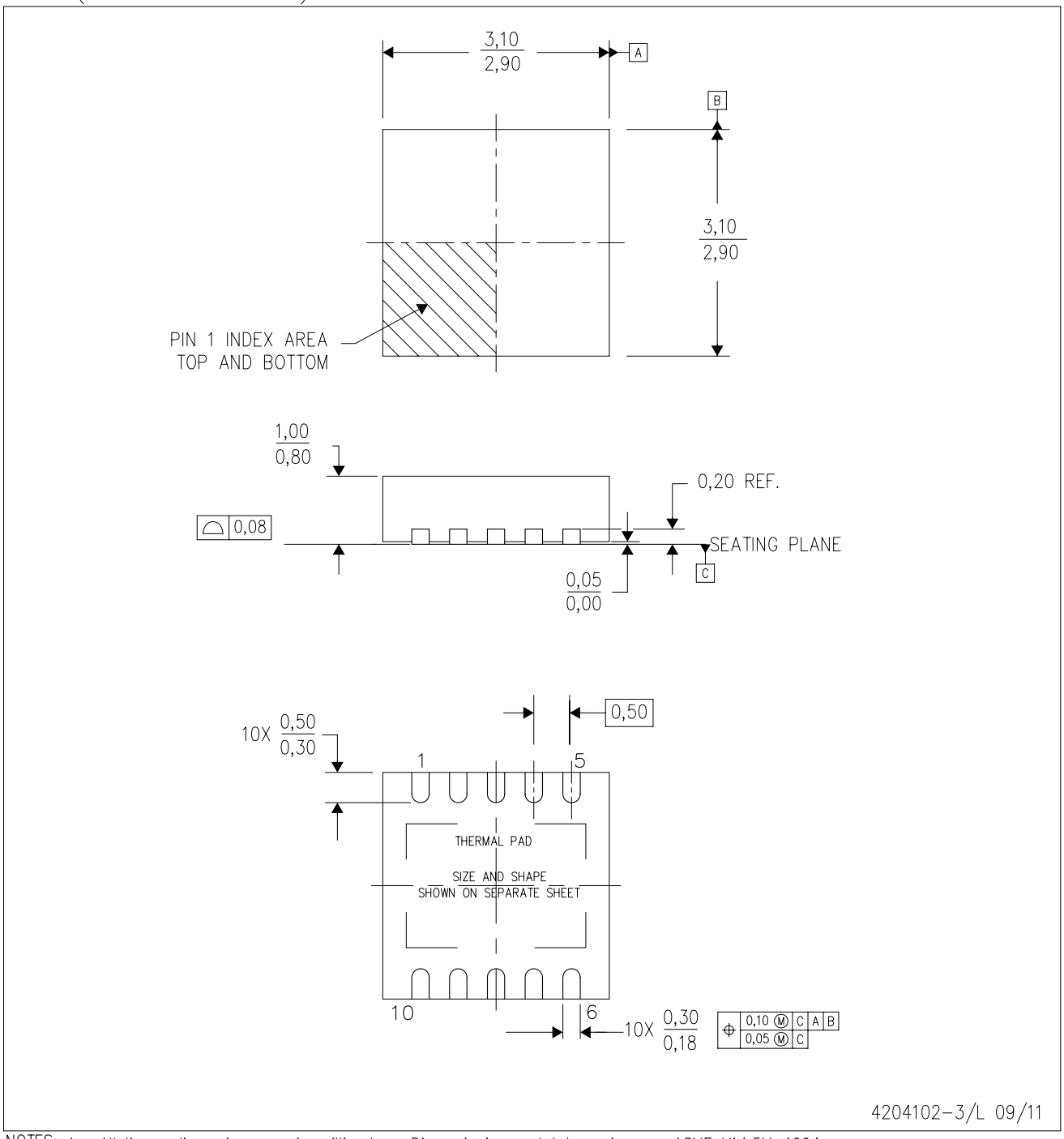
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

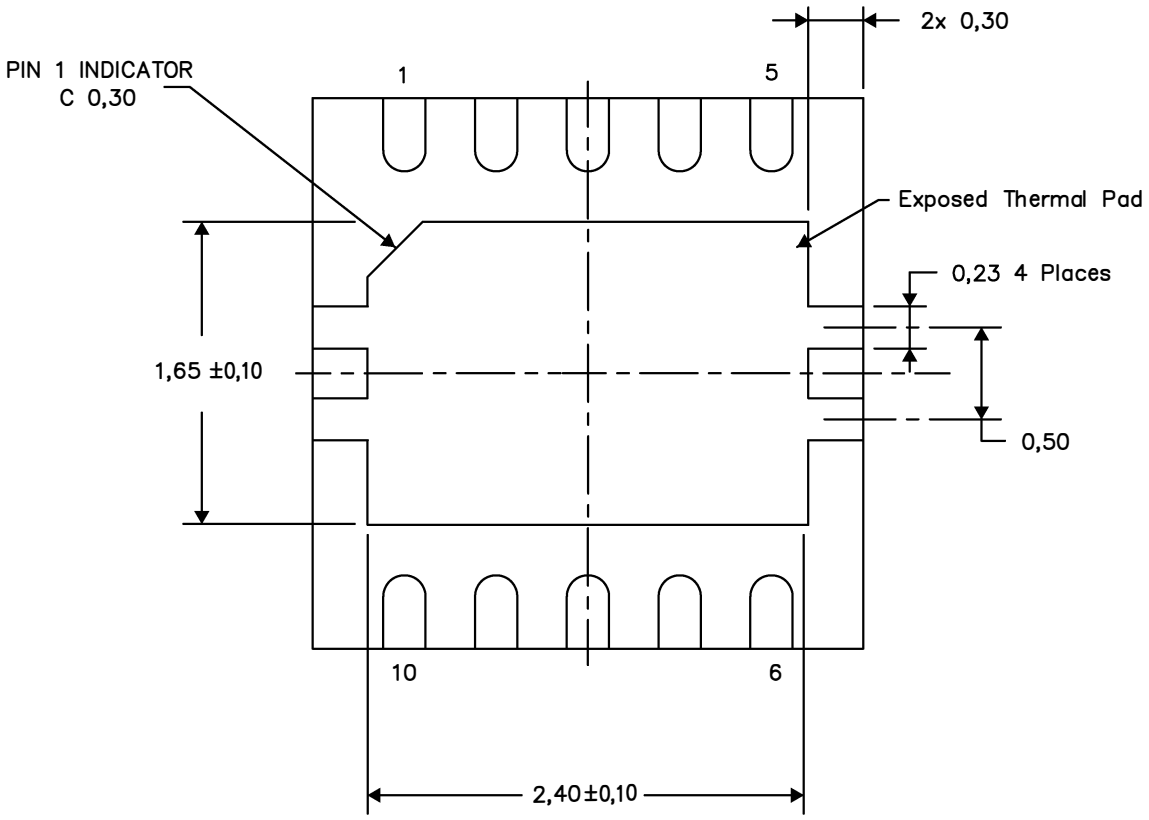
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



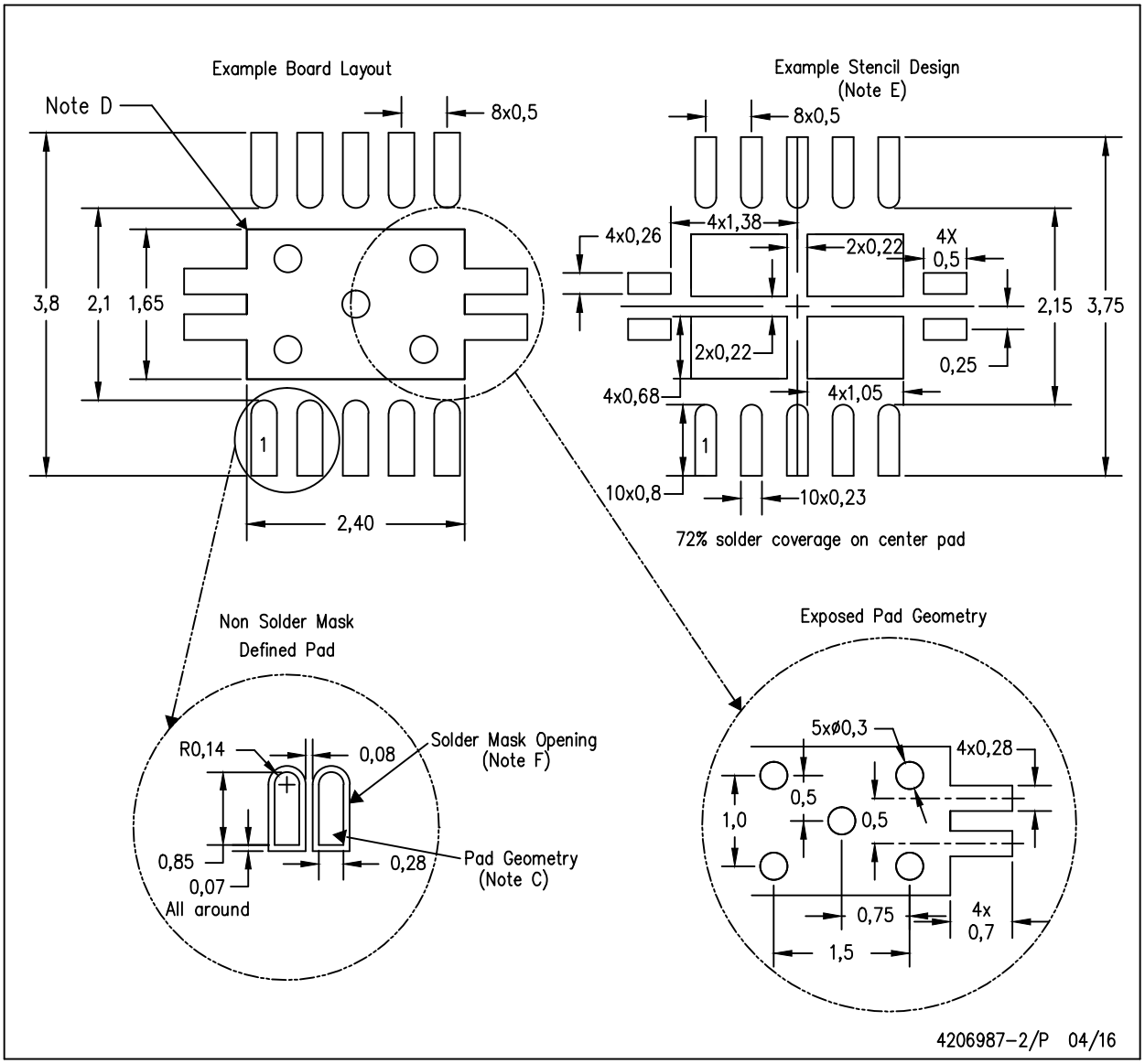
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.