JW5033T

18V/2A

Sync. Step-Down Converter

Parameters Subject to Change Without Notice

DESCRIPTION

The JW®5033T is a current mode monolithic buck voltage converter. Operating with an input range of 3.7V-18V, the JW5033T delivers 2A of continuous output current with two integrated N-Channel MOSFETs. At light loads, regulators operate in low frequency to maintain high efficiency and low output ripple.

The JW5033T guarantees robustness with short circuit protection, thermal protection, current run-away protection, and input under voltage lockout.

The JW5033T is available in a 6-pin TSOT23-6 package, which provides a compact solution with minimal external components.

FEATURES

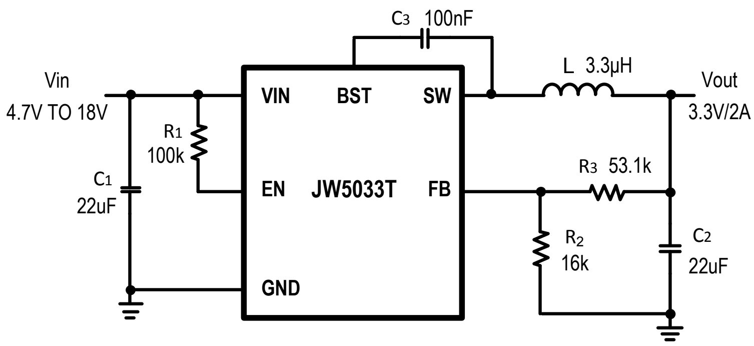
- 3.7V to 18V operating input range
  2A output current
- Up to 95% efficiency
- High efficiency at light load
- Fixed 800kHz Switching frequency
- Input under voltage lockout
- Start-up current run-away protection
- Over current protection and Hiccup
- Thermal protection
- Available in TSOT23-6 package

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

TYPICAL APPLICATION

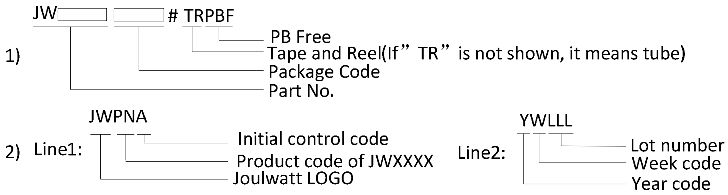
3.3V/2A Step Down Regulator



ORDER INFORMATION

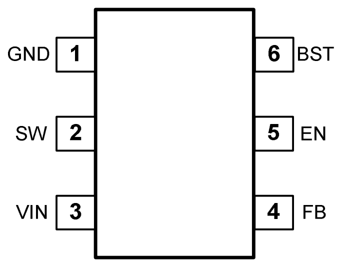
DEVICE[1]	PACKAGE	TOP MARKING[2]
JW5033TTSOTB#TRPBF	TSOT23-6	JWCDX YWLLL

Notes：



PIN CONFIGURATION

TOP VIEW



TSOT23-6

ABSOLUTE MAXIMUM RATING[1)]

VIN, EN, SW Pin .... -0.3V to 20V
SW..................................... -0.3V(-4.5V for 10ns) to 20V(22V for 10ns)
BST Pin .... SW-0.3V to SW+5V
All other Pins .... -0.3V to 6V
Junction Temp. [2) 3)] 150ºC
Lead Temperature 260ºC
ESD Susceptibility (Human Body Model) 2kV

RECOMMENDED OPERATING CONDITIONS

Input Voltage VIN .... 3.7V to 18V
Output Voltage Vout ....0.765V to VIN-3V

THERMAL PERFORMANCE[4)]

Absolute Max Storage Temp.	Recommended Operating Junction Temp. Range	Recommended Max Case Temp. T_C (ºC)	Abs. Max Junction Temp. T_j (ºC)	Recommended Max Power Loss P_D@25ºC (W)
-65ºC to 150ºC	-40ºC to 125ºC	119	150	0.9
$R_{\theta JC}$ (ºC/W)	$R_{\theta JA}$ (ºC/W)	$R_{\theta JB}$ (ºC/W)	ψ_{JT} (ºC/W)	ψ_{JB} (ºC/W)
55	110	14.7	1.2	14.7

Note：

1) Exceeding these ratings may damage the device.

2) The JW5033T guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

3) The JW5033T includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

VIN=12V, T_A=25℃, Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_MIN}	V_{IN} rising	3.2	3.4	3.7	V
V_{IN} Under voltage Lockout Hysteresis[5)]	$V_{IN\_MIN\_HYST}$			300		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V		0.1	1	μA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1.2V		120	150	μA
Feedback Voltage	V_{FB}	3.7V<V_{VIN}<18V	742	765	788	mV
Top Switch Resistance[5)]	$R_{DS(ON)T}$			130		mΩ
Bottom Switch Resistance[5)]	$R_{DS(ON)B}$			70		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=18V, V_{EN}=0V, V_{SW}=0V		0.1	1	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=18V, V_{EN}=0V, V_{SW}=18V		0.1	1	μA
Top Switch Current Limit[5)]	I_{LIM_TOP}	Minimum Duty Cycle	3.2	3.9		A
Switch Frequency	F_{SW}		600	800	1000	kHz
Minimum On Time[5)]	T_{ON_MIN}			100		ns
Minimum Off Time[5)]	T_{OFF_MIN}	V_{FB}=0.4V		150		ns
EN high level input voltage	V_{EN_H}	V_{EN} rising	2.4			V
EN low level input voltage	V_{EN_L}	V_{EN} falling			0.6	V
Soft-Start Period	t_{SS}			1.2		ms
Thermal Shutdown[5)]	T_{TSD}			145		°C
Thermal Shutdown hysteresis[5)]	T_{TSD_HYST}			20		°C

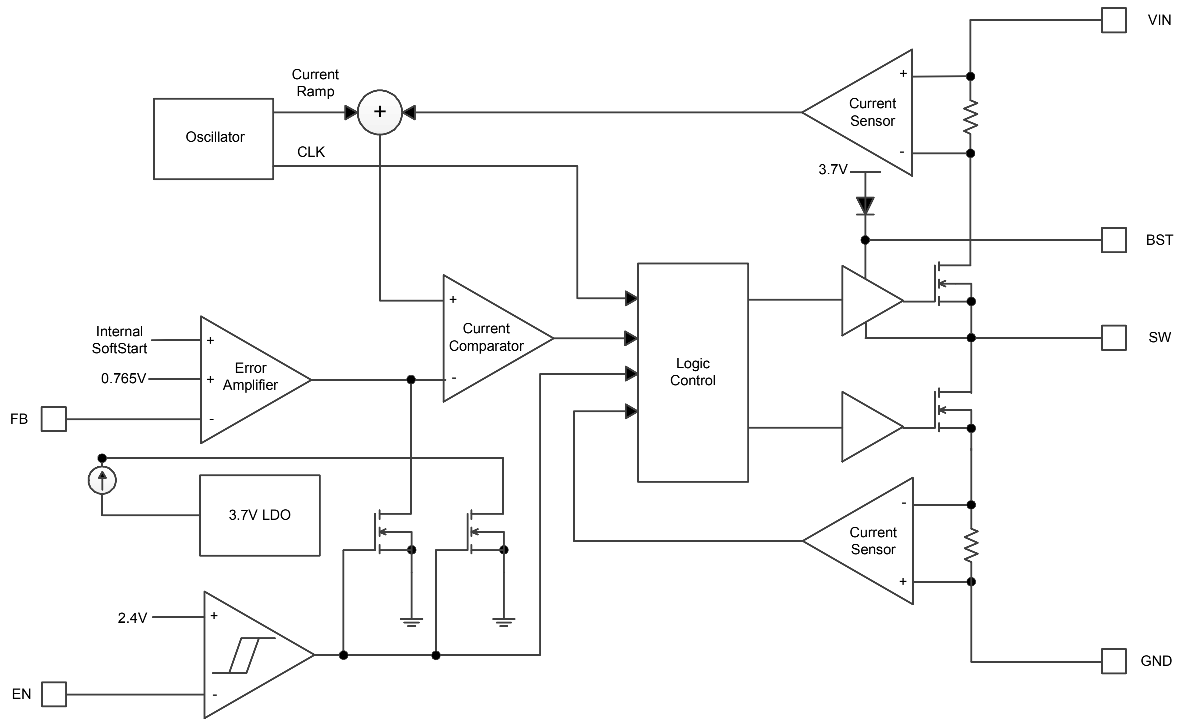
Note:

5) Guaranteed by design.

PIN DESCRIPTION

TSOT23-6 Pin	Name	Description
1	GND	Ground.
2	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 3.7V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.765V. Connect a resistive divider at FB.
5	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
6	BST	Bootstrap pin for top switch. A 0.1uF or larger capacitor should be connected between this pin and the SW pin to supply current to the top switch and top switch driver.

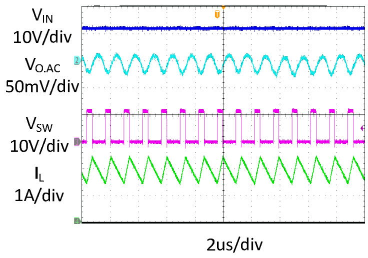
BLOCK DIAGRAM



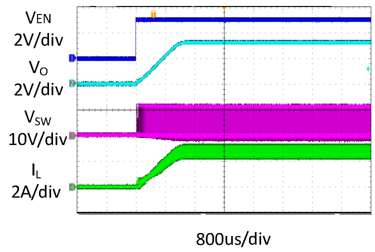
TYPICAL PERFORMANCE CHARACTERISTICS

Vin =12V, Vout = 3.3V, L = 3.3μH, Cout = 22μF, TA = +25°C, unless otherwise noted

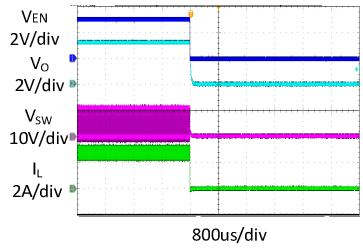
Steady State Test
VIN=12V, Vout=3.3V
Iout=2A



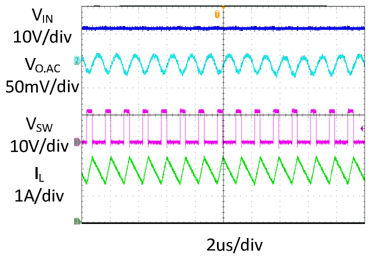
Startup through Enable
VIN=12V, Vout=3.3V
Iout=2A(Resistive load)



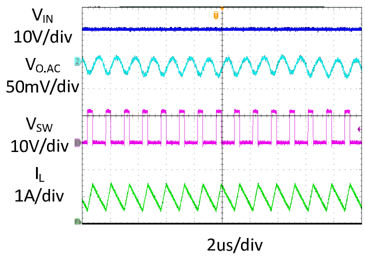
Shutdown through Enable
VIN=12V, Vout=3.3V
Iout=2A (Resistive load)



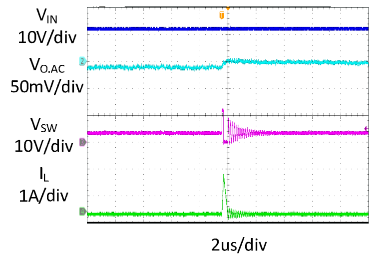
Heavy Load Operation
2A LOAD



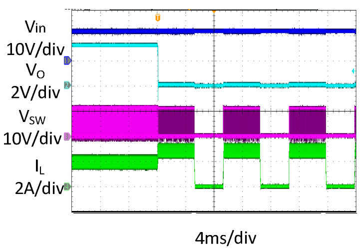
Medium Load Operation
1A LOAD



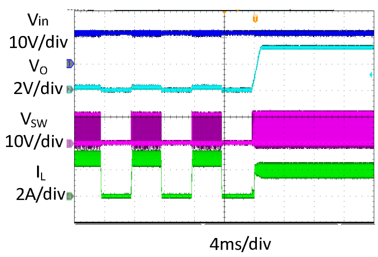
Light Load Operation
0 A LOAD



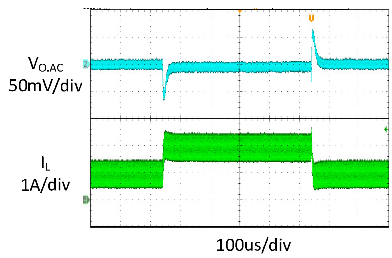
Short Circuit Protection
VIN=12V, Vout=3.3V
Iout=2A- Short



Short Circuit Recovery
VIN=12V, Vout=3.3V
Iout= Short-2A



Load Transient
1A LOAD → 2A LOAD → 1A LOAD
Current Slew rate: 2.5A/us



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Vin=12V, TA = +25°C, unless otherwise noted

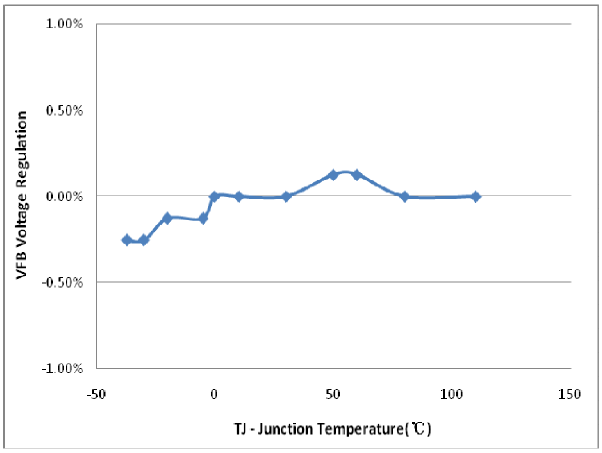


Figure 1. VFB Volatge Regulation vs Junction Temperature

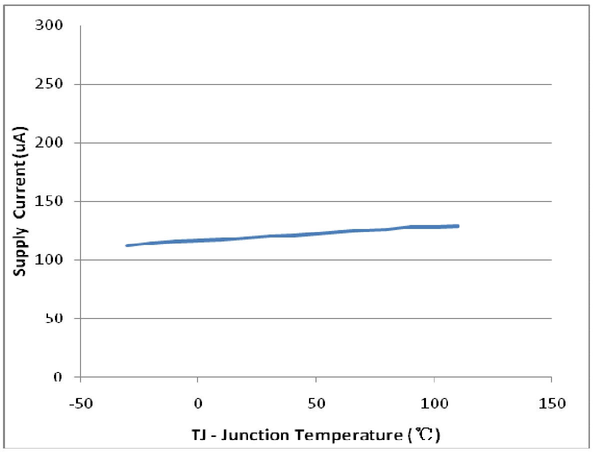


Figure 2. Supply Current vs Junction Temperature

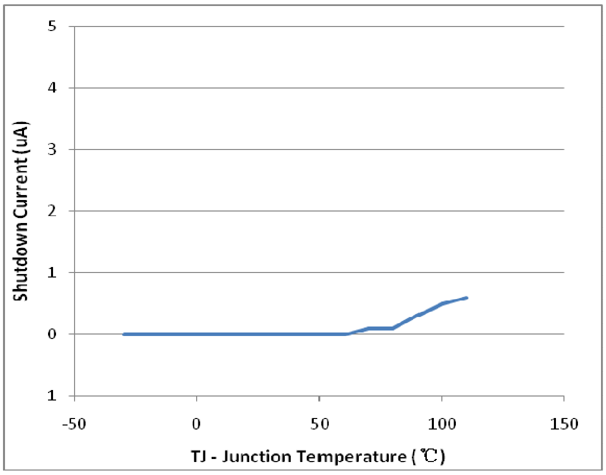


Figure 3. Shutdown Current vs Junction Temperature

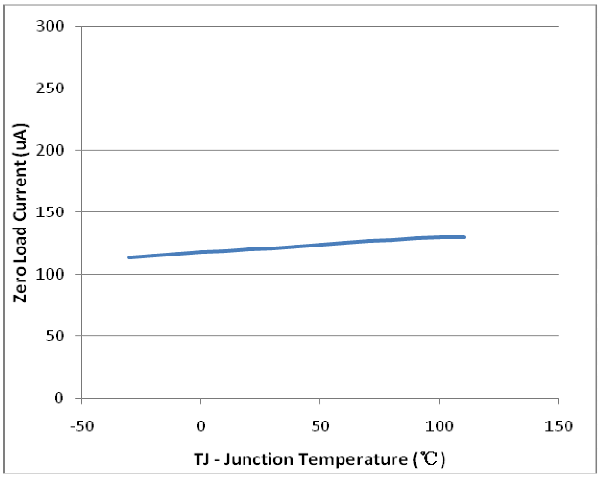


Figure 4. Zero-Load Current vs Junction Temperature

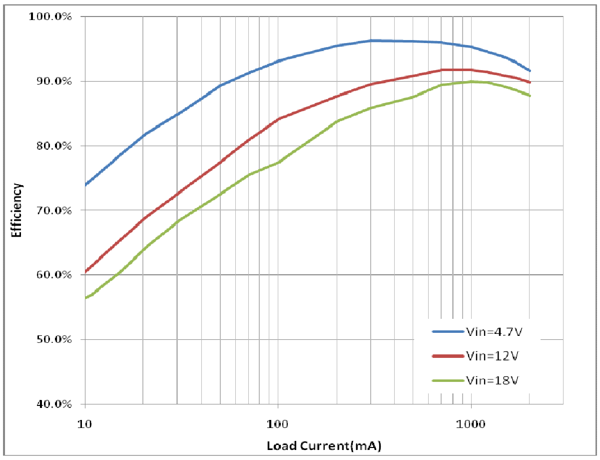


Figure 5. Efficiency vs Load Current (Vout=3.3V)

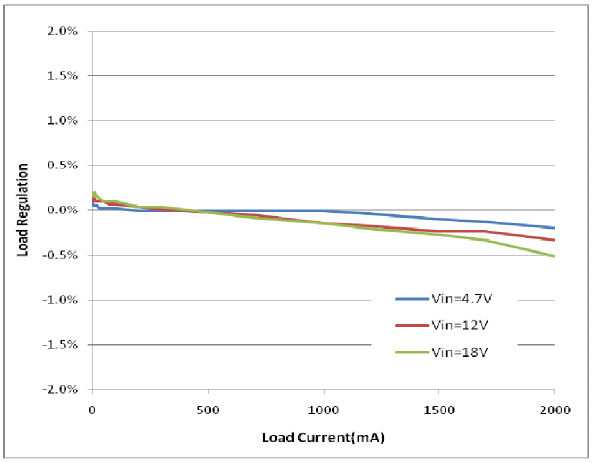


Figure 6. Output Voltage Regulation vs Load Current (Vout=3.3V)

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Vin=12V, TA = +25°C, unless otherwise noted

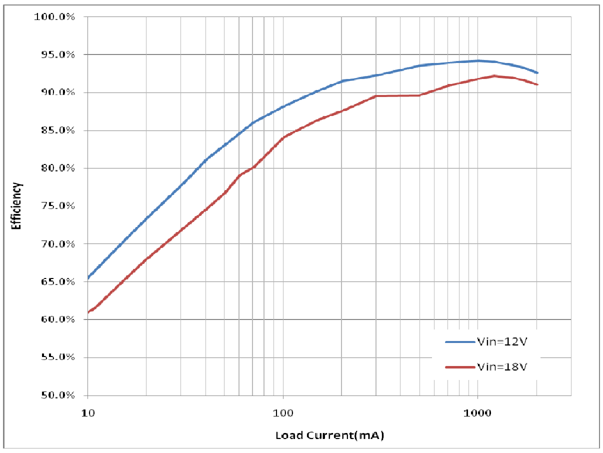


Figure 7. Efficiency vs Load Current
(Vout=5V)

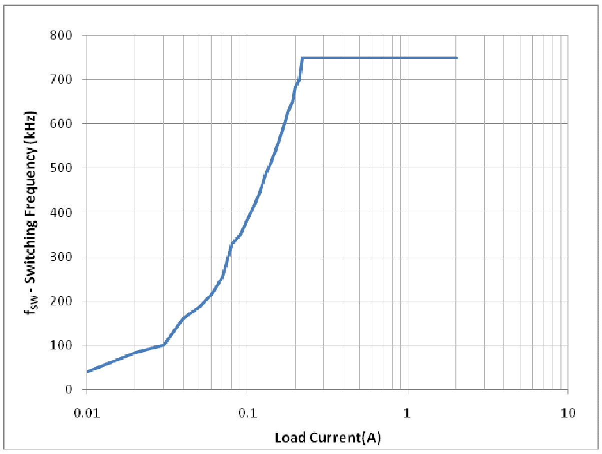


Figure 8. Switching Frequency vs Load Current
(Vout=1V)

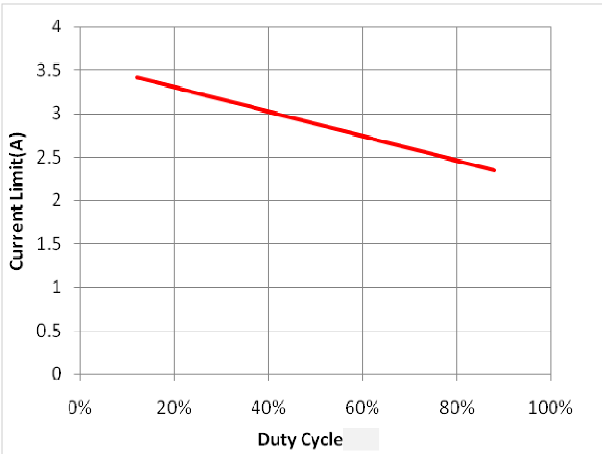


Figure 9.DutyCycle vs Current Limit

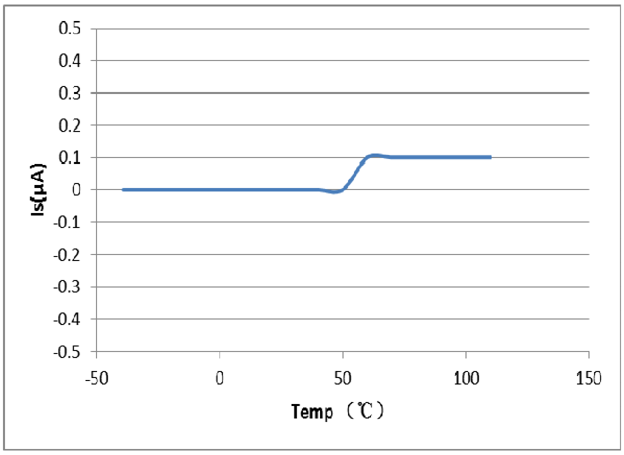


Figure 10. Temperature vs Is

FUNCTIONAL DESCRIPTION

The JW5033T is a synchronous, current-mode, step-down regulator. It regulates input voltages from 3.7V to 18V down to an output voltage as low as 0.765V, and is capable of supplying up to 2A of load current.

Current-Mode Control

The JW5033T utilizes current-mode control to regulate the FB voltage. Voltage at the FB pin is regulated at 0.765V so that by connecting an appropriate resistive divider between VOUT and GND, designed output voltage can be achieved.

PFM Mode

The JW5033T operates in PFM mode at light load. In PFM mode, switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

Internal Soft-Start.

Soft-Start makes output voltage rising smoothly follow an internal SS voltage until SS voltage is higher than the internal reference voltage. It can prevent overshoot of output voltage when startup.

Power Switch

N-Channel MOSFET switches are integrated on the JW5033T to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.7V rail when SW is low.

Vin Under-Voltage Protection

A resistive divider can be connected between Vin and GND, with the central tap connected to EN, so that when Vin drops to the pre-set value, EN drops below 1.8V to trigger input under voltage lockout protection.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductance can be easily built up, resulting in a large start-up output current. A valley current limit is designed in the JW5033T so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Over Current Protection and Hiccup

JW5033T has a cycle-by-cycle current limit. When the inductor current triggers current limit, JW5033T enters hiccup mode and periodically restart the chip.

JW5033T will exit hiccup mode while not triggering current limit.

Thermal Protection

When the temperature of the JW5033T rises above 145°C, it is forced into thermal shut-down.

Only when core temperature drops below 125°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_2}{R_2 + R_3}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_2 around 20kΩ, and then R_3 can be calculated by:

$$R_3 = R_2\left(\frac{V_{OUT}}{0.765} - 1\right)$$

Too large resistance and the following table lists the recommended values.

VOUT(V)	R2(kΩ)	R3(kΩ)
2.5	22	49.9
3.3	16	53.1
5	20	110

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_1 is the input capacitance value, f_S is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22uF ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_S \cdot C_2}\right)$$

where C_2 is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 22uF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5033T (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.

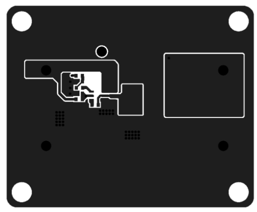


Figure 1. Top Layer

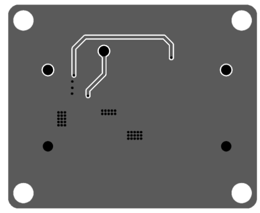


Figure 2. Bottom Layer

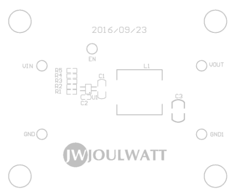


Figure 3. Silk Layer

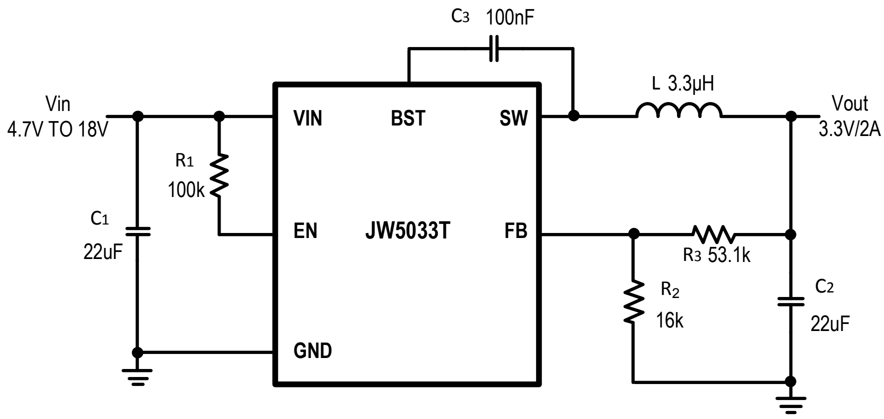
REFERENCE DESIGN

Reference 1：

V_{IN} : 4.7V ~ 18V

V_{OUT}: 3.3V

I_{OUT} : 0~2A

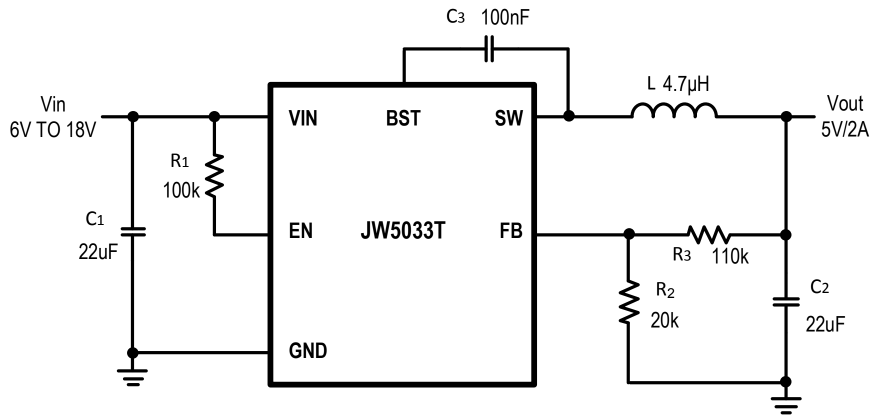


Reference 2：

V_{IN} : 6V ~ 18V

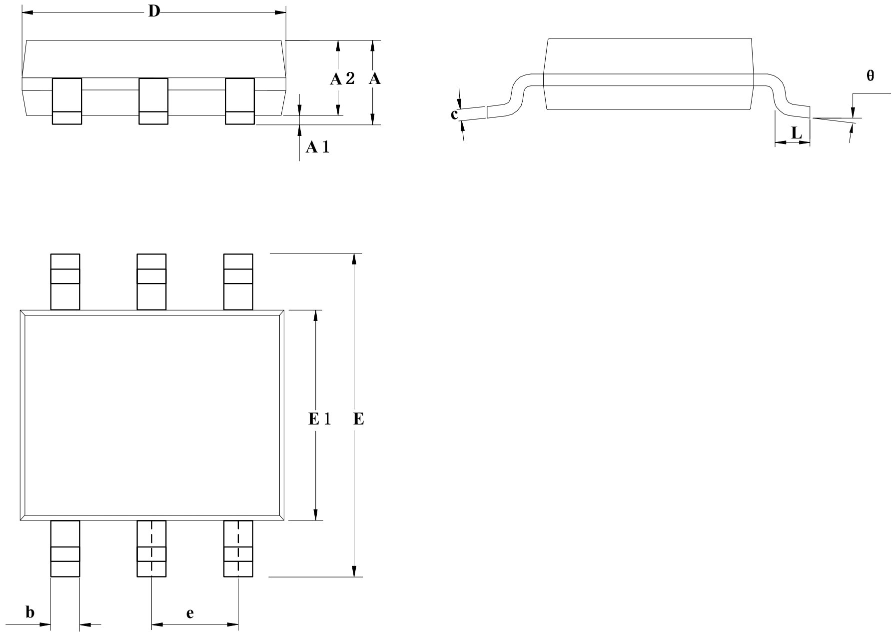
V_{OUT}: 5V

I_{OUT} : 0~2A



PACKAGE OUTLINE

TSOT23-6 UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0	—	0.15
A2	0.55		1.00
b	0.30	0.40	0.50
c	0.08	0.15	0.30
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95（BSC)		
L	0.30	0.45	0.60
θ	0°	—	10°

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