LPV521 NanoPower, 1.8-V, RRIO, CMOS Input, Operational Amplifier

1 Features

- For V_S = 5 V, Typical Unless Otherwise Noted
  - Supply Current at V_{CM} = 0.3 V 400 nA (Max)
  - Operating Voltage Range 1.6 V to 5.5 V
  - Low TCV_{OS} 3.5 µV/°C (Max)
  - V_{OS} 1 mV (Max)
  - Input Bias Current 40 fA
  - PSRR 109 dB
  - CMRR 102 dB
  - Open-Loop Gain 132 dB
  - Gain Bandwidth Product 6.2 kHz
  - Slew Rate 2.4 V/ms
  - Input Voltage Noise at f = 100 Hz 255 nV/√Hz
  - Temperature Range −40°C to 125°C

2 Applications

- Wireless Remote Sensors
- Powerline Monitoring
- Power Meters
- Battery Powered Industrial Sensors
- Micropower Oxygen sensor and Gas Sensor
- Active RFID Readers
- Zigbee Based Sensors for HVAC Control
- Sensor Network Powered by Energy Scavenging

3 Description

The LPV521 is a single nanopower 552-nW amplifier designed for ultra long life battery applications. The operating voltage range of 1.6 V to 5.5 V coupled with typically 351 nA of supply current make it well suited for RFID readers and remote sensor nanopower applications. The device has input common mode voltage 0.1 V over the rails, guaranteed TCV_{OS} and voltage swing to the rail output performance. The LPV521 has a carefully designed CMOS input stage that outperforms competitors with typically 40 fA I_{BIAS} currents. This low input current significantly reduces I_{BIAS} and I_{OS} errors introduced in megohm resistance, high impedance photodiode, and charge sense situations. The LPV521 is a member of the PowerWise™ family and has an exceptional power-to-performance ratio.

The wide input common mode voltage range, guaranteed 1 mV V_{OS} and 3.5 µV/°C TCV_{OS} enables accurate and stable measurement for both high-side and low-side current sensing.

EMI protection was designed into the device to reduce sensitivity to unwanted RF signals from cell phones or other RFID readers.

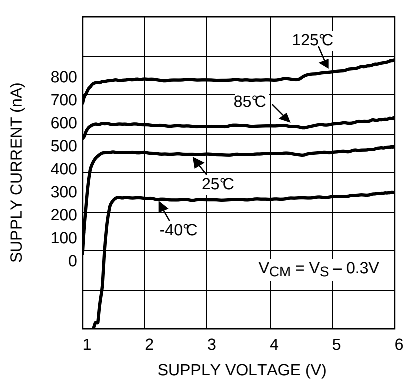
The LPV521 is offered in the 5-pin SC70 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LPV521	SC70 (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Nanopower Supply Current



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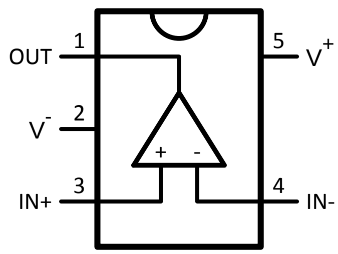
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (Feburary 2013) to Revision D	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

SC70-5 Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUT	O	Output
2	V-	P	Negative Power Supply
3	IN+	I	Noninverting Input
4	IN-	I	Inverting Input
5	V+	P	Positive Power Supply

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Any pin relative to V^-		−0.3	6	V
IN+, IN-, OUT Pins		V^- – 0.3 V	V^+ + 0.3 V	V
V^+, V^-, OUT Pins			40	mA
Differential Input Voltage (V_{IN+} - V_{IN-})		–300	300	mV
Junction Temperature(2)		–40	150	°C
Mounting Temperature	Infrared or Convection (30 sec.)		260	°C
	Wave Soldering Lead Temp. (4 sec.)		260	°C
Storage temperature, T_{stg}		−65	150	°C

(1) *Absolute Maximum Ratings* indicate limits beyond which damage may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) The maximum power dissipation is a function of TJ(MAX), θJA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(MAX) – TA)/ θJA. All numbers apply for packages soldered directly onto a PC Board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine Model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions[1]

	MIN	MAX	UNIT
Temperature Range[2]	−40	125	°C
Supply Voltage ($V_S = V^+ - V^-$)	1.6	5.5	V

(1) *Absolute Maximum Ratings* indicate limits beyond which damage may occur. *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see *Electrical Characteristics*.
(2) The maximum power dissipation is a function of TJ(MAX), θJA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(MAX) – TA)/ θJA. All numbers apply for packages soldered directly onto a PC Board.

6.4 Thermal Information

THERMAL METRIC[1]		DCK	UNIT
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	456	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of TJ(MAX), θJA. The maximum allowable power dissipation at any ambient temperature is PD = (TJ(MAX) – TA)/ θJA. All numbers apply for packages soldered directly onto a PC Board.

6.5 1.8-V DC Electrical Characteristics

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 1.8 V, V^- = 0 V, $V_{CM} = V_O = V^+/2$, and R_L > 1 MΩ.[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.3 V	–1	0.1	1	mV
		Temperature extremes	–1.23		1.23	
		V_{CM} = 1.5 V	–1	0.1	1	
		Temperature extremes	–1.23		1.23	
TCV_{OS}	Input Offset Voltage Drift[2]			±0.4		μV/°C
		Temperature extremes	–3		3	
I_{BIAS}	Input Bias Current		–1	0.01	1	pA
		Temperature extremes	–50		50	
I_{OS}	Input Offset Current			10		fA
CMRR	Common Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 1.8 V	66	92		dB
		Temperature extremes	60			
		0 V ≤ V_{CM} ≤ 0.7 V	75	101		
		Temperature extremes	74			
		1.2 V ≤ V_{CM} ≤ 1.8 V	75	120		
		Temperature extremes	53			
PSRR	Power Supply Rejection Ratio	1.6 V ≤ V^+ ≤ 5.5 V V_{CM} = 0.3 V	85	109		dB
		Temperature extremes	76			
CMVR	Common Mode Voltage Range	CMRR ≥ 67 dB CMRR ≥ 60 dB	0 0		 1.8	V
		Temperature extremes			1.8	
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 V to 1.3 V R_L = 100 kΩ to $V^+/2$	74	125		dB
		Temperature extremes	73			

1.8-V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L > 1 MΩ.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output Swing High	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = 100 mV		2	50	mV from either rail
		Temperature extremes			50	
	Output Swing Low	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = −100 mV		2	50	
		Temperature extremes			50	
I_O	Output Current(3)	Sourcing, V_O to V^- V_{IN}(diff) = 100 mV	1	3		mA
		Temperature extremes	0.5			
		Sinking, V_O to V^+ V_{IN}(diff) = −100 mV	1	3		
		Temperature extremes	0.5			
I_S	Supply Current	V_{CM} = 0.3 V		345	400	nA
		Temperature extremes			580	
		V_{CM} = 1.5 V		472	600	
		Temperature extremes			850	

(3) The short circuit test is a momentary open-loop test.

6.6 1.8-V AC Electrical Characteristics

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L > 1 MΩ.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GBW	Gain-Bandwidth Product	C_L = 20 pF, R_L = 100 kΩ			6.1		kHz
SR	Slew Rate	A_V = +1, V_{IN} = 0V to 1.8V	Falling Edge		2.9		V/ms
			Rising Edge		2.3		
θ_m	Phase Margin	C_L = 20 pF, R_L = 100 kΩ			72		deg
G_m	Gain Margin	C_L = 20 pF, R_L = 100 kΩ			19		dB
e_n	Input-Referred Voltage Noise Density	f = 100 Hz			265		nV/√Hz
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz			24		μV_{PP}
I_n	Input-Referred Current Noise	f = 100 Hz			100		fA/√Hz

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ TA. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

6.7 3.3-V DC Electrical Characteristics

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 3.3 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L > 1 MΩ.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.3 V	–1	0.1	1	mV
		Temperature extremes	–1.23		1.23	
		V_{CM} = 3 V	–1	0.1	1	
		Temperature extremes	–1.23		1.23	
TCV_{OS}	Input Offset Voltage Drift(2)			±0.4		µV/°C
		Temperature extremes	–3		3	
I_{BIAS}	Input Bias Current		–1	0.01	1	pA
		Temperature extremes	–50		50	
I_{OS}	Input Offset Current			20		fA
CMRR	Common Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 3.3 V	72	97		dB
		Temperature extremes	70			
		0 V ≤ V_{CM} ≤ 2.2 V	78	106		
		Temperature extremes	75			
		2.7 V ≤ V_{CM} ≤ 3.3 V	77	121		
		Temperature extremes	76			
PSRR	Power Supply Rejection Ratio	1.6 V ≤ V^+ ≤ 5.5 V V_{CM} = 0.3 V	85	109		dB
		Temperature extremes	76			
CMVR	Common Mode Voltage Range	CMRR ≥ 72 dB CMRR ≥ 70 dB	−0.1		3.4	V
		Temperature extremes	0		3.3	
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 V to 2.8 V R_L = 100 kΩ to $V^+/2$	82	120		dB
		Temperature extremes	76			
V_O	Output Swing High	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = 100 mV		3	50	mV from either rail
		Temperature extremes			50	
	Output Swing Low	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = −100 mV		2	50	
		Temperature extremes			50	
I_O	Output Current(3)	Sourcing, V_O to V^- V_{IN}(diff) = 100 mV	5	11		mA
		Temperature extremes	4			
		Sinking, V_O to V^+ V_{IN}(diff) = −100 mV	5	12		
		Temperature extremes	4			
I_S	Supply Current	V_{CM} = 0.3 V		346	400	nA
		Temperature extremes			600	
		V_{CM} = 3 V		471	600	
		Temperature extremes			860	

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ TA. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) The offset voltage average drift is determined by dividing the change in VOS at the temperature extremes by the total temperature change.
(3) The short circuit test is a momentary open-loop test.

6.8 3.3-V AC Electrical Characteristics

Unless otherwise is specified, all limits for T_A = 25°C, V^+ = 3.3 V, V^- = 0 V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ.(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GBW	Gain-Bandwidth Product	C_L = 20 pF, R_L = 100 kΩ			6.2		kHz
SR	Slew Rate	A_V = +1, V_{IN} = 0V to 3.3V	Falling Edge		2.9		V/ms
			Rising Edge		2.5		
θ_m	Phase Margin	C_L = 20 pF, R_L = 10 kΩ			73		deg
G_m	Gain Margin	C_L = 20 pF, R_L = 10 kΩ			19		dB
e_n	Input-Referred Voltage Noise Density	f = 100 Hz			259		nV/√Hz
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz			22		μV_{PP}
I_n	Input-Referred Current Noise	f = 100 Hz			100		fA/√Hz

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ TA. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

6.9 5-V DC Electrical Characteristics

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = V^+/2, and R_L > 1 MΩ.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage	V_{CM} = 0.3 V		0.1	±1	mV
		Temperature extremes	–1.23		1.23	
		V_{CM} = 4.7 V		0.1	±1	
		Temperature extremes	–1.23		1.23	
TCV_{OS}	Input Offset Voltage Drift(2)			±0.4		μV/°C
		Temperature extremes	–3.5		3.5	
I_{BIAS}	Input Bias Current			0.04	±1	pA
		Temperature extremes	–50		50	
I_{OS}	Input Offset Current			60		fA
CMRR	Common Mode Rejection Ratio	0 V ≤ V_{CM} ≤ 5.0 V	75	102		dB
		Temperature extremes	74			
		0 V ≤ V_{CM} ≤ 3.9 V	84	108		
		Temperature extremes	80			
			77	115		
		Temperature extremes	76			
PSRR	Power Supply Rejection Ratio	1.6 V ≤ V^+ ≤ 5.5 V V_{CM} = 0.3 V	85	109		dB
		Temperature extremes	76			
CMVR	Common Mode Voltage Range	CMRR ≥ 75 dB CMRR ≥ 74 dB	−0.1		5.1	V
		Temperature extremes	0		5	
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 V to 4.5 V R_L = 100 kΩ to V^+/2	84	132		dB
		Temperature extremes	76			

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ TA. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) The offset voltage average drift is determined by dividing the change in VOS at the temperature extremes by the total temperature change.

5-V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L > 1 MΩ.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output Swing High	R_L = 100 kΩ to $V^+/2$ V_{IN}(diff) = 100 mV		3	50	mV from either rail
		Temperature extremes			50	
	Output Swing Low	R_L = 100 kΩ to $V^+/2$ V_{IN} (diff) = −100 mV		3	50	
		Temperature extremes			50	
I_O	Output Current	Sourcing, V_O to V^- V_{IN}(diff) = 100 mV	15	23		mA
		Temperature extremes	8			
		Sinking, V_O to V^+ V_{IN}(diff) = −100 mV	15	22		
		Temperature extremes	8			
I_S	Supply Current	V_{CM} = 0.3 V		351	400	nA
		Temperature extremes			620	
		V_{CM} = 4.7 V		475	600	
		Temperature extremes			870	

6.10 5-V AC Electrical Characteristics(1)

Unless otherwise specified, all limits for T_A = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$, and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		MIN (2)	TYP (3)	MAX (2)	UNIT
GBW	Gain-Bandwidth Product	C_L = 20 pF, R_L = 100 kΩ			6.2		kHz
SR	Slew Rate	A_V = +1, V_{IN} = 0 V to 5 V	Falling Edge	1.1	2.7		V/ms
			Temperature extremes	1.2			
			Rising Edge	1.1	2.4		
			Temperature extremes	1.2			
θ_m	Phase Margin	C_L = 20 pF, R_L = 100 kΩ			73		deg
G_m	Gain Margin	C_L = 20 pF, R_L = 100 kΩ			20		dB
e_n	Input-Referred Voltage Noise Density	f = 100 Hz			255		nV/√Hz
	Input-Referred Voltage Noise	0.1 Hz to 10 Hz			22		μV_{PP}
I_n	Input-Referred Current Noise	f = 100 Hz			100		fA/√Hz
EMIRR	EMI Rejection Ratio, IN+ and IN−(4)	V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 400 MHz			121		dB
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 900 MHz			121		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 1800 MHz			124		
		V_{RF_PEAK} = 100 mV_P (−20 dB_P), f = 2400 MHz			142		

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that TJ = TA. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where TJ TA. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are guaranteed by testing, statistical analysis or design.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.
(4) The EMI Rejection Ratio is defined as EMIRR = 20log (VRF_PEAK/ΔVOS).

6.11 Typical Characteristics

At T_J = 25°C, unless otherwise specified.

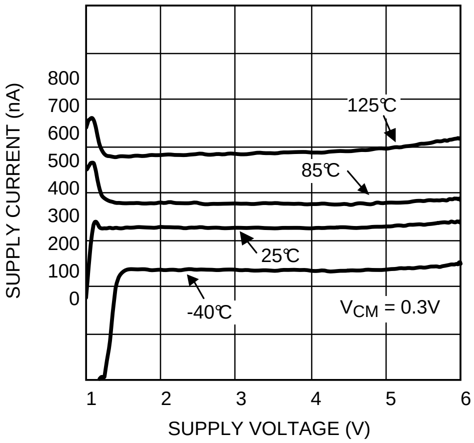


Figure 1. Supply Current vs. Supply Voltage

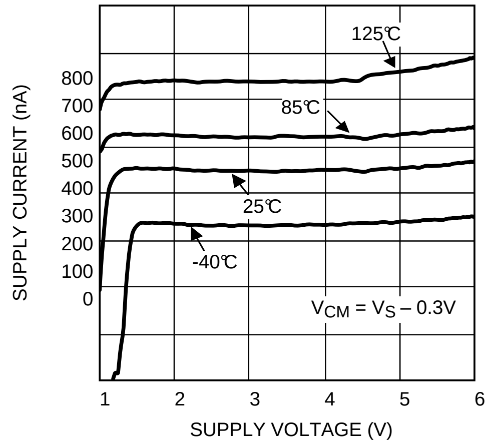


Figure 2. Supply Current vs. Supply Voltage

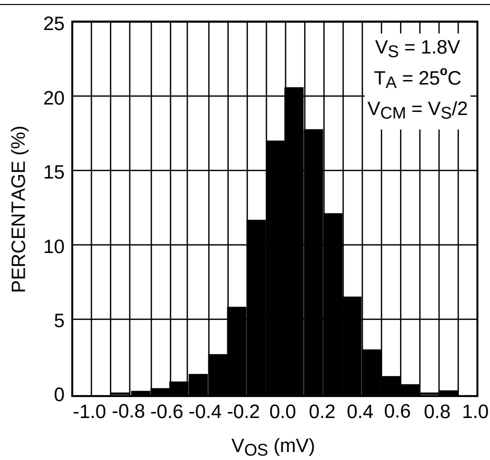


Figure 3. Offset Voltage Distribution

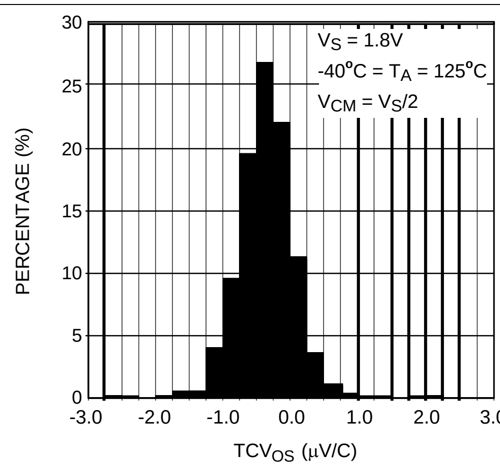


Figure 4. Tcv_{OS} Distribution

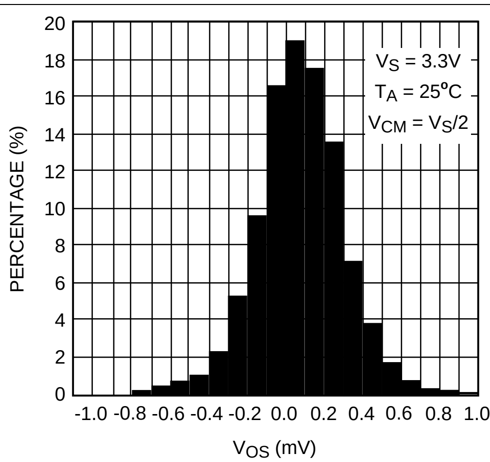


Figure 5. Offset Voltage Distribution

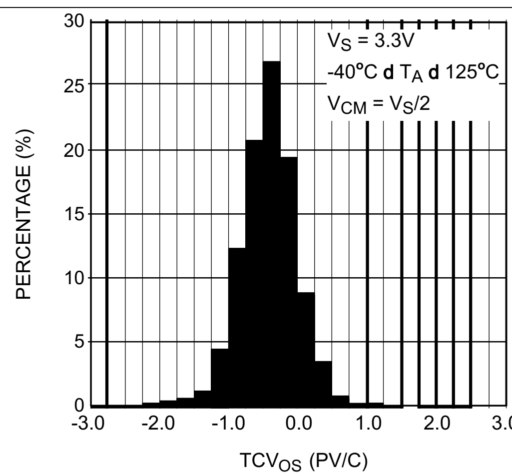


Figure 6. Tcv_{OS} Distribution

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

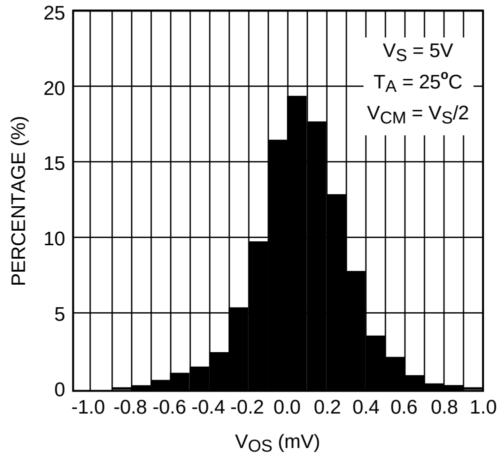


Figure 7. Offset Voltage Distribution

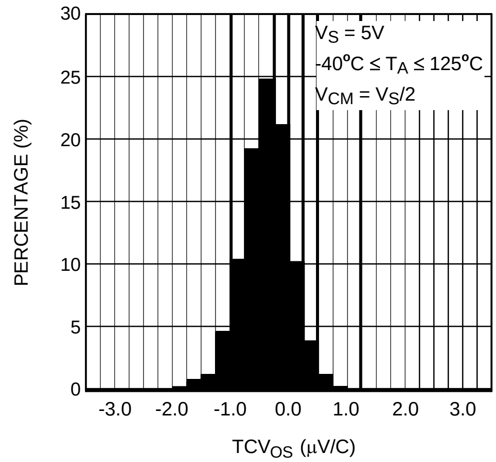


Figure 8. Tcv_{OS} Distribution

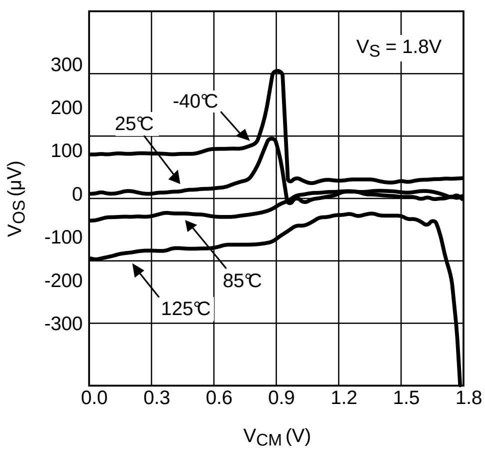


Figure 9. Input Offset Voltage vs. Input Common Mode

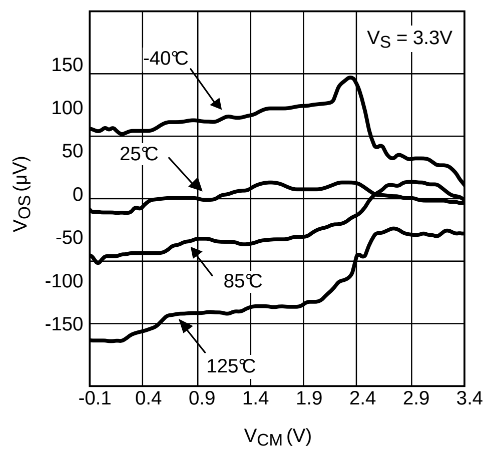


Figure 10. Input Offset Voltage vs. Input Common Mode

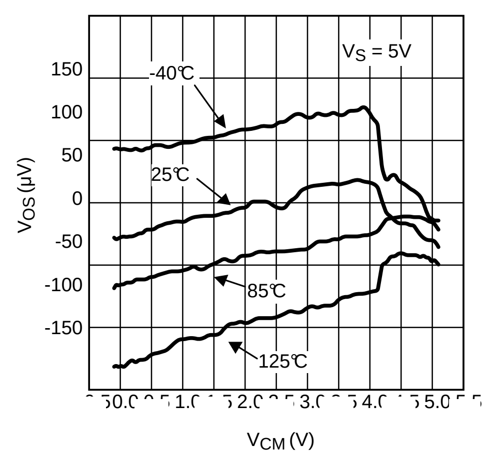


Figure 11. Input Offset Voltage vs. Input Common Mode

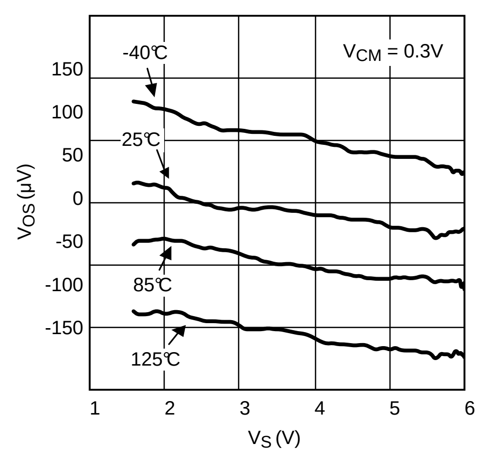


Figure 12. Input Offset Voltage vs. Supply Voltage

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

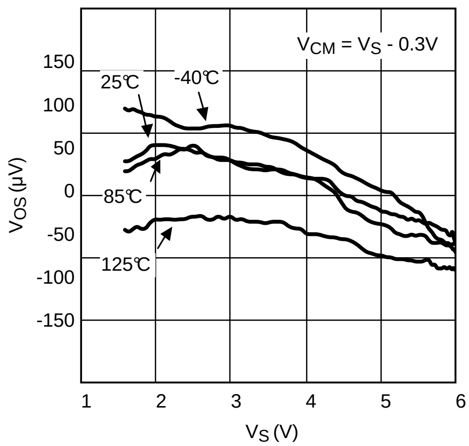


Figure 13. Input Offset Voltage vs. Supply Voltage

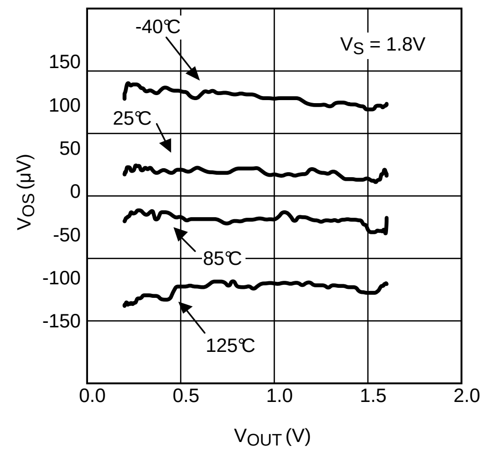


Figure 14. Input Offset Voltage vs. Output Voltage

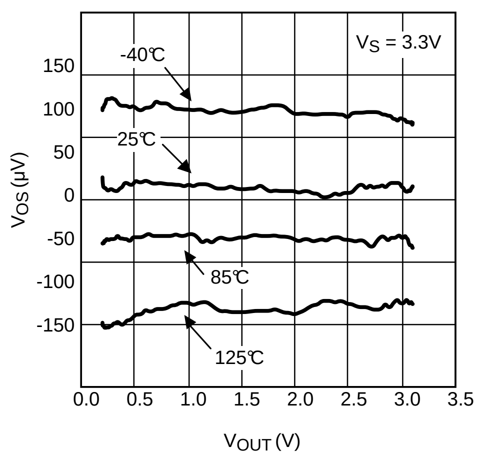


Figure 15. Input Offset Voltage vs. Output Voltage

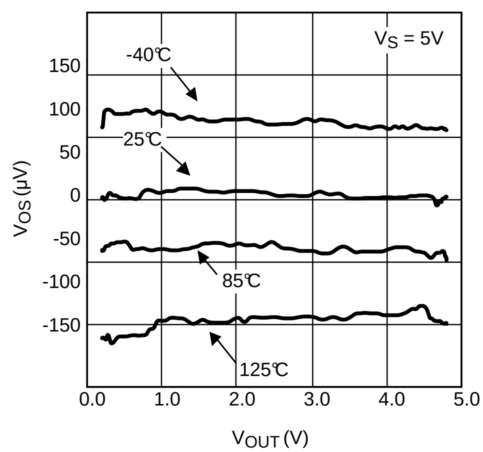


Figure 16. Input Offset Voltage vs. Output Voltage

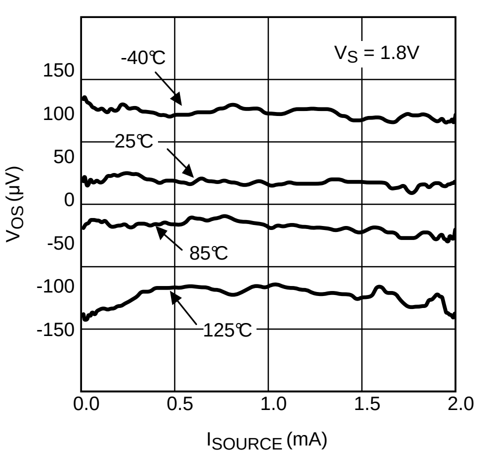


Figure 17. Input Offset Voltage vs. Sourcing Current

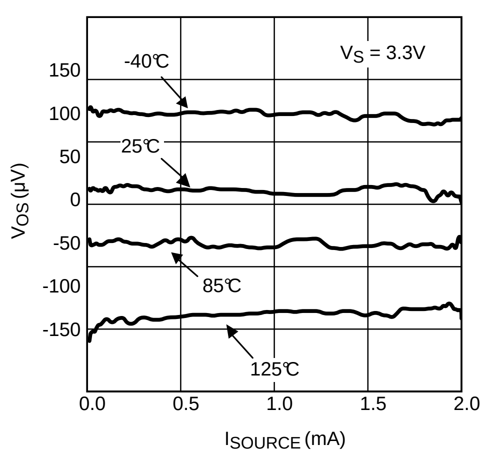


Figure 18. Input Offset Voltage vs. Sourcing Current

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

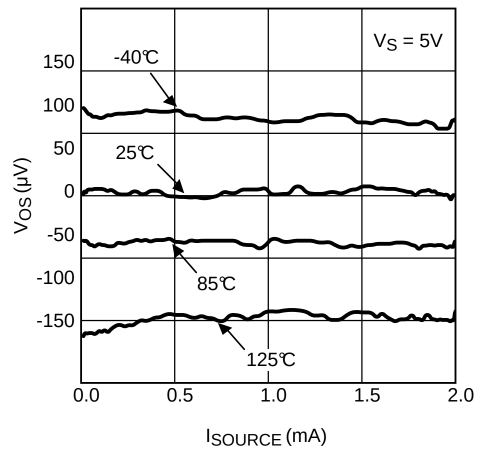


Figure 19. Input Offset Voltage vs. Sourcing Current

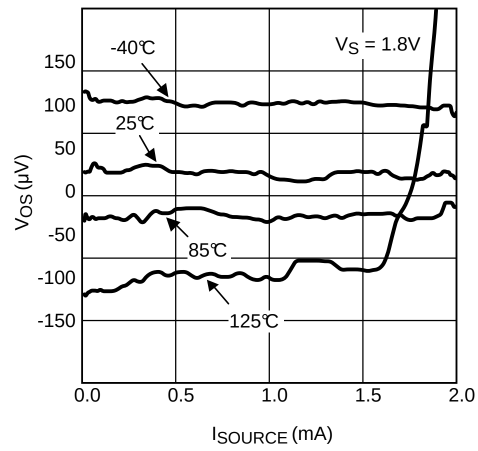


Figure 20. Input Offset Voltage vs. Sinking Current

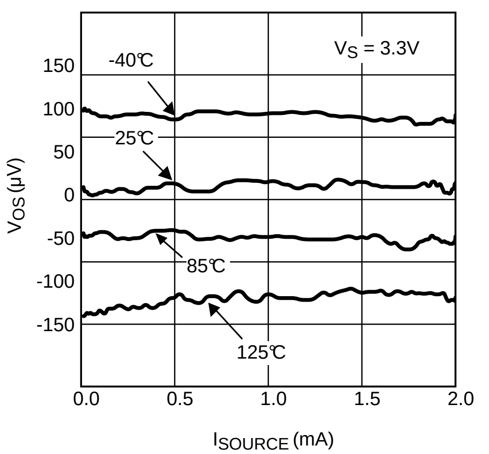


Figure 21. Input Offset Voltage vs. Sinking Current

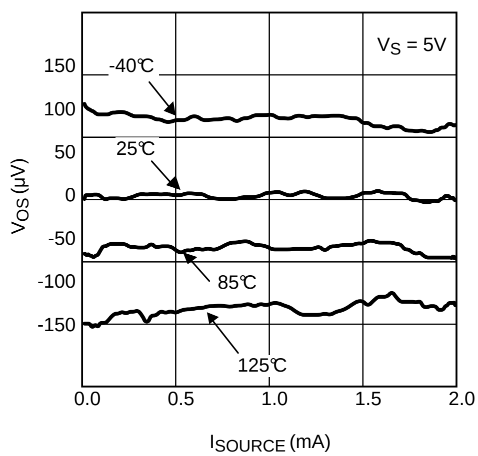


Figure 22. Input Offset Voltage vs. Sinking Current

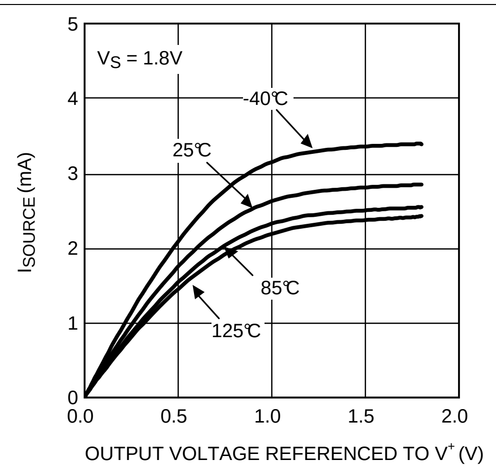


Figure 23. Sourcing Current vs. Output Voltage

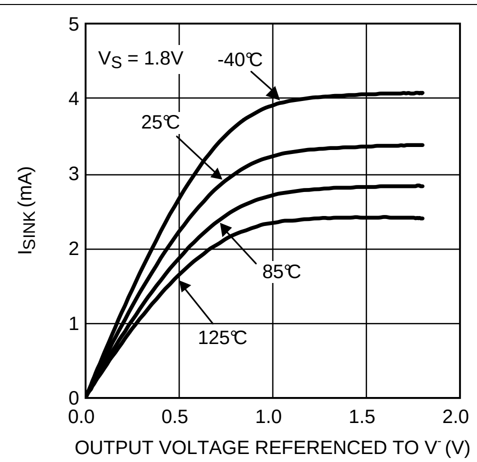


Figure 24. Sinking Current vs. Output Voltage

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

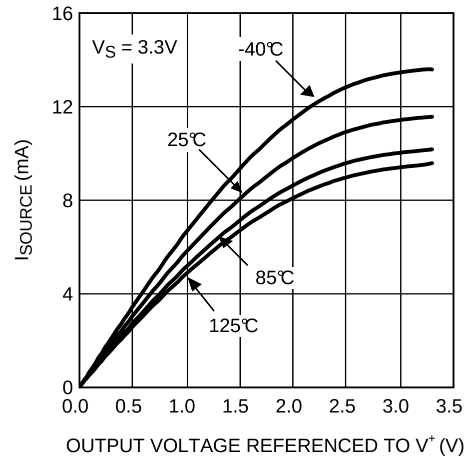


Figure 25. Sourcing Current vs. Output Voltage

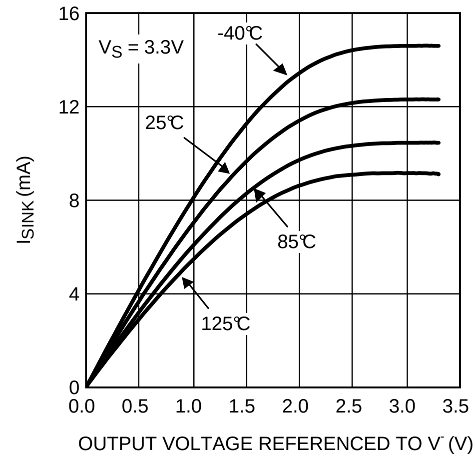


Figure 26. Sinking Current vs. Output Voltage

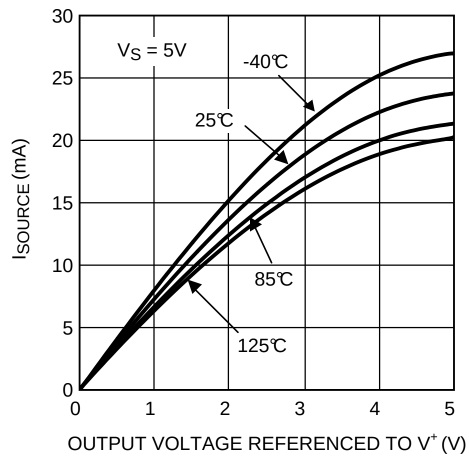


Figure 27. Sourcing Current vs. Output Voltage

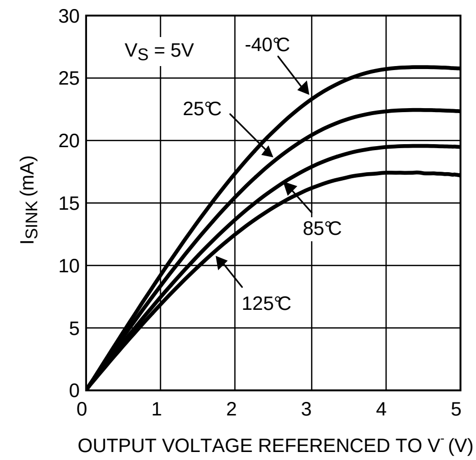


Figure 28. Sinking Current vs. Output Voltage

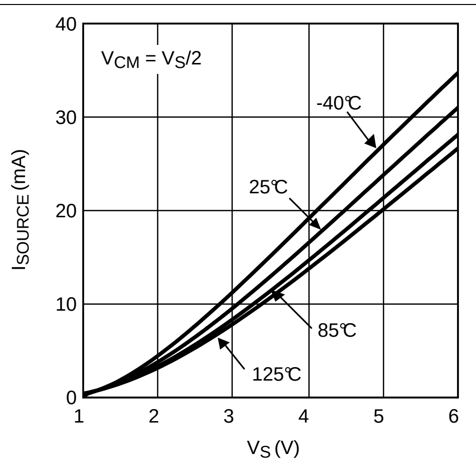


Figure 29. Sourcing Current vs. Supply Voltage

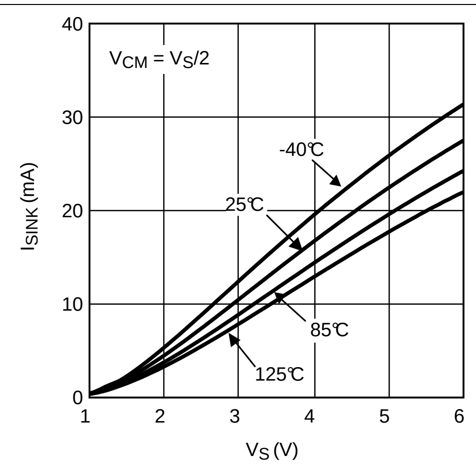


Figure 30. Sinking Current vs. Supply Voltage

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

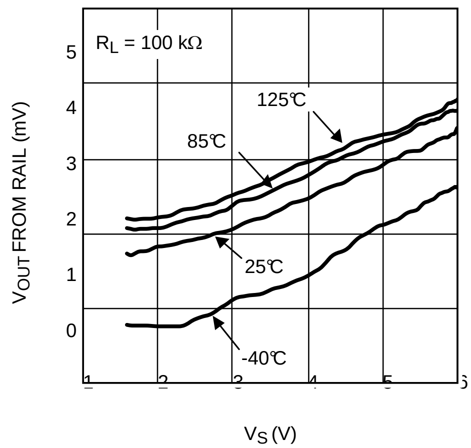


Figure 31. Output Swing High vs. Supply Voltage

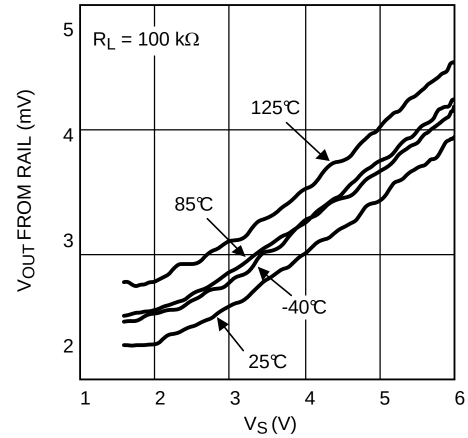


Figure 32. Output Swing Low vs. Supply Voltage

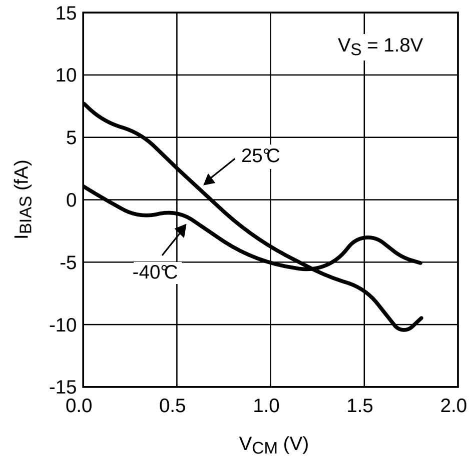


Figure 33. Input Bias Current vs. Common Mode Voltage

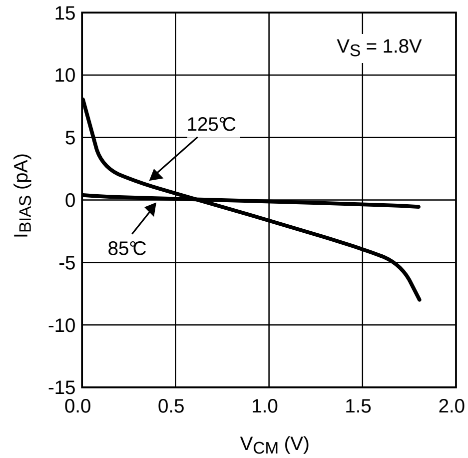


Figure 34. Input Bias Current vs. Common Mode Voltage

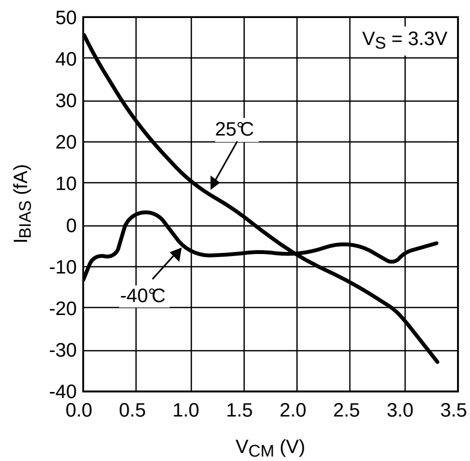


Figure 35. Input Bias Current vs. Common Mode Voltage

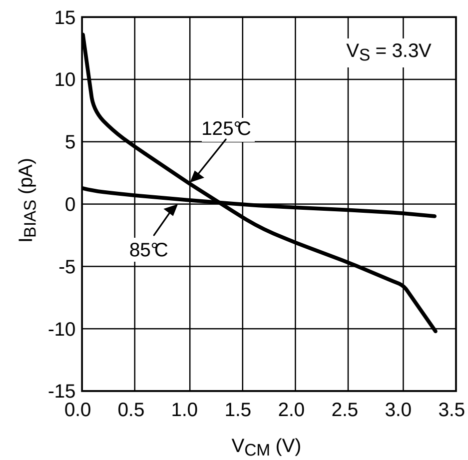


Figure 36. Input Bias Current vs. Common Mode Voltage

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

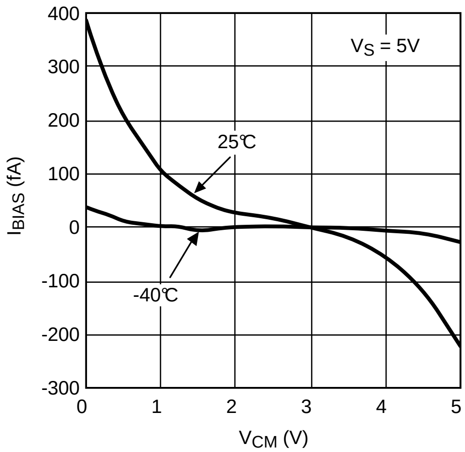


Figure 37. Input Bias Current vs. Common Mode Voltage

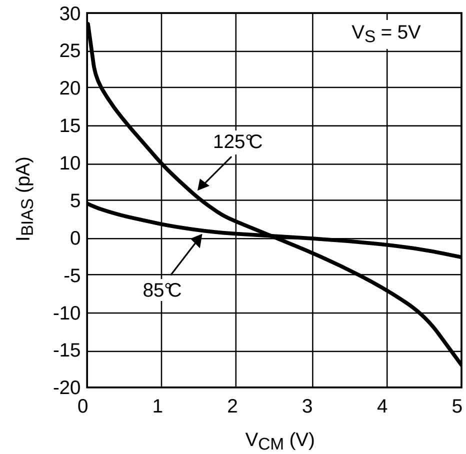


Figure 38. Input Bias Current vs. Common Mode Voltage

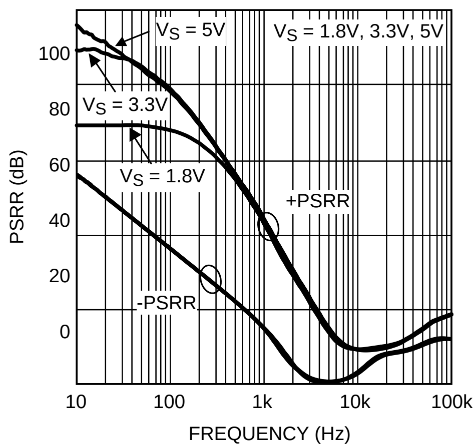


Figure 39. PSRR vs. Frequency

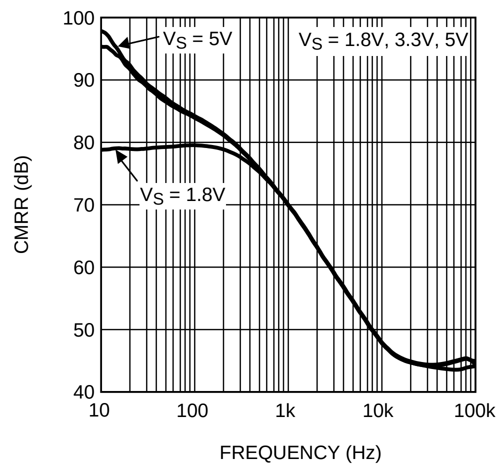


Figure 40. CMRR vs. Frequency

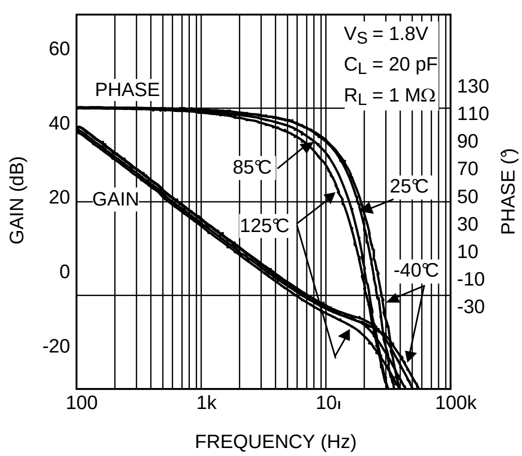


Figure 41. Frequency Response vs. Temperature

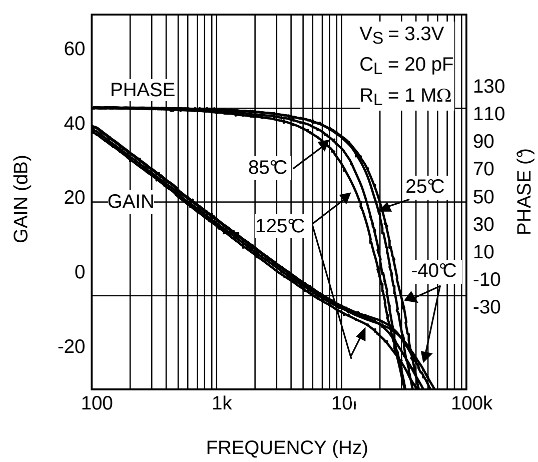


Figure 42. Frequency Response vs. Temperature

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

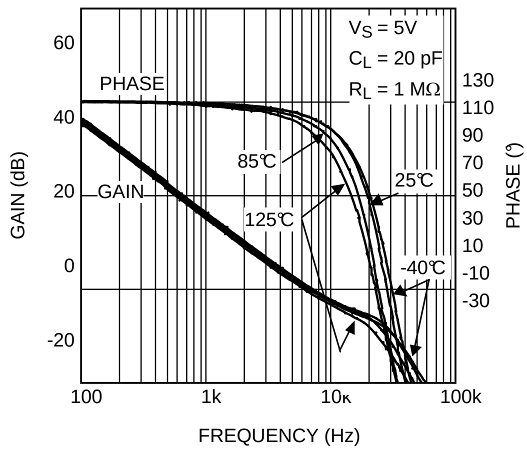


Figure 43. Frequency Response vs. Temperature

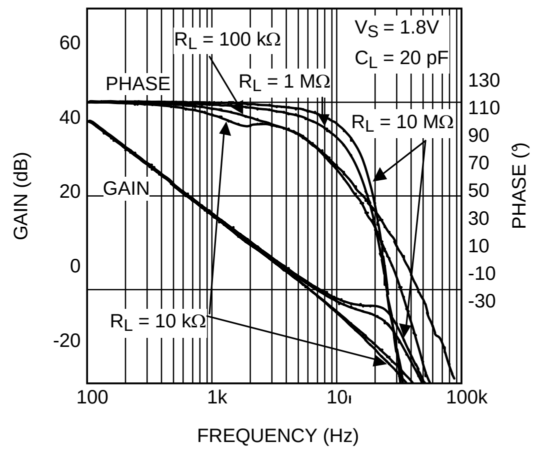


Figure 44. Frequency Response vs. R_L

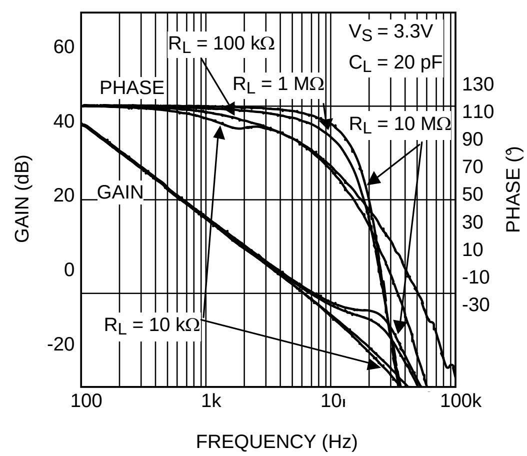


Figure 45. Frequency Response vs. R_L

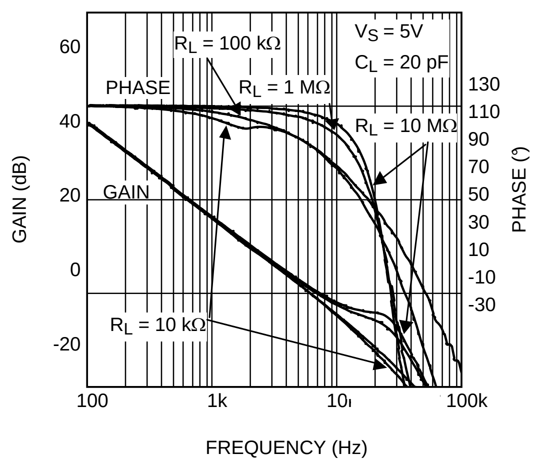


Figure 46. Frequency Response vs. R_L

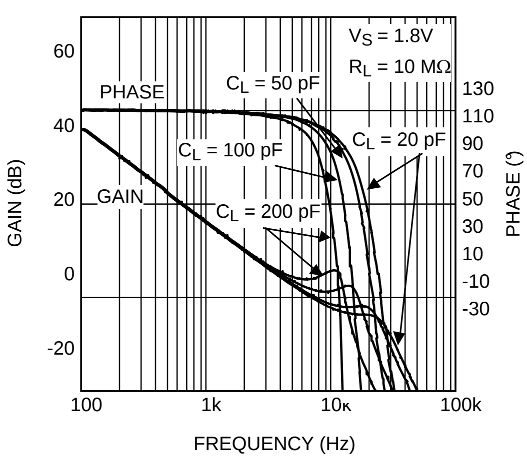


Figure 47. Frequency Response vs. C_L

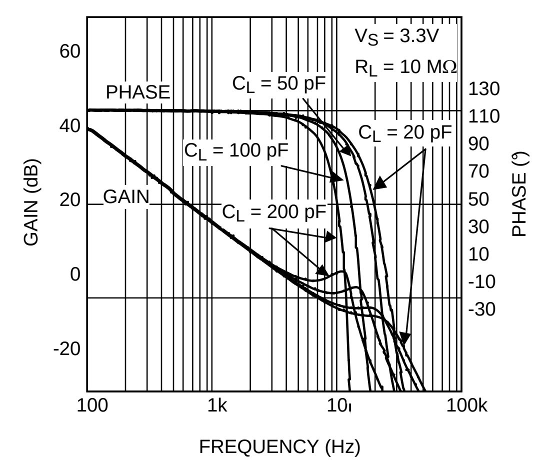


Figure 48. Frequency Response vs. C_L

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

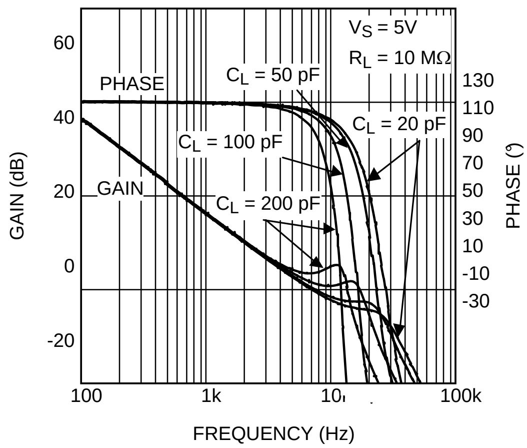


Figure 49. Frequency Response vs. C_L

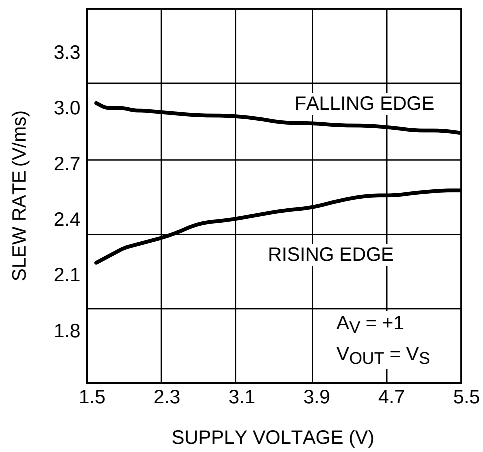


Figure 50. Slew Rate vs. Supply Voltage

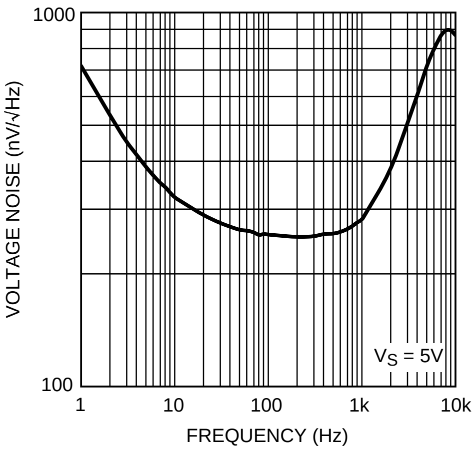


Figure 51. Voltage Noise vs. Frequency

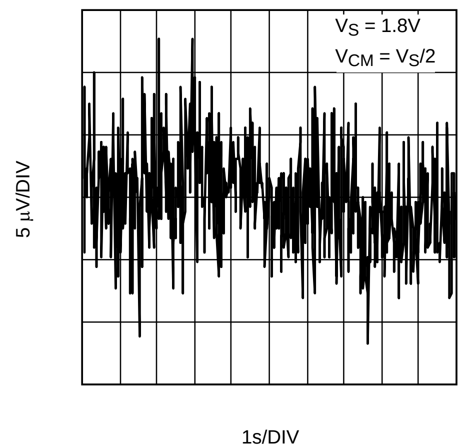


Figure 52. 0.1 to 10 Hz Time Domain Voltage Noise

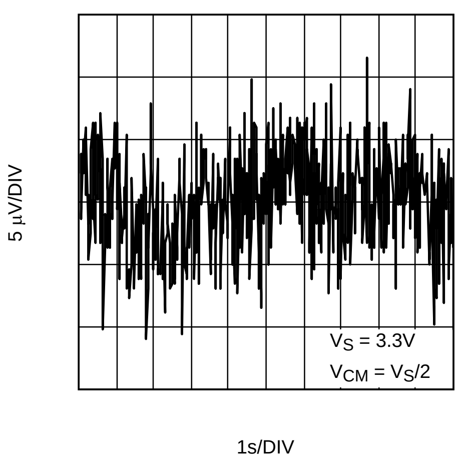


Figure 53. 0.1 to 10 Hz Time Domain Voltage Noise

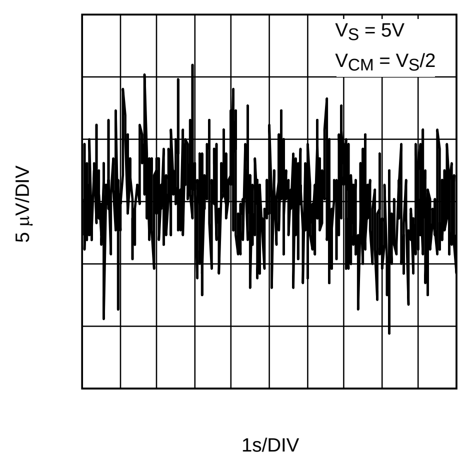


Figure 54. 0.1 to 10 Hz Time Domain Voltage Noise

Typical Characteristics (continued)

At T_J = 25°C, unless otherwise specified.

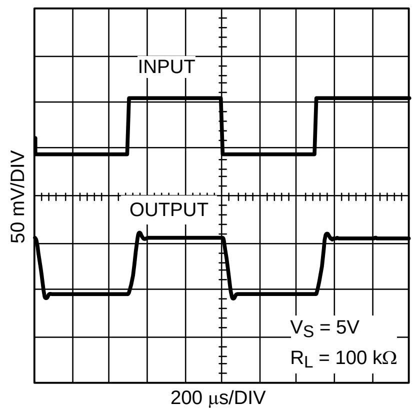


Figure 55. Small Signal Pulse Response

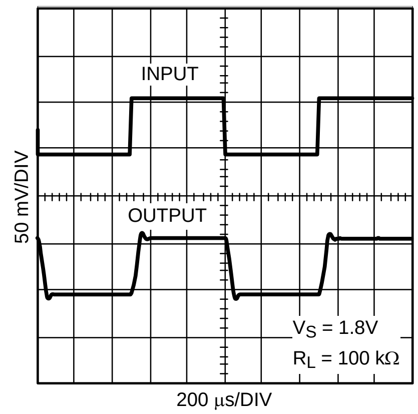


Figure 56. Small Signal Pulse Response

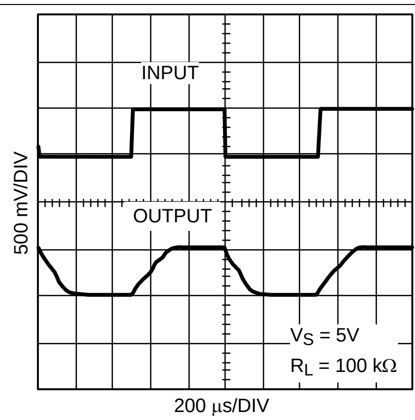


Figure 57. Large Signal Pulse Response

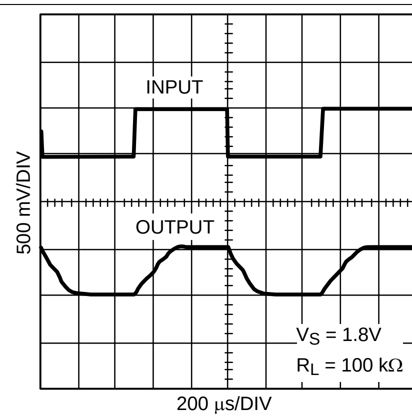


Figure 58. Large Signal Pulse Response

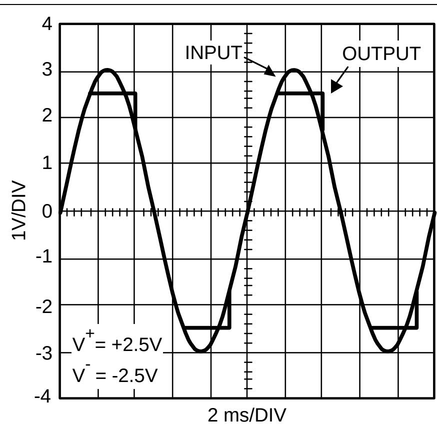


Figure 59. Overload Recovery Waveform

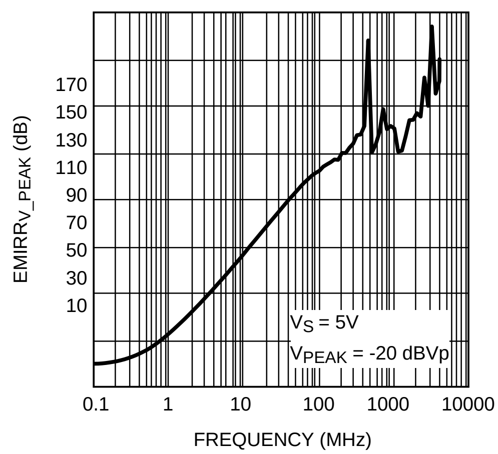


Figure 60. EMIRR vs. Frequency

7 Detailed Description

7.1 Overview

The LPV521 is fabricated with Texas Instruments' state-of-the-art VIP50 process. This proprietary process dramatically improves the performance of Texas Instruments' low-power and low-voltage operational amplifiers. The following sections showcase the advantages of the VIP50 process and highlight circuits which enable ultra-low power consumption.

7.2 Functional Block Diagram

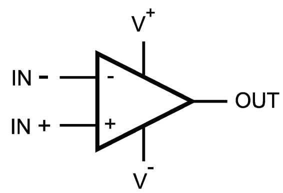


Figure 61. Block Diagram

7.3 Feature Description

The amplifier's differential inputs consist of a noninverting input (+IN) and an inverting input (–IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp Vout is given by Equation 1:

$$V_{OUT} = A_{OL} (IN^+ - IN^-) \tag{1}$$

where A_{OL} is the open-loop gain of the amplifier, typically around 100 dB (100,000x, or 10uV per Volt).

7.4 Device Functional Modes

7.4.1 Input Stage

The LPV521 has a rail-to-rail input which provides more flexibility for the system designer. Rail-to-rail input is achieved by using in parallel, one PMOS differential pair and one NMOS differential pair. When the common mode input voltage (V_{CM}) is near V+, the NMOS pair is on and the PMOS pair is off. When V_{CM} is near V−, the NMOS pair is off and the PMOS pair is on. When V_{CM} is between V+ and V−, internal logic decides how much current each differential pair will get. This special logic ensures stable and low distortion amplifier operation within the entire common mode voltage range.

Because both input stages have their own offset voltage (V_{OS}) characteristic, the offset voltage of the LPV521 becomes a function of V_{CM}. V_{OS} has a crossover point at 1.0 V below V+. Refer to the 'V_{OS} vs. V_{CM}' curve in the Typical Performance Characteristics section. Caution should be taken in situations where the input signal amplitude is comparable to the V_{OS} value and/or the design requires high accuracy. In these situations, it is necessary for the input signal to avoid the crossover point. In addition, parameters such as PSRR and CMRR which involve the input offset voltage will also be affected by changes in V_{CM} across the differential pair transition region.

7.4.2 Output Stage

The LPV521 output voltage swings 3 mV from rails at 3.3-V supply, which provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The LPV521 Maximum Output Voltage Swing defines the maximum swing possible under a particular output load. The LPV521 output swings 50 mV from the rail at 5-V supply with an output load of 100 kΩ.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LPV521is specified for operation from 1.6 V to 5.5 V (±0.8 V to ±2.25 V). Many of the specifications apply from –40°C to 125°C. The LMV521 features rail to rail input and rail-to-rail output swings while consuming only nanowatts of power. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

8.1.1 Driving Capacitive Load

The LPV521 is internally compensated for stable unity gain operation, with a 6.2-kHz, typical gain bandwidth. However, the unity gain follower is the most sensitive configuration to capacitive load. The combination of a capacitive load placed at the output of an amplifier along with the amplifier's output impedance creates a phase lag, which reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be under damped which causes peaking in the transfer and, when there is too much peaking, the op amp might start oscillating.

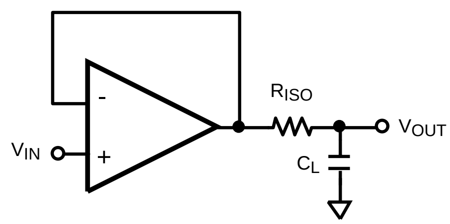


Figure 62. Resistive Isolation of Capacitive Load

In order to drive heavy capacitive loads, an isolation resistor, R_{ISO}, should be used, as shown in Figure 62. By using this isolation resistor, the capacitive load is isolated from the amplifier's output. The larger the value of R_{ISO}, the more stable the amplifier will be. If the value of R_{ISO} is sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

Recommended minimum values for R_{ISO} are given in the following table, for 5-V supply. Figure 63 shows the typical response obtained with the C_L = 50 pF and R_{ISO} = 154 kΩ. The other values of R_{ISO} in the table were chosen to achieve similar dampening at their respective capacitive loads. Notice that for the LPV521 with larger C_L a smaller R_{ISO} can be used for stability. However, for a given C_L a larger R_{ISO} will provide a more damped response. For capacitive loads of 20 pF and below no isolation resistor is needed.

C_L	R_{ISO}
0 – 20 pF	not needed
50 pF	154 kΩ
100 pF	118 kΩ
500 pF	52.3 kΩ
1 nF	33.2 kΩ
5 nF	17.4 kΩ
10 nF	13.3 kΩ

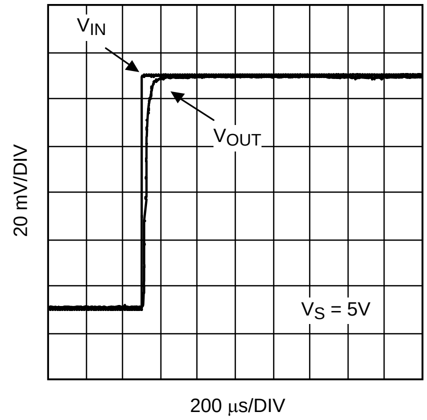


Figure 63. Step Response

8.1.2 EMI Suppression

The near-ubiquity of cellular, Bluetooth, and Wi-Fi signals and the rapid rise of sensing systems incorporating wireless radios make electromagnetic interference (EMI) an evermore important design consideration for precision signal paths. Though RF signals lie outside the op amp band, RF carrier switching can modulate the DC offset of the op amp. Also some common RF modulation schemes can induce down-converted components. The added DC offset and the induced signals are amplified with the signal of interest and thus corrupt the measurement. The LPV521 uses on chip filters to reject these unwanted RF signals at the inputs and power supply pins; thereby preserving the integrity of the precision signal path.

Twisted pair cabling and the active front-end's common-mode rejection provide immunity against low-frequency noise (i.e. 60-Hz or 50-Hz mains) but are ineffective against RF interference. Even a few centimeters of PCB trace and wiring for sensors located close to the amplifier can pick up significant 1 GHz RF. The integrated EMI filters of the LPV521 reduce or eliminate external shielding and filtering requirements, thereby increasing system robustness. A larger EMIRR means more rejection of the RF interference. For more information on EMIRR, please refer to AN-1698.

8.2 Typical Applications

8.2.1 60-Hz Twin T-Notch Filter

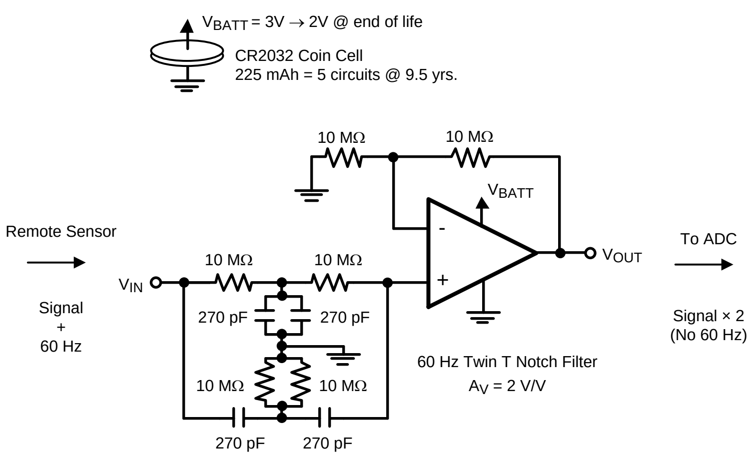


Figure 64. 60-Hz Notch Filter

Typical Applications (continued)

8.2.1.1 Design Requirements

Small signals from transducers in remote and distributed sensing applications commonly suffer strong 60-Hz interference from AC power lines. The circuit of Figure 64 notches out the 60 Hz and provides a gain A_V = 2 for the sensor signal represented by a 1-kHz sine wave. Similar stages may be cascaded to remove 2nd and 3rd harmonics of 60 Hz. Thanks to the nA power consumption of the LPV521, even 5 such circuits can run for 9.5 years from a small CR2032 lithium cell. These batteries have a nominal voltage of 3 V and an end of life voltage of 2 V. With an operating voltage from 1.6 V to 5.5 V the LPV521 can function over this voltage range.

8.2.1.2 Detailed Design Procedure

The notch frequency is set by $F_0 = 1 / 2\pi RC$. To achieve a 60-Hz notch use R = 10 MΩ and C = 270 pF. If eliminating 50-Hz noise, which is common in European systems, use R = 11.8 MΩ and C = 270 pF.

The Twin T Notch Filter works by having two separate paths from V_{IN} to the amplifier's input. A low frequency path through the resistors R - R and another separate high frequency path through the capacitors C - C. However, at frequencies around the notch frequency, the two paths have opposing phase angles and the two signals will tend to cancel at the amplifier's input.

To ensure that the target center frequency is achieved and to maximize the notch depth (Q factor) the filter needs to be as balanced as possible. To obtain circuit balance, while overcoming limitations of available standard resistor and capacitor values, use passives in parallel to achieve the 2C and R/2 circuit requirements for the filter components that connect to ground.

To make sure passive component values stay as expected clean board with alcohol, rinse with deionized water, and air dry. Make sure board remains in a relatively low humidity environment to minimize moisture which may increase the conductivity of board components. Also large resistors come with considerable parasitic stray capacitance which effects can be reduced by cutting out the ground plane below components of concern.

Large resistors are used in the feedback network to minimize battery drain. When designing with large resistors, resistor thermal noise, op amp current noise, as well as op amp voltage noise, must be considered in the noise analysis of the circuit. The noise analysis for the circuit in Figure 64 can be done over a bandwidth of 5 kHz, which takes the conservative approach of overestimating the bandwidth (LPV521 typical GBW/A_V is lower). The total noise at the output is approximately 800 µVpp, which is excellent considering the total consumption of the circuit is only 540 nA. The dominant noise terms are op amp voltage noise (550 µVpp), current noise through the feedback network (430 µVpp), and current noise through the notch filter network (280 µVpp). Thus the total circuit's noise is below ½ LSB of a 10 bit system with a 2-V reference, which is 1 mV.

8.2.1.3 Application Curve

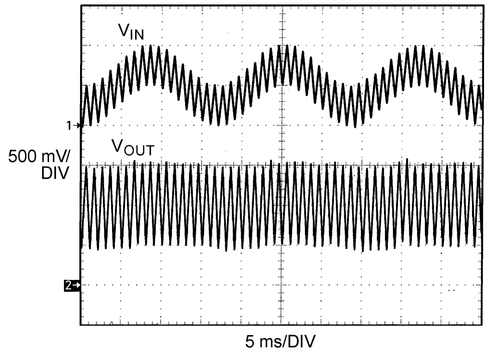


Figure 65. 60-Hz Notch Filter Waveform

Typical Applications (continued)

8.2.2 Portable Gas Detection Sensor

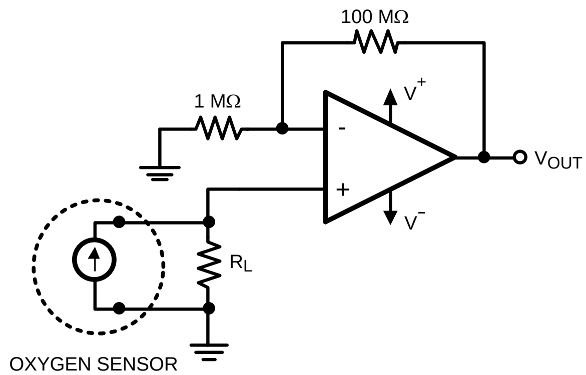


Figure 66. Precision Oxygen Sensor

8.2.2.1 Design Requirements

Gas sensors are used in many different industrial and medical applications. They generate a current which is proportional to the percentage of a particular gas sensed in an air sample. This current goes through a load resistor and the resulting voltage drop is measured. The LPV521 makes an excellent choice for this application as it only draws 345 nA of current and operates on supply voltages down to 1.6V. Depending on the sensed gas and sensitivity of the sensor, the output current can be in the order of tens of microamperes to a few milliamperes. Gas sensor datasheets often specify a recommended load resistor value or they suggest a range of load resistors to choose from.

Oxygen sensors are used when air quality or oxygen delivered to a patient needs to be monitored. Fresh air contains 20.9% oxygen. Air samples containing less than 18% oxygen are considered dangerous. This application detects oxygen in air. Oxygen sensors are also used in industrial applications where the environment must lack oxygen. An example is when food is vacuum packed. There are two main categories of oxygen sensors, those which sense oxygen when it is abundantly present (i.e. in air or near an oxygen tank) and those which detect traces of oxygen in ppm.

8.2.2.2 Detailed Design Procedure

Figure 66 shows a typical circuit used to amplify the output of an oxygen detector. The oxygen sensor outputs a known current through the load resistor. This value changes with the amount of oxygen present in the air sample. Oxygen sensors usually recommend a particular load resistor value or specify a range of acceptable values for the load resistor. The use of the nanopower LPV521 means minimal power usage by the op amp and it enhances the battery life. With the components shown in Figure 66 the circuit can consume less than 0.5 µA of current ensuring that even batteries used in compact portable electronics, with low mAh charge ratings, could last beyond the life of the oxygen sensor. The precision specifications of the LPV521, such as its very low offset voltage, low TCV_{OS} , low input bias current, high CMRR, and high PSRR are other factors which make the LPV521 a great choice for this application.

Typical Applications (continued)

8.2.2.3 Application Curve

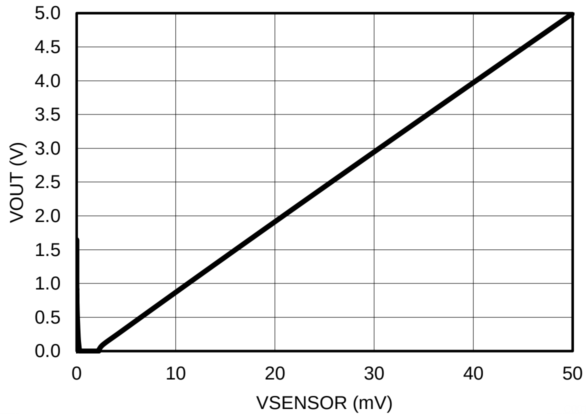


Figure 67. Calculated Oxygen Sensor Circuit Output (Single 5V Supply)

8.2.3 High-Side Battery Current Sensing

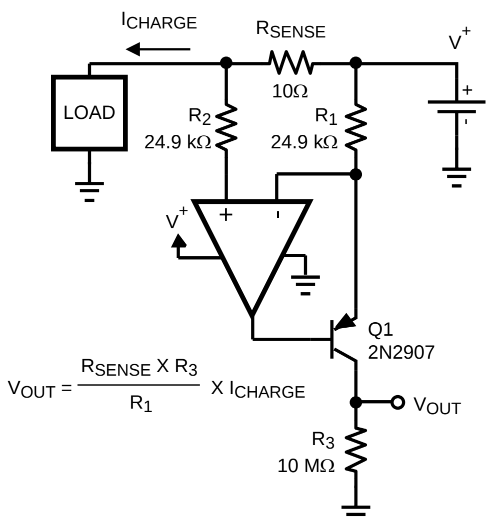


Figure 68. High-Side Current Sensing

8.2.3.1 Design Requirements

The rail-to-rail common mode input range and the very low quiescent current make the LPV521 ideal to use in high-side and low-side battery current sensing applications. The high-side current sensing circuit in Figure 68 is commonly used in a battery charger to monitor the charging current in order to prevent over charging. A sense resistor R_{SENSE} is connected in series with the battery.

8.2.3.2 Detailed Design Procedure

The theoretical output voltage of the circuit is V_{OUT} = [®$_{SENSE}$ × R_3) / R_1] × I_{CHARGE}. In reality, however, due to the finite Current Gain, β, of the transistor the current that travels through R_3 will not be I_{CHARGE}, but instead, will be α × I_{CHARGE} or β/(β+1) × I_{CHARGE}. A Darlington pair can be used to increase the β and performance of the measuring circuit.

Using the components shown in Figure 68 will result in V_{OUT} ≈ 4000 Ω × I_{CHARGE}. This is ideal to amplify a 1 mA I_{CHARGE} to near full scale of an ADC with V_{REF} at 4.1 V. A resistor, R2 is used at the noninverting input of the amplifier, with the same value as R1 to minimize offset voltage.

Typical Applications (continued)

Selecting values per Figure 68 will limit the current traveling through the R_1 – Q1 – R_3 leg of the circuit to under 1 µA which is on the same order as the LPV521 supply current. Increasing resistors R_1 , R_2 , and R_3 will decrease the measuring circuit supply current and extend battery life.

Decreasing R_{SENSE} will minimize error due to resistor tolerance, however, this will also decrease V_{SENSE} = $I_{CHARGE} \times R_{SENSE}$, and in turn the amplifier offset voltage will have a more significant contribution to the total error of the circuit. With the components shown in Figure 68 the measurement circuit supply current can be kept below 1.5 µA and measure 100 µA to 1 mA.

8.2.3.3 Application Curve

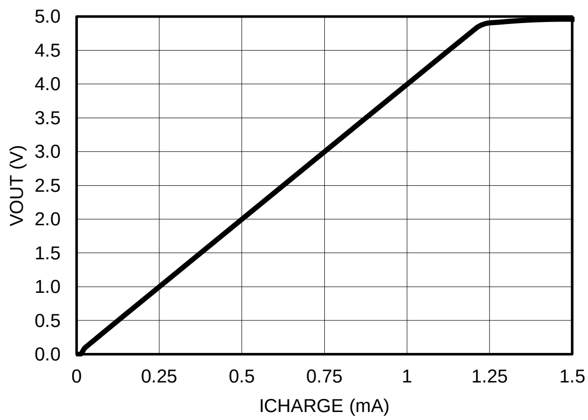


Figure 69. Calculated High-Side Current Sense Circuit Output

9 Power Supply Recommendations

The LPV521 is specified for operation from 1.6 V to 5.5 V (±0.8 V to ±2.75 V) over a –40°C to 125°C temperature range. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device.

Low bandwidth nanopower devices do not have good high frequency (>1KHz) AC PSRR rejection against high-frequency switching supplies and other kHz and above noise sources, so extra supply filtering is recommended if kHz range noise is expected on the power supply lines.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for singlesupply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Layout Example*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

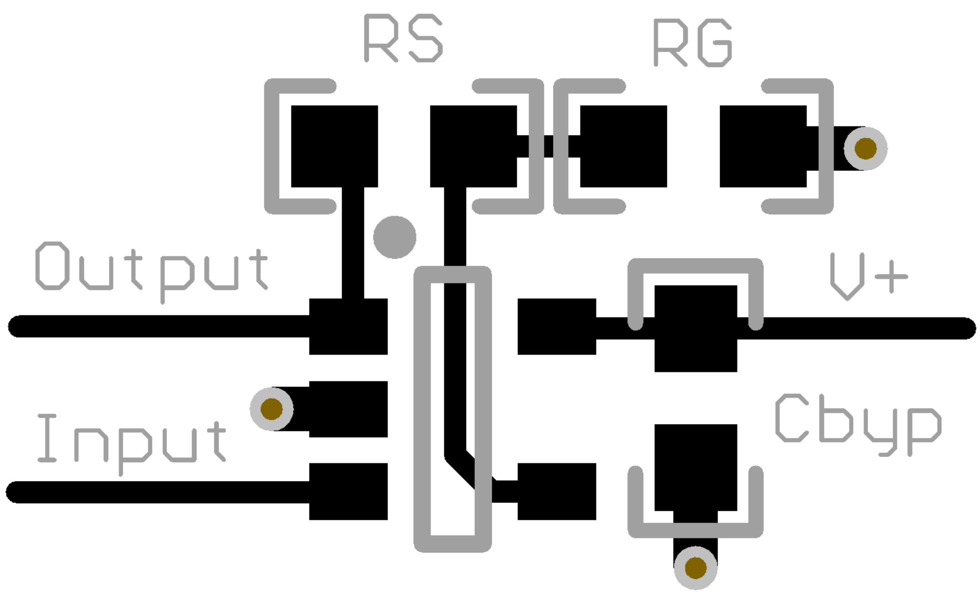


Figure 70. Noninverting Layout Example

- Feedback Plots Define Op Amp AC Performance, SBOA015 (AB-028)
- Circuit Board Layout Techniques, SLOA089
- Op Amps for Everyone, SLOD006
- AN-1698 A Specification for EMI Hardened Operational Amplifiers, SNOA497
- EMI Rejection Ratio of Operational Amplifiers, SBOA128
- Capacitive Load Drive Solution using an Isolation Resistor, TIPD128
- Handbook of Operational Amplifier Applications, SBOA092

11.3 Trademarks

PowerWise is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

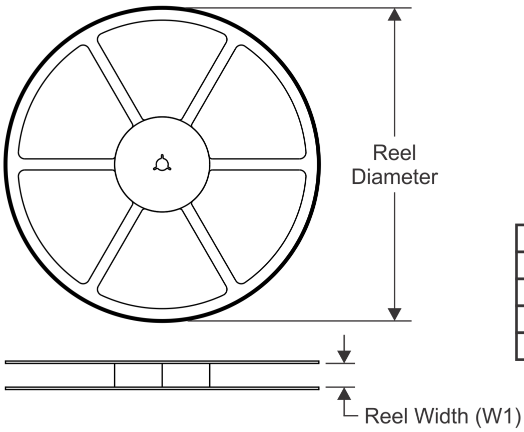
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

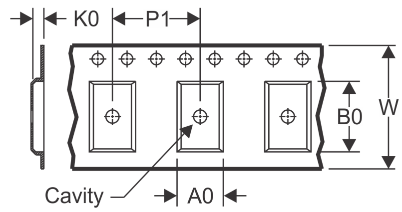
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV521MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AHA	Samples
LPV521MGE/NOPB	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AHA	Samples
LPV521MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AHA	Samples

TAPE AND REEL INFORMATION

REEL DIMENSIONS

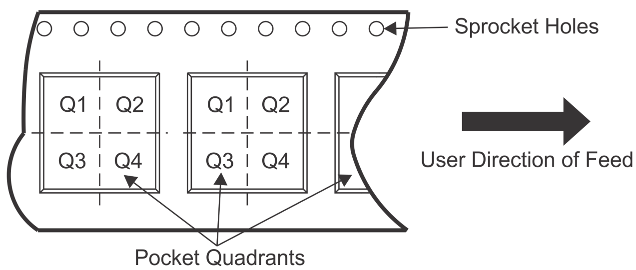


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

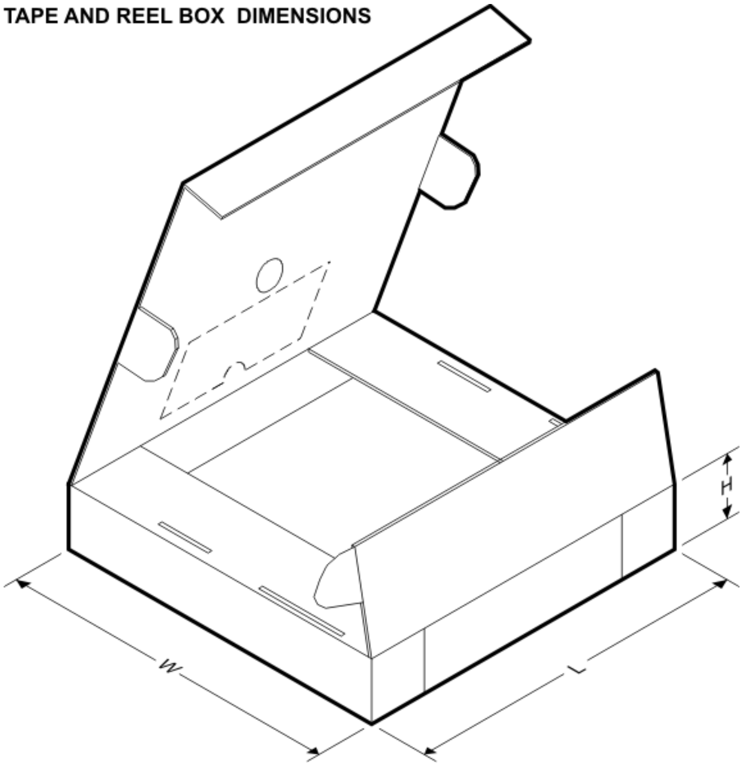
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV521MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV521MGE/NOPB	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LPV521MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

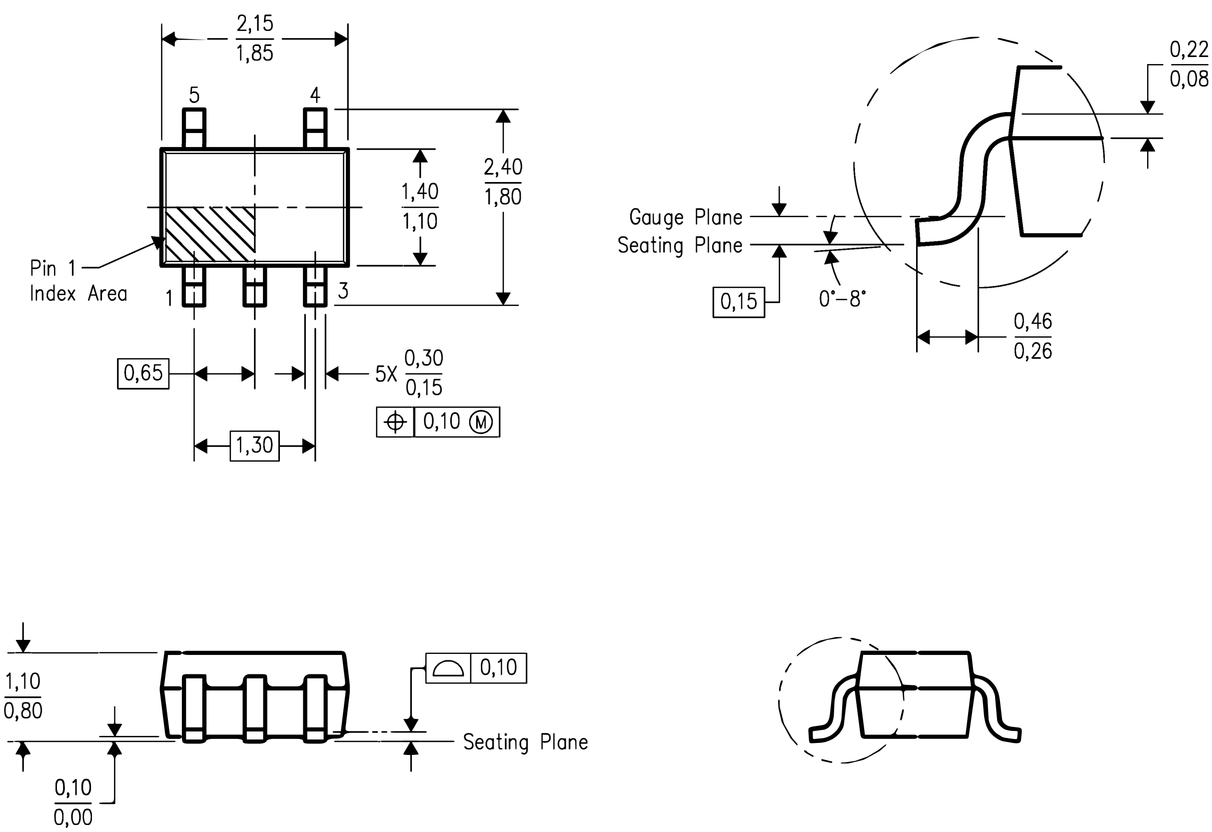
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV521MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LPV521MGE/NOPB	SC70	DCK	5	250	210.0	185.0	35.0
LPV521MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



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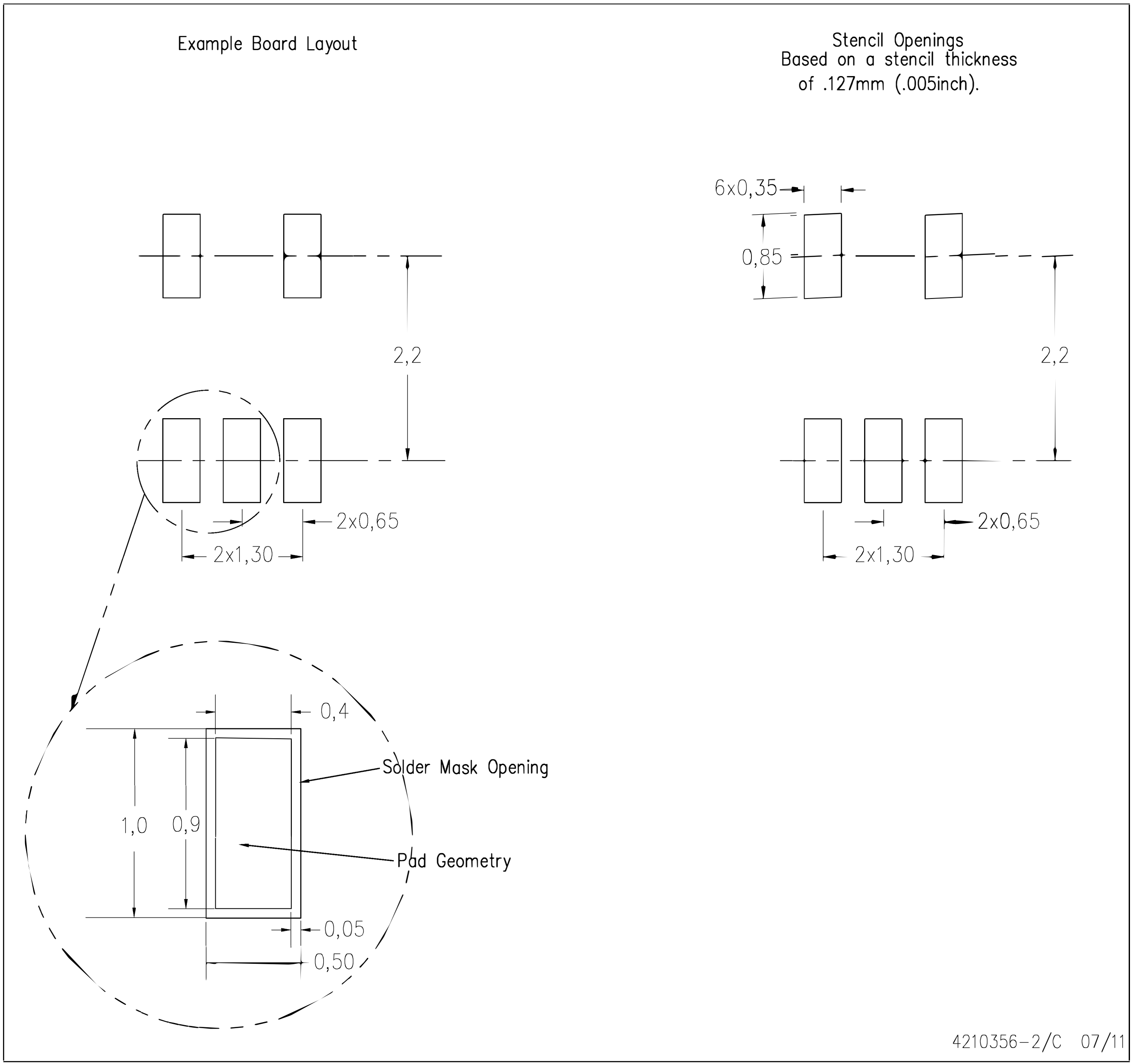
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.