LPV811/LPV812 Precision 425 nA Nanopower Operational Amplifiers

1 Features

- Nanopower Supply Current: 425 nA/channel
- Offset Voltage: 300 µV (max)
- Good TcVos: 1.5 µV/°C
- Gain-Bandwidth: 8 kHz
- Unity-Gain Stable
- Low Input Bias Current : 100 fA
- Wide Supply Range: 1.6 V to 5.5 V
- Rail-to-Rail Output
- No Output Reversals
- EMI Protection
- Temperature Range: –40°C to 125°C
- Industry Standard Packages:
  - Single in 5-pin SOT-23
  - Dual in 8-pin VSSOP

2 Applications

- Gas Detectors such as CO and O2
- Current Sensing
- Motion Detectors using PIR sensors
- Portable Medical Equipment
- Thermostats
- Remote Sensors, IoT
- Active RFID Readers and Tags

3 Description

The LPV811/LPV812 is an ultra-low-power operational amplifier family for “Always ON” sensing applications in wireless and wired equipment. With 8 kHz of bandwidth from 425 nA of quiescent current and less than 300µV of input offset, the LPV811/LPV812 amplifiers provide the required precision while minimizing power consumption in equipment such as gas detectors and portable electronic devices where operational battery-life is critical.

In addition to being ultra-low-power, the LPV811/LPV812 amplifiers have CMOS input stages with fempto-amp bias current which reduces errors commonly introduced in transimpedance amplifier (TIA) configurations with megaohm feedback resistors and high source impedance applications. The LPV811/LPV812 amplifiers also feature a negative-rail sensing input stage and a rail-to-rail output stage that swings within millivolts of the rails, maintaining the widest dynamic range possible. Likewise, EMI protection is designed into the LPV811/LPV812 in order to reduce system sensitivity to unwanted RF signals from mobile phones, WiFi, radio transmitters, and tag readers.

The LPV811/LPV812 amplifiers operate with a single supply voltage as low as 1.6V, ensuring continuous performance in low battery situations over the extended temperature range of -40ºC to 125ºC. The single and dual channel versions are available in industry standard 5-pin SOT-23 and 8-pin VSSOP packages respectively.

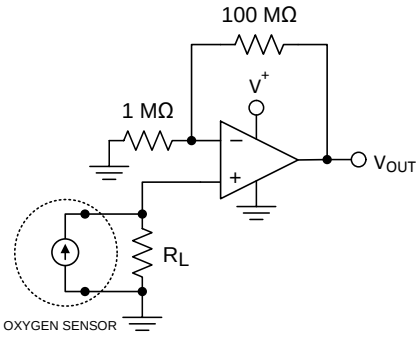
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
LPV811	SOT-23 (5)	2.90 mm x 1.60 mm
LPV812	VSSOP (8)	3.00 mm × 3.00 mm

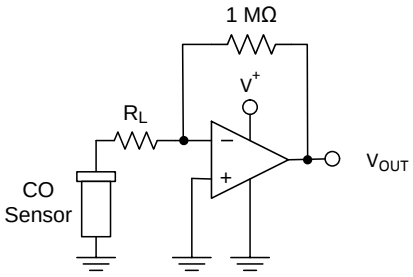
(1) For all available packages, see the orderable addendum at the end of the data sheet.

PRODUCT PREVIEW

Nanopower Oxygen Sensor



Nanopower CO Sensor



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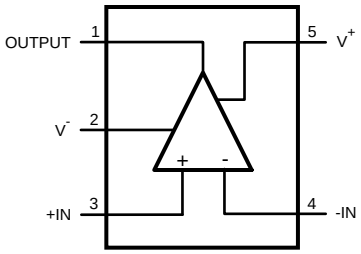
4 Revision History

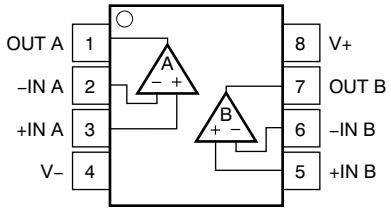
DATE	REVISION	NOTES
August 2016	*	Initial release.

5 Pin Configuration and Functions

LPV811 5-Pin SOT-23
DBV Package
Top View



LPV812 8-Pin VSSOP
DGK Package
Top View



Pin Functions: LPV811 DBV

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
OUT	1	O	Channel A Output
-IN	2	I	Channel A Inverting Input
+IN	3	I	Channel A Non-Inverting Input
V-	4	P	Negative (lowest) power supply
V+	5	P	Positive (highest) power supply

Pin Functions: LPV812 DGK

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
OUT A	1	O	Channel A Output
-IN A	2	I	Channel A Inverting Input
+IN A	3	I	Channel A Non-Inverting Input
V-	4	P	Negative (lowest) power supply
+IN B	5	I	Channel B Non-Inverting Input
-IN B	6	I	Channel B Inverting Input
OUT B	7	O	Channel B Output
V+	8	P	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) - (V-)			–0.3	6	V
Input pins	Voltage (2) (3)	Common mode	(V-) - 0.3	(V+) + 0.3	V
		Differential	(V-) - 0.3	(V+) + 0.3	V
Input pins	Current		-10	10	mA
Output short current (4)			Continuous	Continuous	
Operating temperature			–40	125	°C
Storage temperature, T_{stg}			–65	150	°C
Junction temperature				150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Not to exceed -0.3V or +6.0V on ANY pin, referred to V-
(3) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current-limited to 10 mA or less.
(4) Short-circuit to Vs/2, one amplifer per package. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±750 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage (V+ – V–)	1.6	5.5	V
Specified temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LPV811 DBV (SOT-23) 5 PINS	LPV811 DGK (VSSOP) 5 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	177.4	184.2	ºC/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	133.9	75.3	
θ_{JB}	Junction-to-board thermal resistance	36.3	105.5	
ψ_{JT}	Junction-to-top characterization parameter	23.6	13.5	
ψ_{JB}	Junction-to-board characterization parameter	35.7	103.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, V_S = 1.8 V to 5 V, V_{CM} = V_{OUT} = V_S/2, and R_L≥ 10 MΩ to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 1.8 V and 3.3 V, V_{CM} = V-			±55	±300	µV
$\Delta V_{OS}/\Delta T$	Input offset drift	V_{CM} = V-	T_A = –40°C to 125°C		1.5		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V to 3.3 V, V_{CM} = V-			1.6	60	µV/V
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	V_S = 3.3V		0		2.4	V
CMRR	Common-mode rejection ratio	(V–) ≤ V_{CM} ≤ (V+) – 0.9 V, V_S = 3.3V		80	98		dB
INPUT BIAS CURRENT							
I_B	Input bias current	V_S = 1.8V			100		fA
I_{OS}	Input offset current	V_S = 1.8V			100		fA
INPUT IMPEDANCE							
	Differential				8		pF
	Common mode				3.8		pF
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			25		µVp-p
e_n	Input voltage noise density	f = 100 Hz			340		nV/√Hz
		f = 1 kHz			420		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.3 V ≤ V_O ≤ (V+) – 0.3 V, R_L = 100 kΩ			135		dB
OUTPUT							
V_{OH}	Voltage output swing from positive rail	V_S = 1.8V, R_L = 100 kΩ to V^+/2		10	6		mV
V_{OL}	Voltage output swing from negative rail	V_S = 1.8V, R_L = 100 kΩ to V^+/2			4	10	
I_{SC}	Short-circuit current	Short to V_S/2			4.7		mA
Z_O	Open loop output impedance	f = 1 KHz, I_O = 0 A			94.5		kΩ
FREQUENCY RESPONSE							
GBP	Gain-bandwidth product	C_L = 20 pF, R_L = 10 MΩ, V_S = 5V			8		kHz
SR	Slew rate (10% to 90%)	G = 1, Rising Edge, C_L = 20 pF, V_S = 5V			1.8		V/ms
		G = 1, Falling Edge, C_L = 20 pF, V_S = 5V			1.7		
POWER SUPPLY							
$I_{Q\text{-}LPV811}$	Quiescent Current, Per Channel	V_{CM} = V-, I_O = 0, V_S = 3.3V			450	540	nA
$I_{Q\text{-}LPV812}$	Quiescent Current, Per Channel	V_{CM} = V-, I_O = 0, V_S = 3.3V			425	495	

- AN-1798 Designing with Electro-Chemical Sensors, SNOA514
- AN-1803 Design Considerations for a Transimpedance Amplifier, SNOA515
- AN-1852 Designing With pH Electrodes, SNOA529
- Compensate Transimpedance Amplifiers Intuitively, SBOA055
- Transimpedance Considerations for High-Speed Operational Amplifiers, SBOA112
- Noise Analysis of FET Transimpedance Amplifiers, SBOA060
- Circuit Board Layout Techniques, SLOA089
- Handbook of Operational Amplifier Applications, SBOA092

7.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LPV811	Click here	Click here	Click here	Click here	Click here
LPV812	Click here	Click here	Click here	Click here	Click here

7.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.6 Trademarks

E2E is a trademark of Texas Instruments.

7.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

7.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

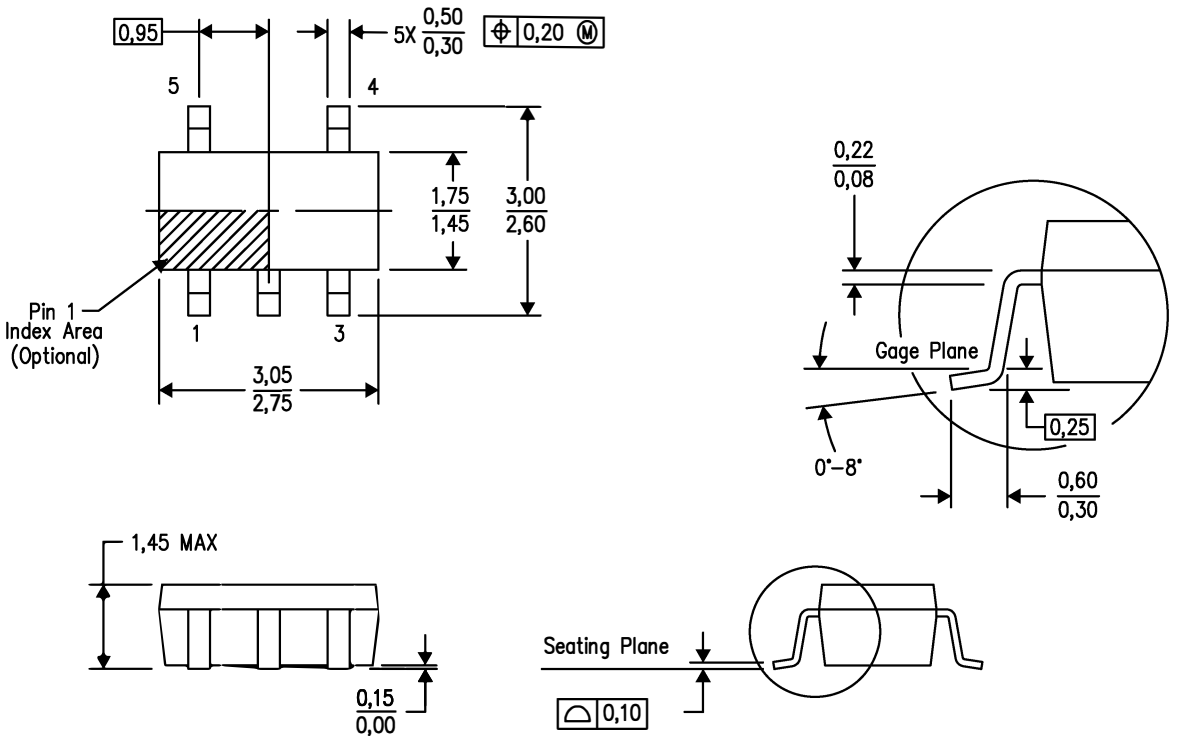
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10-Aug-2016

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LPV811DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
LPV811DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		
LPV812DGKR	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
LPV812DGKT	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		
PLPV811DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	-40 to 125		
PLPV812DGKT	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		

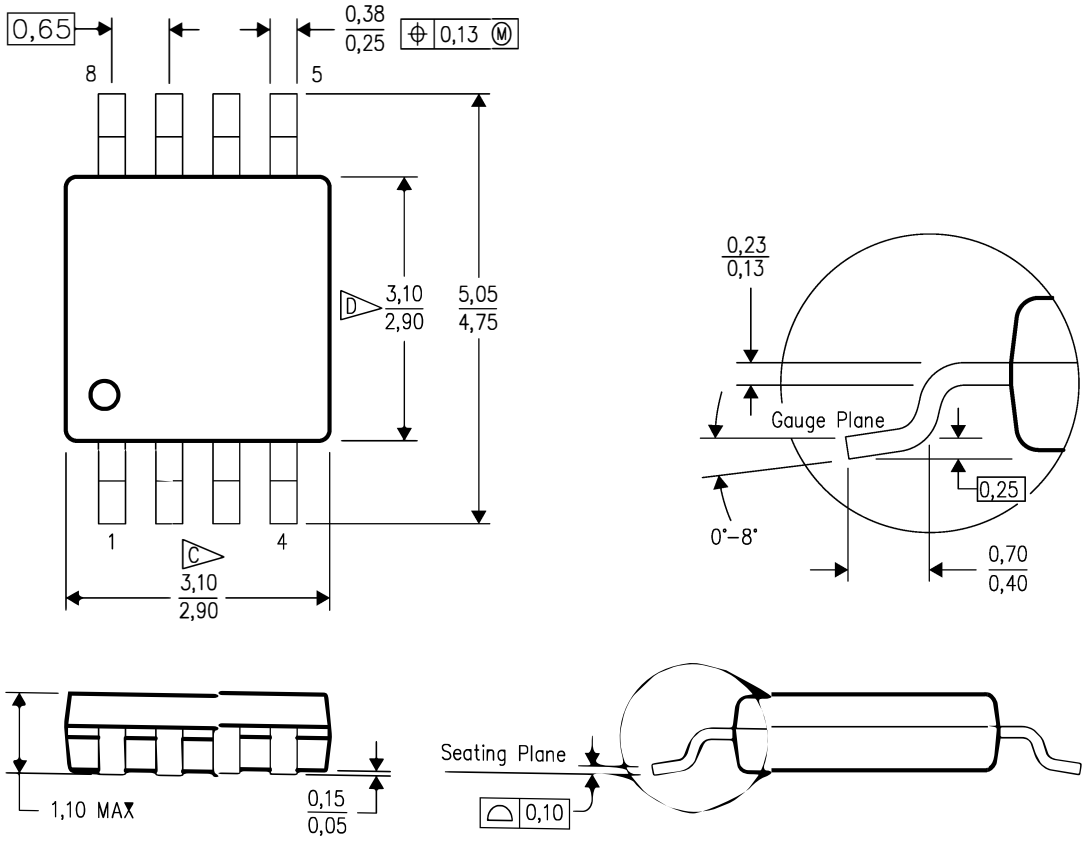
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.