MCP6L71/1R/2/4

2 MHz, 150 µA Op Amps

Features

- Gain Bandwidth Product: 2 MHz (typical)
- Supply Current: I_Q = 150 µA (typical)
- Supply Voltage: 2.0V to 6.0V
- Rail-to-Rail Input/Output
- Extended Temperature Range: –40°C to +125°C
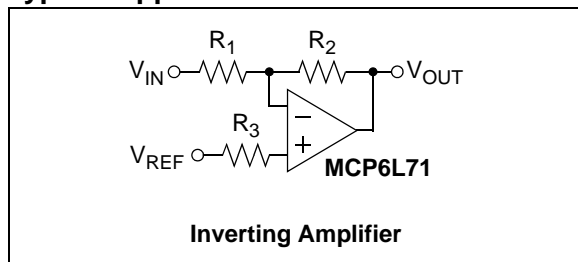- Available in Single, Dual and Quad Packages

Typical Applications

- Portable Equipment
- Photodiode Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery Powered Systems

Design Aids

- FilterLab® Software
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application

Inverting Amplifier

Description

The Microchip Technology Inc. MCP6L71/1R/2/4 family of operational amplifiers (op amps) supports general purpose applications. The combination of rail-to-rail input and output, low quiescent current and bandwidth fit into many applicaitons.

This family has a 2 MHz Gain Bandwidth Product (GBWP) and a low 150 µA per amplifier quiescent current. These op amps operate on supply voltages between 2.0V and 6.0V, with rail-to-rail input and output swing. They are available in the extended temperature range.

Package Types
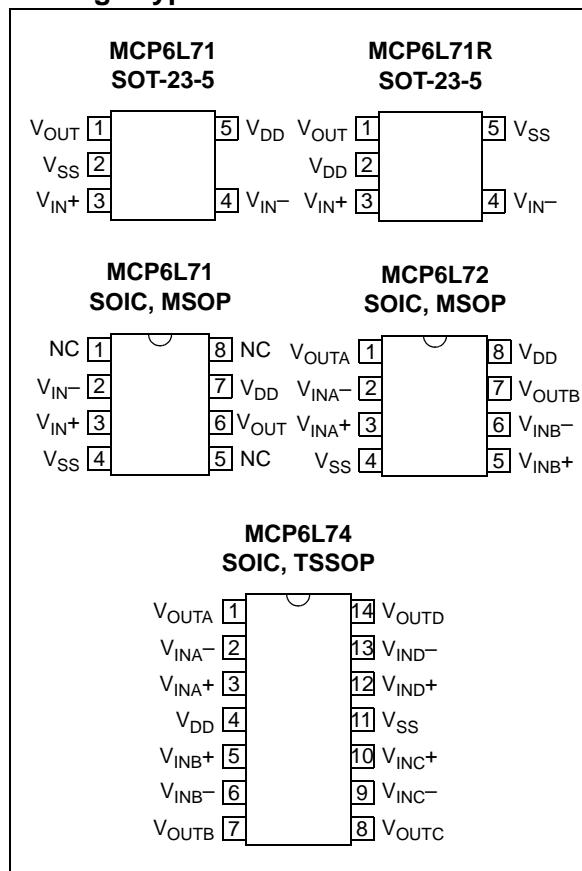
TABLE 1-1: **DC ELECTRICAL SPECIFICATIONS (CONTINUED)**

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2 and R_L = 10 kΩ to V_L. (Refer to Figure 1-1).

Parameters	Sym	Min (Note 1)	Typ	Max (Note 1)	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	2.0	—	6.0	V	
Quiescent Current per Amplifier	I_Q	50	150	240	µA	I_O = 0

Note 1: For design guidance only; not tested.

TABLE 1-2: **AC ELECTRICAL SPECIFICATIONS**

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF. (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	2.0	—	MHz	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Slew Rate	SR	—	0.9	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	4.6	—	µV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	19	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	3	—	fA/√Hz	f = 1 kHz

TABLE 1-3: **TEMPERATURE SPECIFICATIONS**

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.0V to +5.5V and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	–40	—	+125	°C	
Operating Temperature Range	T_A	–40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	–65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

1.3   Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT}; see Equation 1-1. Note that V_{CM} is not the circuit's common mode voltage $((V_P + V_M)/2)$, and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F/R_G$$
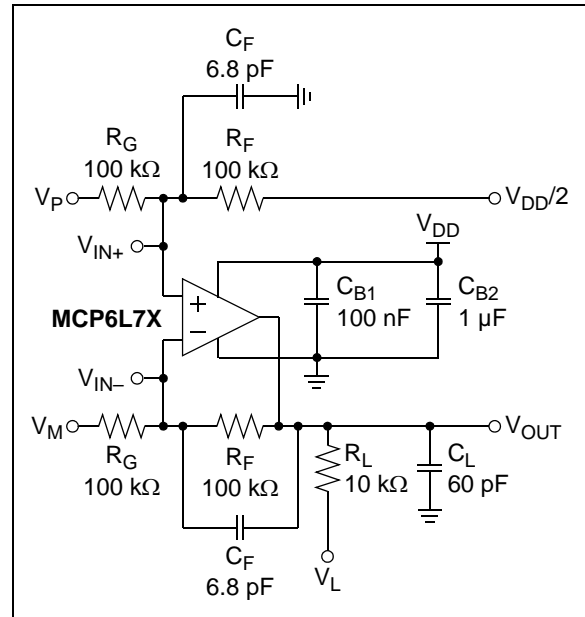$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$
Where:

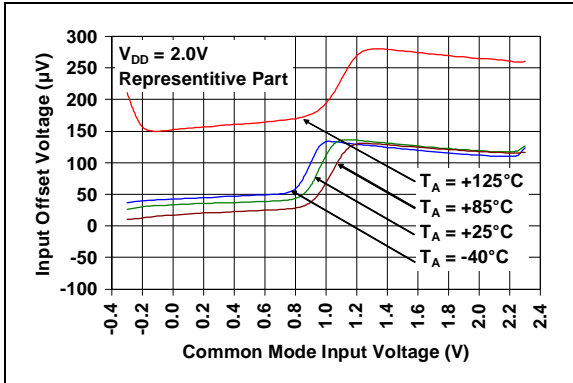|			
G_{DM}	=	Differential Mode Gain	(V/V)
V_{CM}	=	Op Amp's Common Mode Input Voltage	(V)
V_{OST}	=	Op Amp's Total Input Offset Voltage	(mV)

FIGURE 1-1:   AC and DC Test Circuit for Most Specifications.
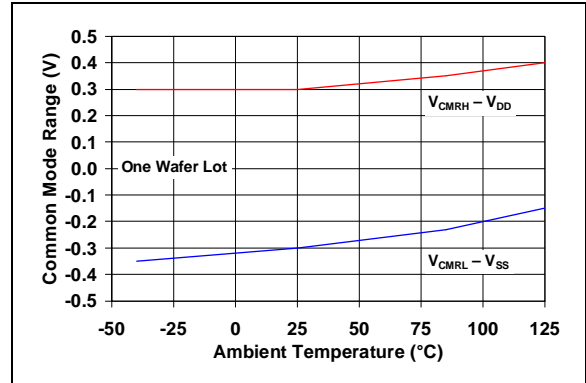
2.0   TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.
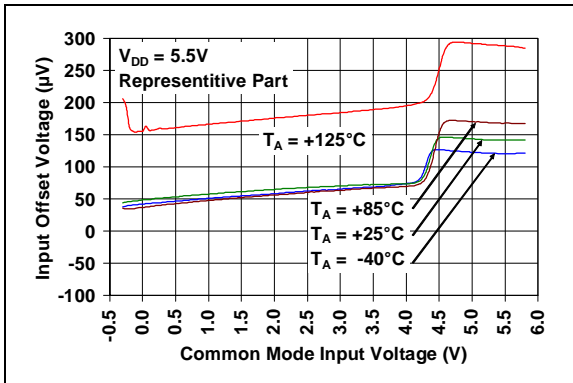
Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.0V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 10 kΩ to V_L and C_L = 60 pF.

FIGURE 2-1: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 2.0V.*

FIGURE 2-2: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

FIGURE 2-3: *Input Offset Voltage vs. Output Voltage.*

FIGURE 2-4: *Input Common Mode Range Voltage vs. Ambient Temperature.*

FIGURE 2-5: *CMRR, PSRR vs. Temperature.*
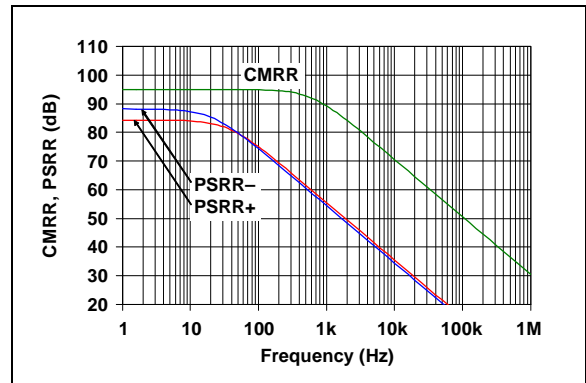
FIGURE 2-6: *CMRR, PSRR vs. Frequency.*

MCP6L71/1R/2/4

Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 5.0V$, $V_{SS} = GND$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, $R_L = 10\ k\Omega$ to V_L and $C_L = 60\ pF$.
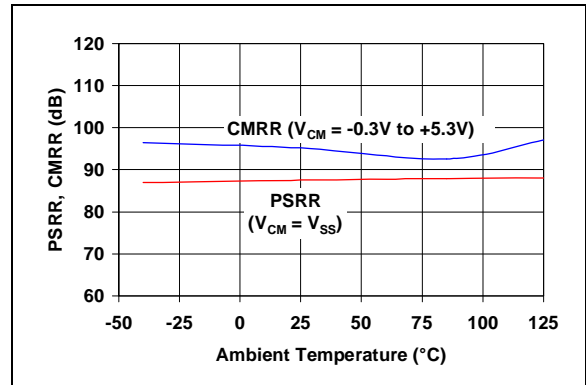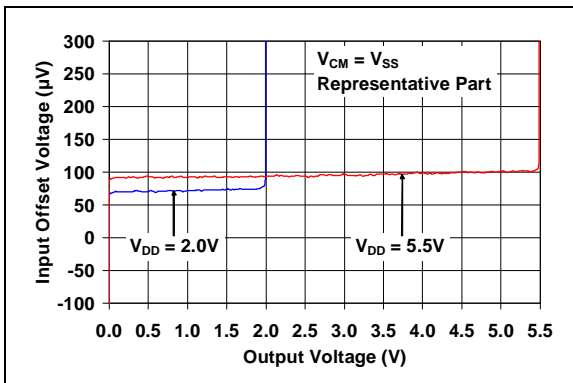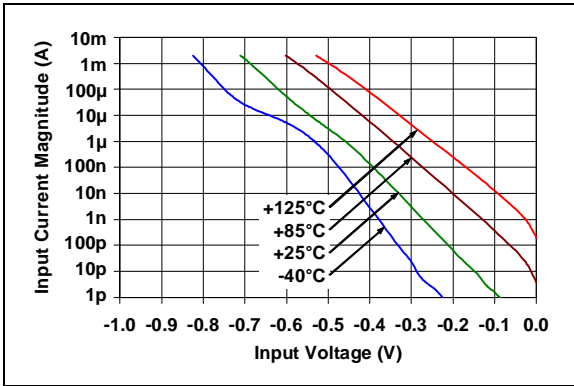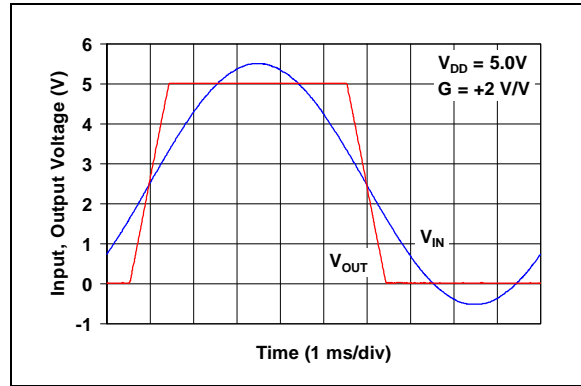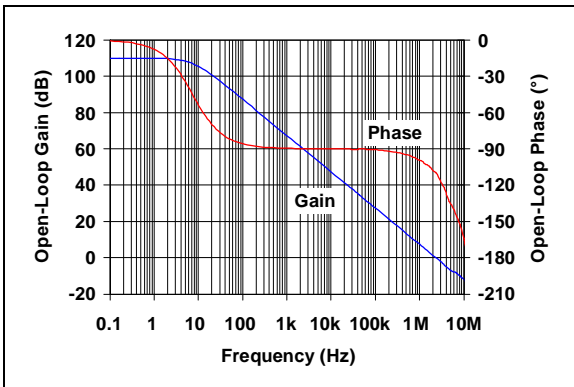

FIGURE 2-7: Input Current vs. Input Voltage.

FIGURE 2-8: Open-Loop Gain, Phase vs. Frequency.

FIGURE 2-9: Input Noise Voltage Density vs. Frequency.

FIGURE 2-10: The MCP6L71/1R/2/4 Show No Phase Reversal.

FIGURE 2-11: Quiescent Current vs. Supply Voltage.
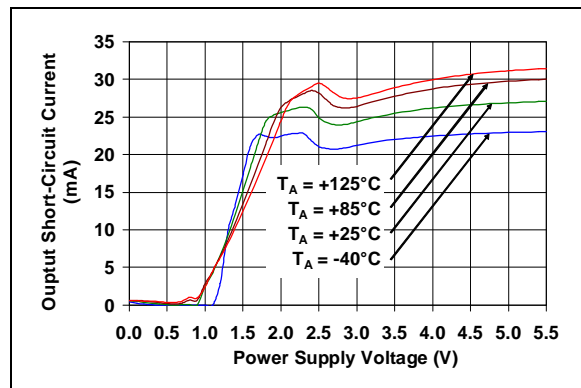
FIGURE 2-12: Output Short Circuit Current vs. Supply Voltage.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.0V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, V_{OUT} ≈ $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 10 kΩ to V_L and C_L = 60 pF.

FIGURE 2-13: *Ratio of Output Voltage Headroom vs. Output Current Magnitude.*

FIGURE 2-14: *Large Signal Non-inverting Pulse Response.*

FIGURE 2-15: *Small Signal Non-inverting Pulse Response.*

FIGURE 2-16: *Slew Rate vs. Ambient Temperature.*

FIGURE 2-17: *Maximum Output Voltage Swing vs. Frequency.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1 (single op amps) and Table 3-2 (dual and quad op amps).

TABLE 3-1: PIN FUNCTION TABLE FOR SINGLE OP AMPS

MCP6L71		MCP6L71R	Symbol	Description
MSOP, SOIC	SOT-23-5	SOT-23-5		
2	4	4	$V_{IN}-$	Inverting Input
3	3	3	$V_{IN}+$	Non-inverting Input
4	2	5	V_{SS}	Negative Power Supply
6	1	1	V_{OUT}	Analog Output
7	5	2	V_{DD}	Positive Power Supply
1,5,8	—	—	NC	No Internal Connection

TABLE 3-2: PIN FUNCTION TABLE FOR DUAL AND QUAD OP AMPS

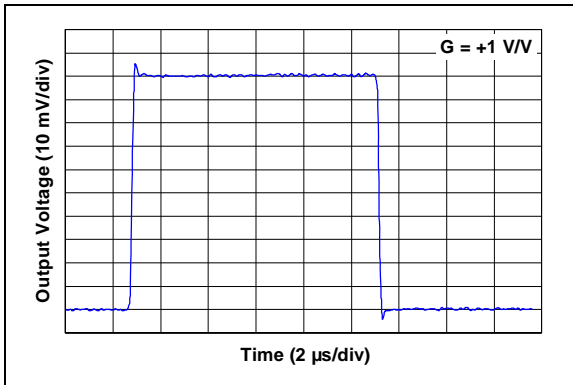| MCP6L72	MCP6L74	Symbol	Description
MSOP, SOIC	SOIC, TSSOP		
1	1	V_{OUTA}	Analog Output (op amp A)
2	2	$V_{INA}-$	Inverting Input (op amp A)
3	3	$V_{INA}+$	Non-inverting Input (op amp A)
8	4	V_{DD}	Positive Power Supply
5	5	$V_{INB}+$	Non-inverting Input (op amp B)
6	6	$V_{INB}-$	Inverting Input (op amp B)
7	7	V_{OUTB}	Analog Output (op amp B)
—	8	V_{OUTC}	Analog Output (op amp C)
—	9	$V_{INC}-$	Inverting Input (op amp C)
—	10	$V_{INC}+$	Non-inverting Input (op amp C)
4	11	V_{SS}	Negative Power Supply
—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	13	$V_{IND}-$	Inverting Input (op amp D)
—	14	V_{OUTD}	Analog Output (op amp D)

3.1 Analog Outputs

The output pins are low impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins

The positive power supply (V_{DD}) is 2.0V to 6.0V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good, high frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with nearby analog parts.

4.5 Unused Amplifiers

An unused op amp in a quad package (MCP6L74) should be configured as shown in Figure 4-3. These circuits prevent the output from toggling and causing crosstalk. In Circuit A, R_1 and R_2 produce a voltage within its output voltage range (V_{OH}, V_{OL}). The op amp buffers this voltage, which can be used elsewhere in the circuit. Circuit B uses the minimum number of components and operates as a comparator.
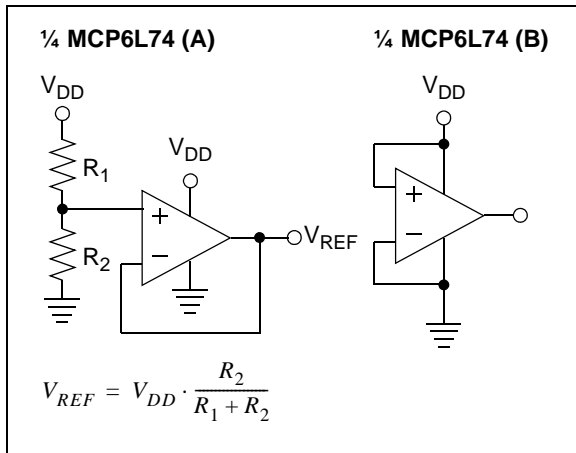

FIGURE 4-3: *Unused Op Amps.*

4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6L71/1R/2/4 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. Figure 4-4 shows an example of this type of layout.
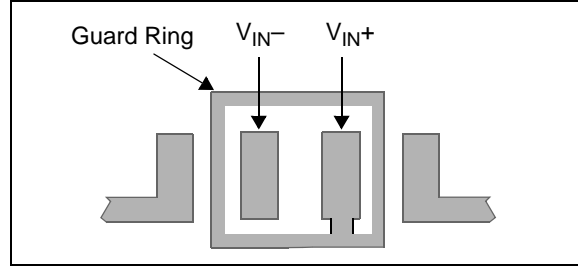

FIGURE 4-4: *Example Guard Ring Layout.*

1. For Inverting Gain and Transimpedance Amplifiers (convert current to voltage, such as photo detectors):
    a) Connect the guard ring to the non-inverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
    b) Connect the inverting pin ($V_{IN}-$) to the input with a wire that does not touch the PCB surface.
2. Non-inverting Gain and Unity Gain Buffer:
    a) Connect the guard ring to the inverting input pin ($V_{IN}-$). This biases the guard ring to the common mode input voltage.
    b) Connect the non-inverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.

4.7 Application Circuits

4.7.1 INVERTING INTEGRATOR

An inverting integrator is shown in Figure 4-5. The circuit provides an output voltage that is proportional to the negative time-integral of the input. The additional resistor R_2 limits DC gain and controls output clipping. To minimize the integrator's error for slow signals, the value of R_2 should be much larger than the value of R_1.
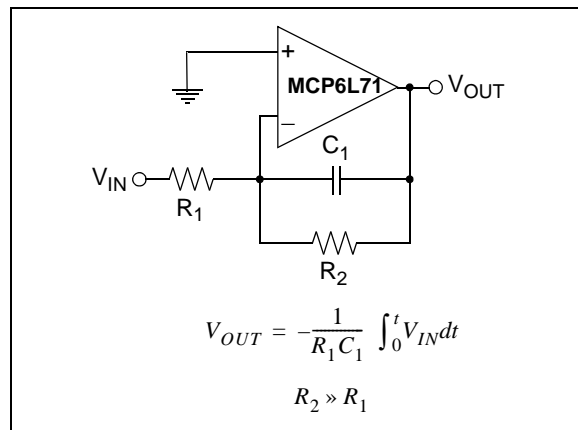

FIGURE 4-5: *Inverting Integrator.*

5.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP6L71/1R/2/4 family of op amps.

5.1 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.2 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/ maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data sheets, Purchase, and Sampling of Microchip parts.

5.3 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/ analogtools.

Some boards that are especially useful are:

• MCP6XXX Amplifier Evaluation Board 1
• MCP6XXX Amplifier Evaluation Board 2
• MCP6XXX Amplifier Evaluation Board 3
• MCP6XXX Amplifier Evaluation Board 4
• Active Filter Demo Board Kit
• 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
• 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
• 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

5.4 Application Notes

The following Microchip Application Notes are available on the Microchip web site at www.microchip. com/appnotes and are recommended as supplemental reference resources.

• **ADN003:** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
• **AN722:** *"Operational Amplifier Topologies and DC Specifications",* DS00722
• **AN723:** *"Operational Amplifier AC Specifications and Applications",* DS00723
• **AN884:** *"Driving Capacitive Loads With Op Amps",* DS00884
• **AN990:** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990

6.0 PACKAGING INFORMATION
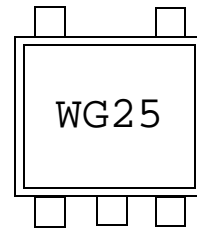
6.1 Package Marking Information
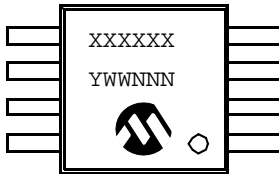
5-Lead SOT-23 (**MCP6L71, MCP6L71R**)

Example:

XXNN

WG25
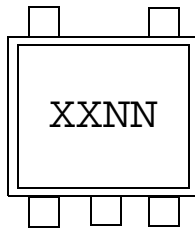
Device	Code
MCP6L71	WGNN
MCP6L71R	WFNN

Note: Applies to 5-Lead SOT-23

8-Lead MSOP (**MCP6L71, MCP6L72**)

Example:

XXXXXX
YWWNNN
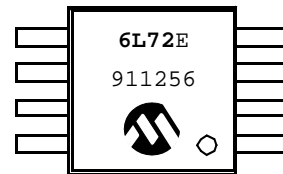
6L72E
911256

8-Lead SOIC (150 mil) (**MCP6L71, MCP6L72**)

Example:

XXXXXXXX
XXXXXYYWW
NNN

MCP6L72E
SN(e3)0911
256
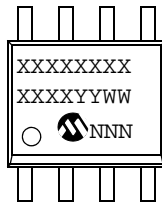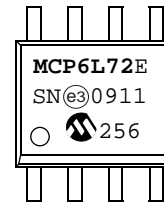
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

14-Lead SOIC (150 mil) **(MCP6L74)**

```
  ┌─────────────────────────┐
  │      XXXXXXXXXX          │
  │      XXXXXXXXXX          │
  │  ○    Ⓜ    YYWWNNN       │
  └─────────────────────────┘
```
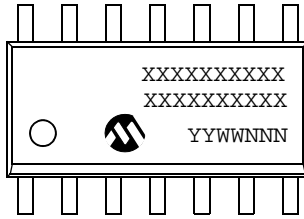
Example:

```
  ┌─────────────────────────┐
  │         MCP6L74          │
  │          E/SLⓔ3          │
  │  ○    Ⓜ   0911256        │
  └─────────────────────────┘
```

14-Lead TSSOP **(MCP6L74)**

```
  ┌──────────────────┐
  │   XXXXXXXX        │
  │   Ⓜ   YYWW        │
  │                   │
  │   ○   NNN         │
  └──────────────────┘
```

Example:

```
  ┌──────────────────┐
  │   6L74EST         │
  │   Ⓜ   0911        │
  │                   │
  │   ○      256      │
  └──────────────────┘
```
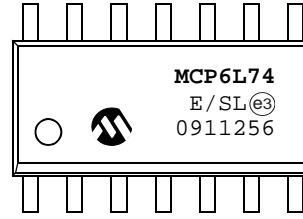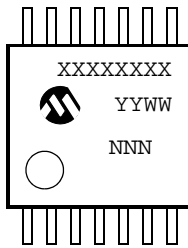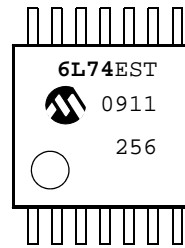
5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

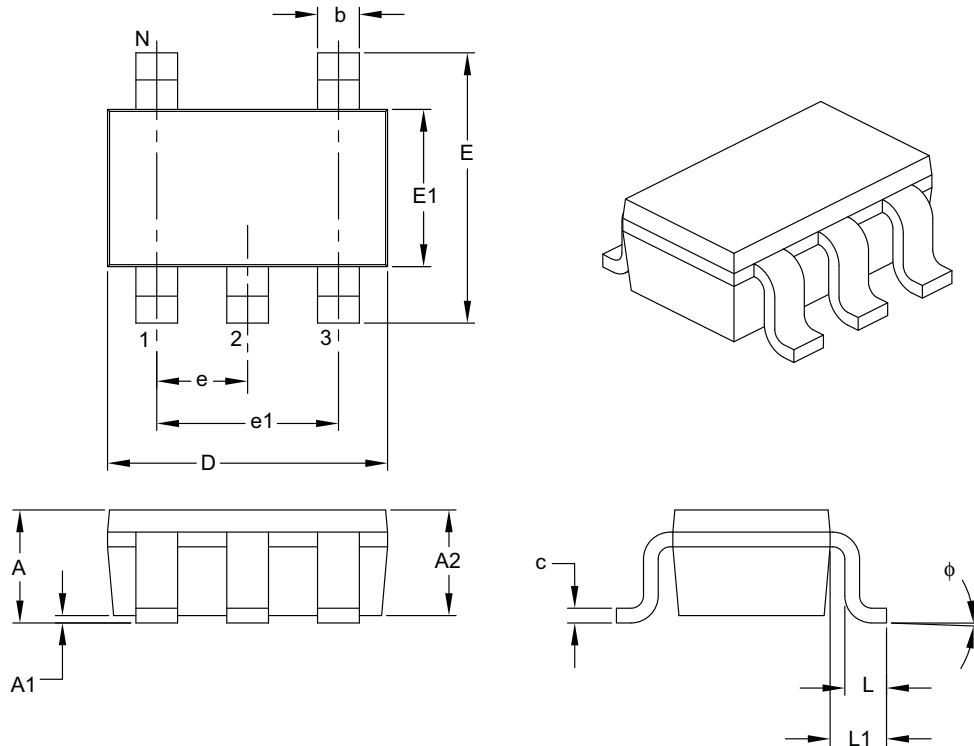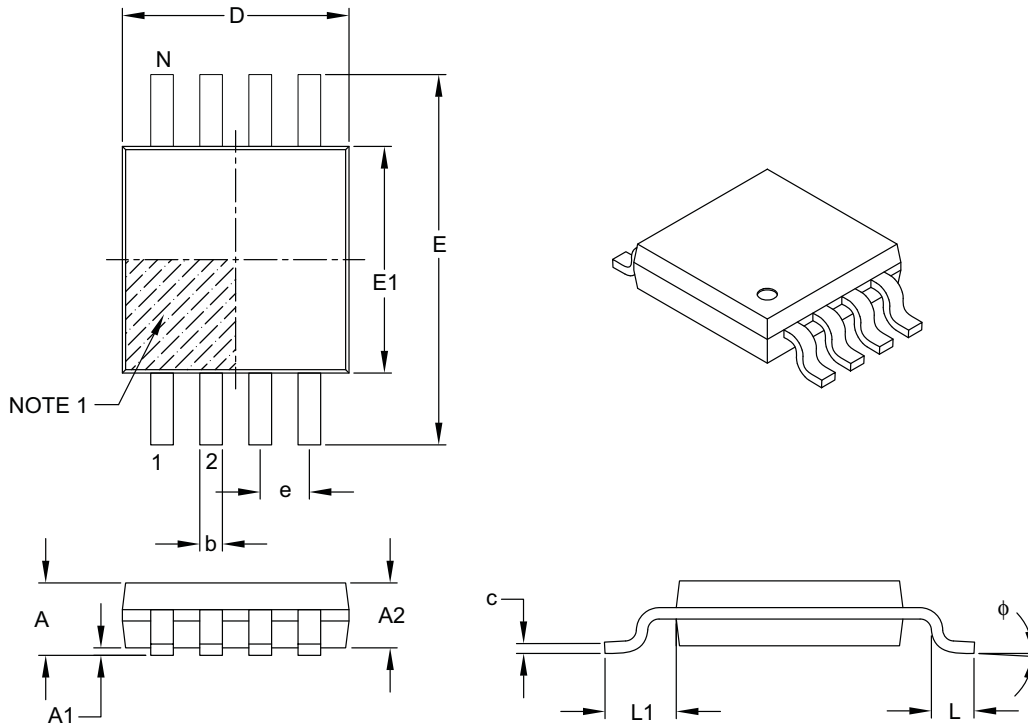|	Unit	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pin	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	φ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Unit	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pin	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

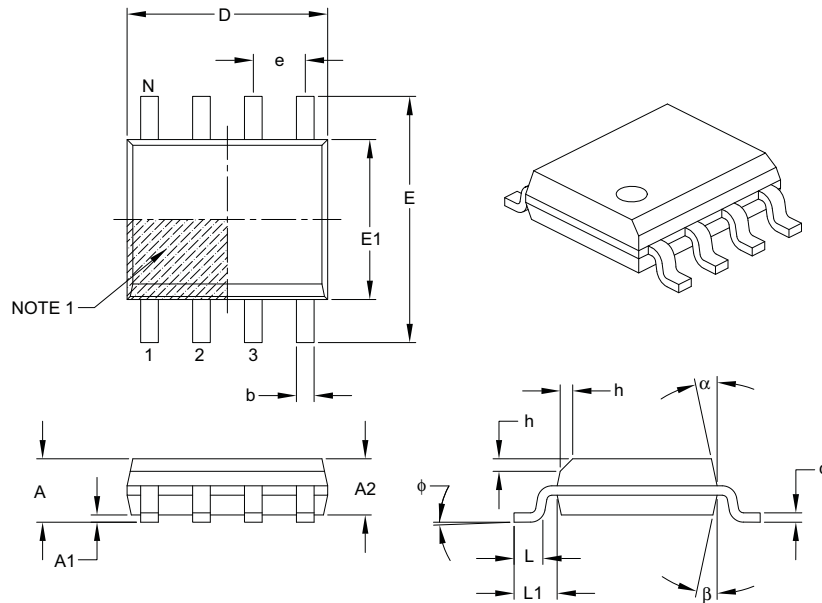3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Unit	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pin	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
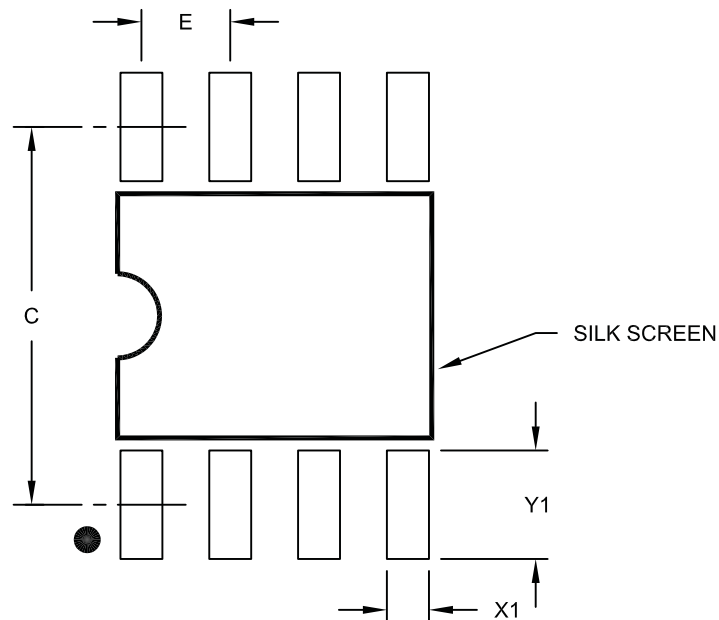4. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

E

C

SILK SCREEN

Y1

X1

RECOMMENDED LAND PATTERN

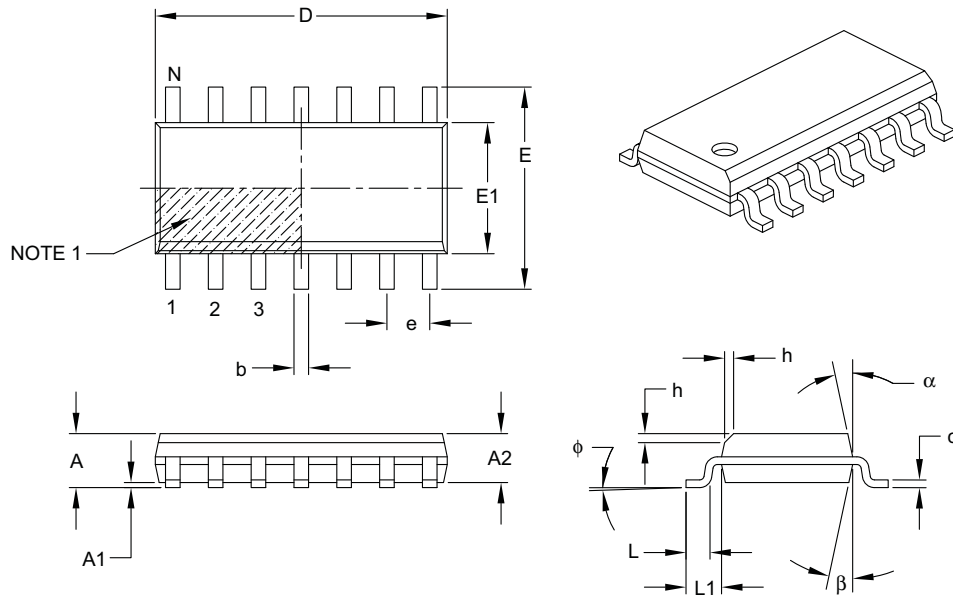|	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

14-Lead Plastic Small Outline (SL) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Unit	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pin	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
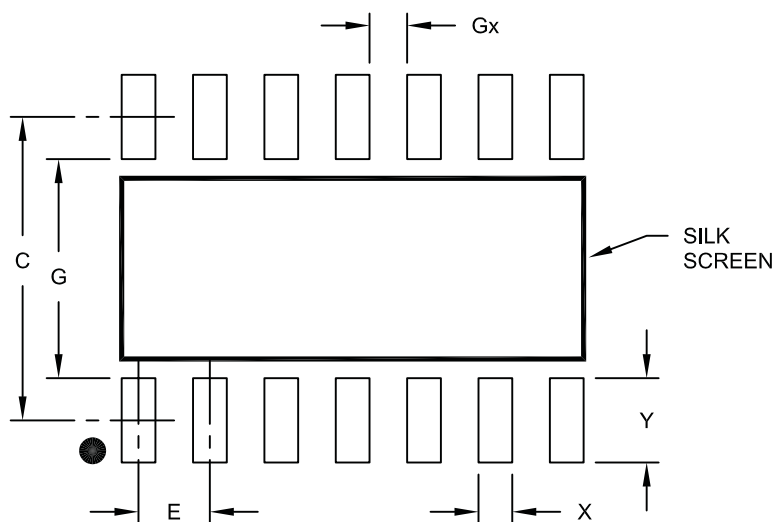4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-065B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

MCP6L71/1R/2/4

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]
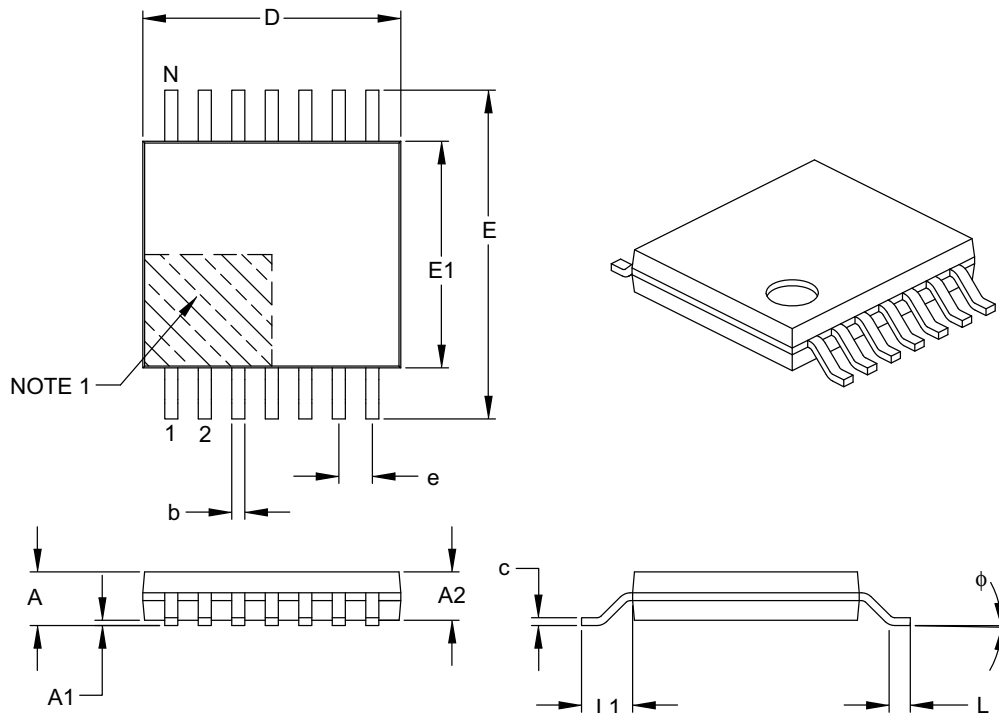
	Unit	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pin	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-087B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.　　—　　X　　　/XX

　　Device　　Temperature　　Package
　　　　　　　　Range

Device:　　　　　　　MCP6L71T:　　Single Op Amp (Tape and Reel)
　　　　　　　　　　　　　　　　　　(MSOP, SOIC, SOT-23-5)
　　　　　　　　　　MCP6L71RT:　　Single Op Amp (Tape and Reel)
　　　　　　　　　　　　　　　　　　(SOT-23-5)
　　　　　　　　　　MCP6L72T:　　Dual Op Amp (Tape and Reel)
　　　　　　　　　　　　　　　　　　(MSOP, SOIC)
　　　　　　　　　　MCP6L74T:　　Quad Op Amp (Tape and Reel)
　　　　　　　　　　　　　　　　　　(SOIC, TSSOP)

Temperature Range:　　E　=　-40°C to +125°C

Package:　　　　　　OT　=　Plastic Small Outline Transistor (SOT-23), 5-lead
　　　　　　　　　　　　　　(MCP6L71, MCP6L71R)
　　　　　　　　　　MS　=　Plastic MSOP, 8-lead
　　　　　　　　　　SN　=　Plastic SOIC, (150 mil Body), 8-lead
　　　　　　　　　　SL　=　Plastic SOIC (150 mil Body), 14-lead
　　　　　　　　　　ST　=　Plastic TSSOP (4.4 mm Body), 14-lead

Examples:

a)　MCP6L71T-E/OT:　Tape and Reel,
　　　　　　　　　　　5LD SOT-23 package.
b)　MCP6L71T-E/MS:　Tape and Reel,
　　　　　　　　　　　8LD MSOP package.
c)　MCP6L71T-E/SN:　Tape and Reel,
　　　　　　　　　　　8LD SOIC package.

a)　MCP6L71RT-E/OT:　Tape and Reel,
　　　　　　　　　　　5LD SOT-23 package.

a)　MCP6L72T-E/MS:　Tape and Reel,
　　　　　　　　　　　8LD MSOP package.
b)　MCP6L72T-E/SN:　Tape and Reel,
　　　　　　　　　　　8LD SOIC package.

a)　MCP6L74T-E/SL:　Tape and Reel,
　　　　　　　　　　　14LD SOIC package.
b)　MCP6L74-E/ST:　Tape and Reel,
　　　　　　　　　　　14LD TSSOP package.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

Worldwide Sales and Service

Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4080

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820