OPAx354 250-MHz, Rail-to-Rail I/O, CMOS Operational Amplifiers

1 Features

- Unity-Gain Bandwidth: 250 MHz
- Wide Bandwidth: 100-MHz GBW
- High Slew Rate: 150 V/µs
- Low Noise: 6.5 nV/√Hz
- Rail-to-Rail I/O
- High Output Current: > 100 mA
- Excellent Video Performance:
  - Differential Gain: 0.02%, Differential Phase: 0.09°
  - 0.1-dB Gain Flatness: 40 MHz
- Low Input Bias Current: 3 pA
- Quiescent Current: 4.9 mA
- Thermal Shutdown
- Supply Range: 2.5 V to 5.5 V
- *Micro*SIZE and PowerPAD™ Packages

2 Applications

- Video Processing
- Ultrasound
- Optical Networking, Tunable Lasers
- Photodiode Transimpedance Amps
- Active Filters
- High-Speed Integrators
- Analog-to-Digital (A/D) Converter Input Buffers
- Digital-to-Analog (D/A) Converter Output Amplifiers
- Barcode Scanners
- Communications

3 Description

The OPAx354 series of high-speed, voltage-feedback CMOS operational amplifiers are designed for video and other applications requiring wide bandwidth. They are unity-gain stable and can drive large output currents. Differential gain is 0.02% and differential phase is 0.09°. Quiescent current is only 4.9 mA per channel.

The OPAx354 series of op amps are optimized for operation on single or dual supplies as low as 2.5 V (±1.25 V) and up to 5.5 V (±2.75 V). Common-mode input range extends beyond the supplies. The output swing is within 100 mV of the rails, supporting wide dynamic range.

For applications requiring the full 100-mA continuous output current, single and dual 8-pin HSOP PowerPAD versions are available.

The single version (OPA354) is available in the tiny 5-pin SOT-23 and 8-pin HSOP PowerPAD packages. The dual version (OPA2354) comes in the miniature 8-pin VSSOP and 8-pin HSOP PowerPAD packages. The quad version (OPA4354) is offered in 14-pin TSSOP and 14-pin SOIC packages.

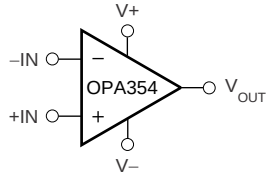
Multichannel version features completely independent circuitry for lowest crosstalk and freedom from interaction. All features are specified over the extended –40°C to +125°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA354	HSOP (8)	4.89 mm × 3.90 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
OPA2354	VSSOP (8)	3.00 mm × 3.00 mm
	HSOP (8)	4.89 mm × 3.90 mm
OPA4354	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Revision F (June 2016) to Revision G **Page**

- Deleted table note about input pins and input signals from *Absolute Maximum Ratings* table ... 6

Changes from Revision E (March 2002) to Revision F **Page**

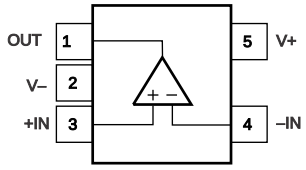
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Package/Ordering Information* table, see POA at the end of the data sheet ... 1
- Renamed *OPAx354 Related Products* table to *Device Comparison Table* ... 3

5 Device Comparison Table

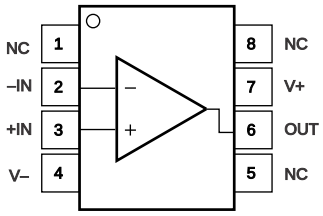
FEATURES	PRODUCT
Shutdown Version of OPAx354 Family	OPAx357
200-MHz GBW, Rail-to-Rail Output, CMOS, Shutdown	OPAx355
200-MHz GBW, Rail-to-Rail Output, CMOS	OPAx356
38-MHz GBW, Rail-to-Rail Input/Output, CMOS	OPAx350/OPAx353
75-MHz BW G = 2, Rail-to-Rail Output	OPA2631
150-MHz BW G = 2, Rail-to-Rail Output	OPA2634
100-MHz BW, Differential Input/Output, 3.3-V Supply	THS412x

6 Pin Configuration and Functions

OPA354 DBV Package
5-Pin SOT-23
Top View



OPA354 DDA Package
8-Pin HSOP
Top View



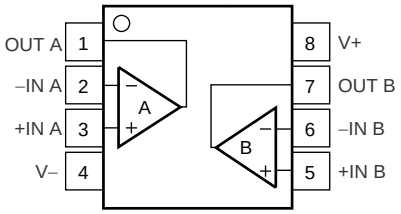
NC – no internal connection

PowerPAD must be connected to V− or left floating.

Pin Functions: OPA354

PIN			I/O	DESCRIPTION
NAME	SOT-23	HSOP		
–IN	4	2	I	Inverting input
+IN	3	3	I	Noninverting input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V–	2	4	—	Negative (lowest) supply
V+	5	7	—	Positive (highest) supply

OPA2354 DGK and DDA Packages
8-Pin VSSOP, HSOP
Top View

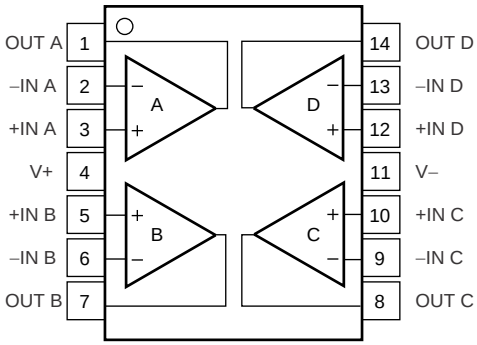


(1) PowerPAD must be connected to V− or left floating.

Pin Functions: OPA2354

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply
V+	8	—	Positive (highest) supply

OPA4354 D and PW Packages
14-Pin SOIC, TSSOP
Top View



Pin Functions: OPA4354

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply
V+	4	—	Positive (highest) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V+ to V−		7.5	V
	Signal input terminals	(V−) − (0.5)	(V+) + 0.5	
Current	Signal input terminals	–10	10	mA
	Output short circuit(2)	Continuous		
Temperature	Operating, T_A	–55	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V– to V+	2.5	5.5	V
	Specified temperature	–40	125	°C

7.4 Thermal Information: OPA354

THERMAL METRIC[1]		OPA354		UNIT
		DBV (SOT-23)	DDA (HSOP)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216.3	42.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.3	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.1	26.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.3	26.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2354

THERMAL METRIC[1]		OPA2354		UNIT
		DDA (HSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.6	175.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	97.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.6	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.6	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4354

THERMAL METRIC[1]		OPA4354		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics: V_S = 2.7 V to 5.5 V (Single-Supply)

at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V T_A = 25°C		±2	±8	mV
		V_S = 5 V, T_A = −40°C to +125°C			±10	
dV_{OS}/dT	Input offset voltage vs temperature	V_S = 5 V T_A = −40°C to +125°C		±4		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.7 V to 5.5 V V_{CM} = (V_S / 2) − 0.55 V		±200	±800	µV/V
		V_S = 2.7 V to 5.5 V V_{CM} = (V_S / 2) − 0.55 V at T_A = −40°C to +125°C			±900	
INPUT BIAS CURRENT						
I_B	Input bias current			3	±50	pA
I_{OS}	Input offset current			±1	±50	pA
NOISE						
e_n	Input voltage noise density	f = 1 MHz		6.5		nV/√Hz
i_n	Current noise density	f = 1 MHz		50		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		(V−) − 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V –0.1 V < V_{CM} < 3.5 V T_A = 25°C	66	80		dB
		V_S = 5.5 V –0.1 V < V_{CM} < 3.5 V T_A = −40°C to +125°C	64			
		V_S = 5.5 V –0.1 V < V_{CM} < 5.6 V T_A = 25°C	56	68		
		V_S = 5.5 V –0.1 V < V_{CM} < 5.6 V T_A = −40°C to +125°C	55			
INPUT IMPEDANCE						
	Differential			10^{13} || 2		Ω || pF
	Common-mode			10^{13} || 2		Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop gain	V_S = 5.5 V 0.3 V < V_O < 4.7 V T_A = 25°C	94	110		dB
		V_S = 5 V 0.4 V < V_O < 4.6 V T_A = −40°C to +125°C	90			
FREQUENCY RESPONSE						
f_{-3dB}	Small-signal bandwidth	At G = +1 V_O = 100 mV_{PP} R_F = 25 Ω		250		MHz
		At G = +2 V_O = 100 mV_{PP}		90		
GBW	Gain-bandwidth product	G = +10		100		MHz
$f_{0.1dB}$	Bandwidth for 0.1-dB gain flatness	At G = +2 V_O = 100 mV_{PP}		40		MHz

Electrical Characteristics: V_S = 2.7 V to 5.5 V (Single-Supply) (continued)

at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	V_S = 5 V, G = +1, 4-V step		150		V/µs
		V_S = 5 V, G = +1, 2-V step		130		
		V_S = 3 V, G = +1, 2-V step		110		
	Rise-and-fall time	At G = +1 V_O = 200 mV_{PP} 10% to 90%		2		ns
		At G = +1, V_O = 2 V_{PP}, 10% to 90%		11		
	Settling time	0.1%, V_S = 5 V, G = +1 2-V output step		30		ns
		0.01%, V_S = 5 V, G = +1 2-V output step		60		
	Overload recovery time	V_{IN} × Gain = V_S		5		ns

Electrical Characteristics: V_S = 2.7 V to 5.5 V (Single-Supply) (continued)

at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE (CONTINUED)							
	Harmonic distortion	Second harmonic	At G = +1, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–75		dBc
		Third harmonic	At G = +1, f = 1 MHz V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–83		
	Differential gain error		NTSC, R_L = 150 Ω		0.02%		
	Differential phase error		NTSC, R_L = 150 Ω		0.09		°
	Channel-to-channel crosstalk	OPA2354	f = 5 MHz		–100		dB
		OPA4354			–84		
OUTPUT							
	Voltage output swing from rail		V_S = 5 V, R_L = 1 kΩ, A_{OL} > 94 dB T_A = 25°C		0.1	0.3	V
			V_S = 5 V, R_L = 1 kΩ, A_{OL} > 90 dB T_A = −40°C to +125°C			0.4	
I_O	Output current, single, dual, quad[1][2]		V_S = 5 V	100			mA
			V_S = 3 V		50		mA
	Closed-loop output impedance		f < 100 kHz		0.05		Ω
R_O	Open-loop output resistance				35		Ω
POWER SUPPLY							
V_S	Specified voltage			2.7		5	V
	Operating voltage			2.5		5.5	
I_Q	Quiescent current (per amplifier)		T_A = 25°C, V_S = 5 V (enabled) I_O = 0		4.9	6	mA
			T_A = –40°C to +125°C			7.5	
THERMAL SHUTDOWN: JUNCTION TEMPERATURE							
	Shutdown				160		°C
	Reset from shutdown				140		°C
THERMAL RANGE							
	Specified			–40		125	°C
	Operating			–55		150	°C
	Storage			–65		150	°C

(1) See typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 20 and Figure 22).
(2) Specified by design.

7.8 Typical Characteristics

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

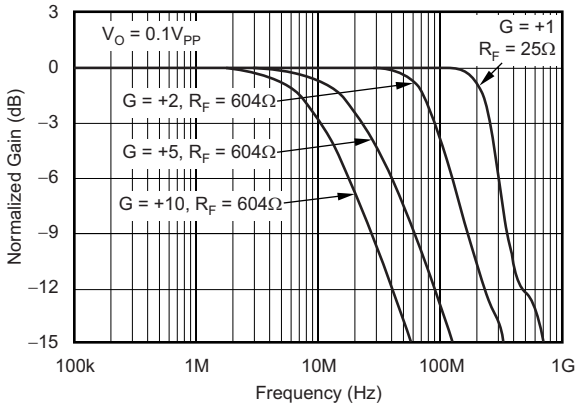


Figure 1. Noninverting Small-Signal Frequency Response

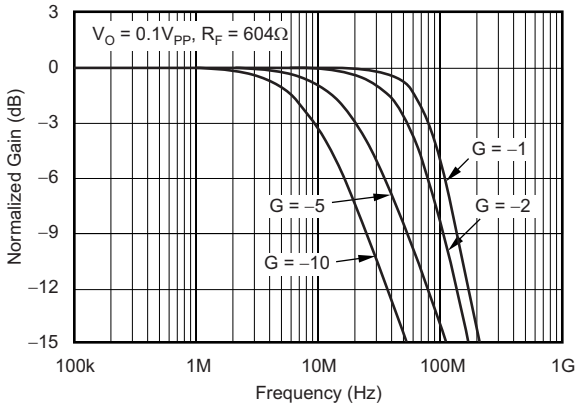


Figure 2. Inverting Small-Signal Frequency Response

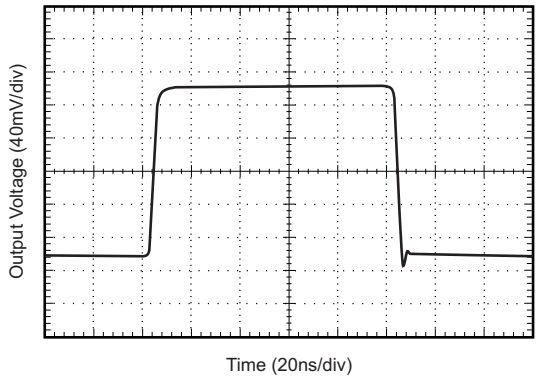


Figure 3. Noninverting Small-Signal Step Response

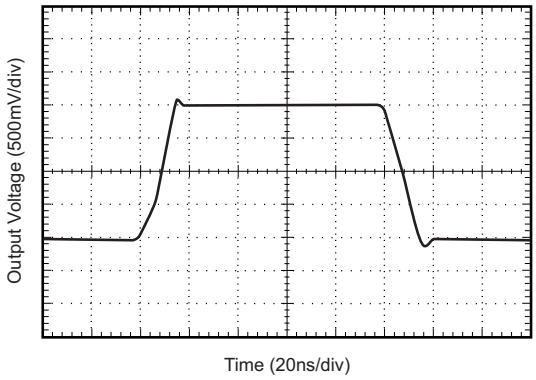


Figure 4. Noninverting Large-Signal Step Response

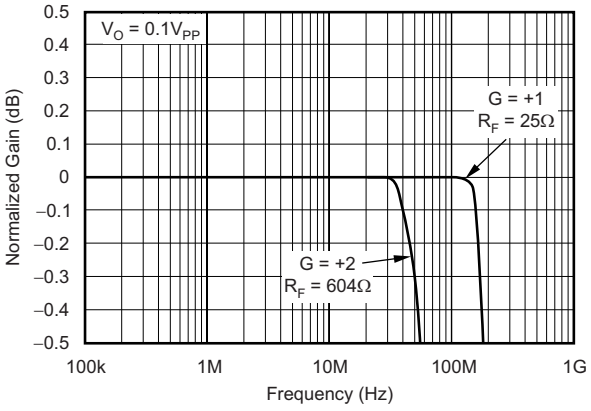


Figure 5. 0.1-dB Gain Flatness

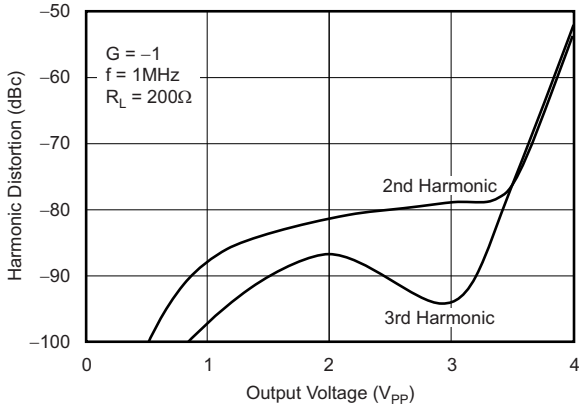


Figure 6. Harmonic Distortion vs Output Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

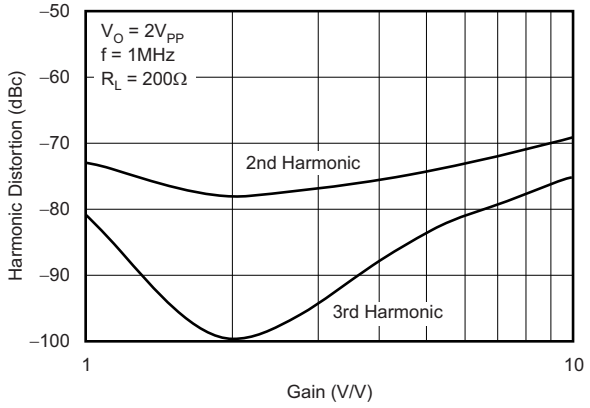


Figure 7. Harmonic Distortion vs Noninverting Gain

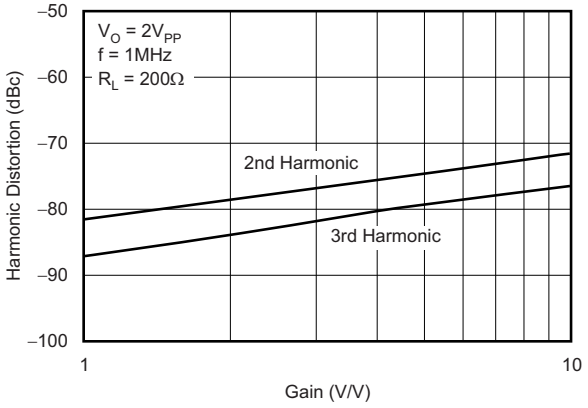


Figure 8. Harmonic Distortion vs Inverting Gain

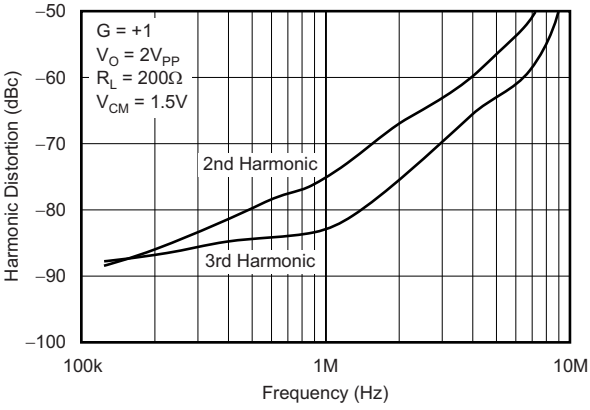


Figure 9. Harmonic Distortion vs Frequency

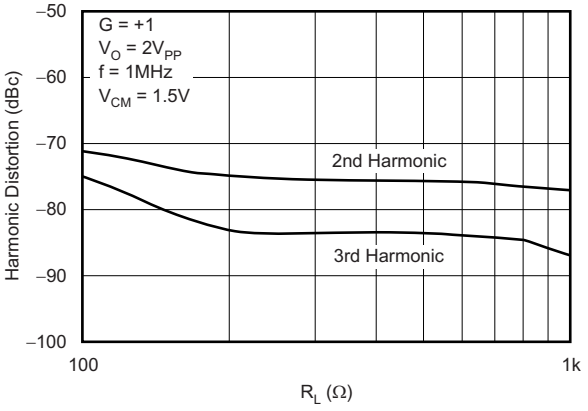


Figure 10. Harmonic Distortion vs Load Resistance

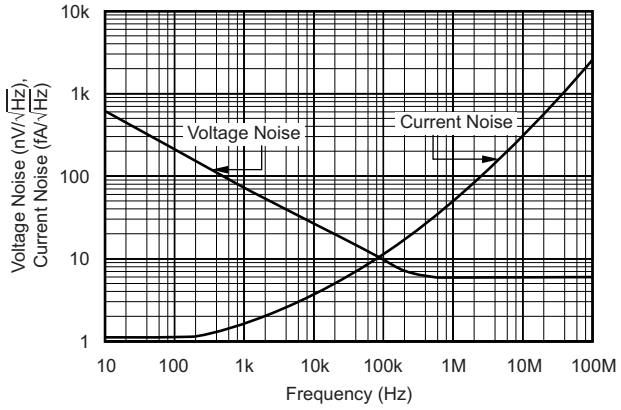


Figure 11. Input Voltage and Current Noise Spectral Density vs Frequency

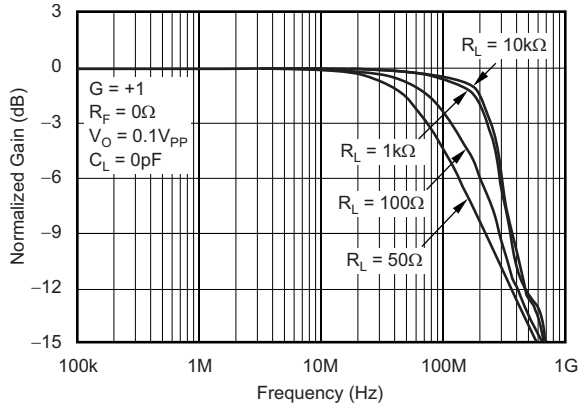


Figure 12. Frequency Response for Various R_L Values

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

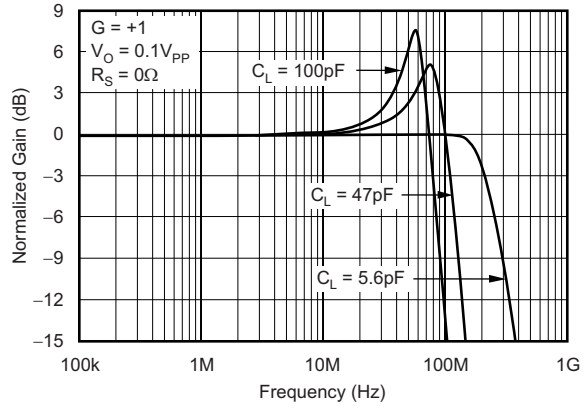


Figure 13. Frequency Response for Various C_L Values

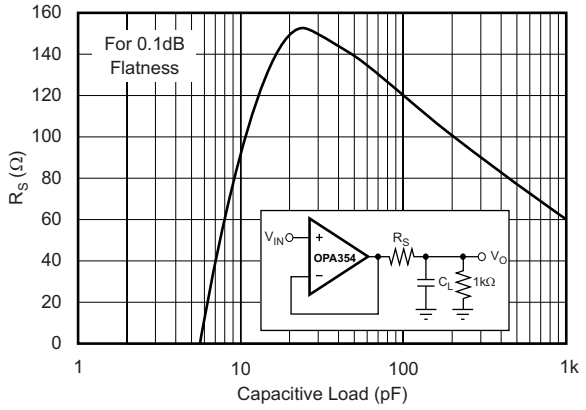


Figure 14. Recommended R_S vs Capacitive Load

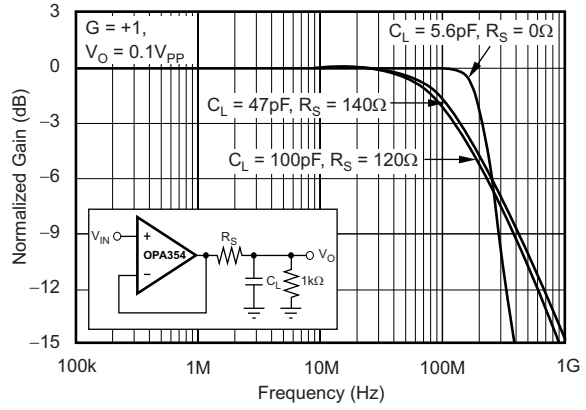


Figure 15. Frequency Response vs Capacitive Load

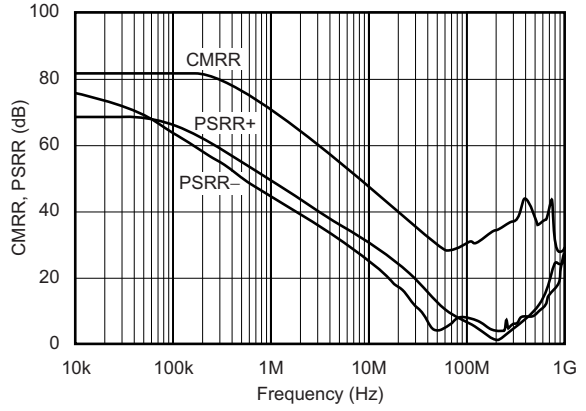


Figure 16. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

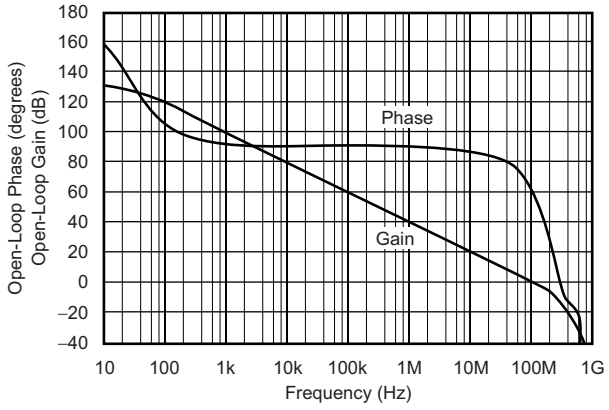


Figure 17. Open-Loop Gain and Phase

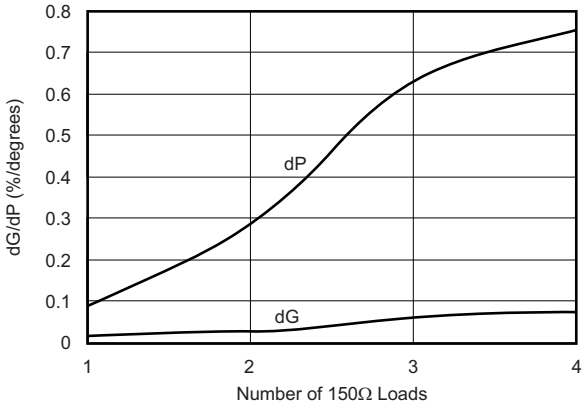


Figure 18. Composite Video Differential Gain and Phase

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

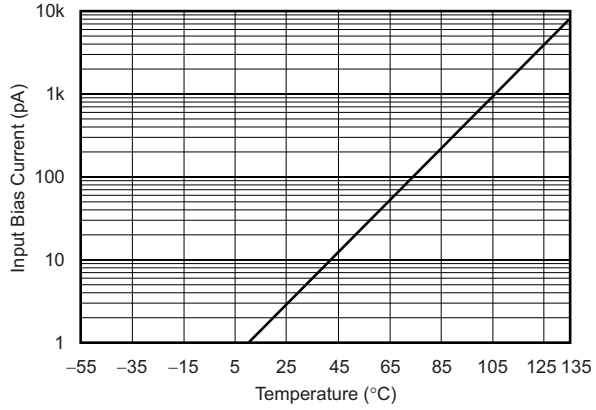


Figure 19. Input Bias Current vs Temperature

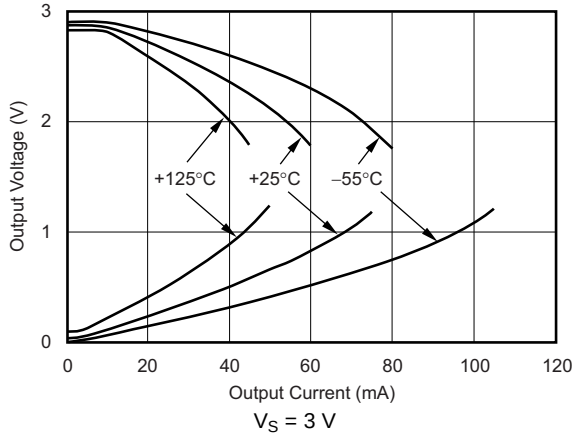


Figure 20. Output Voltage Swing vs Output Current

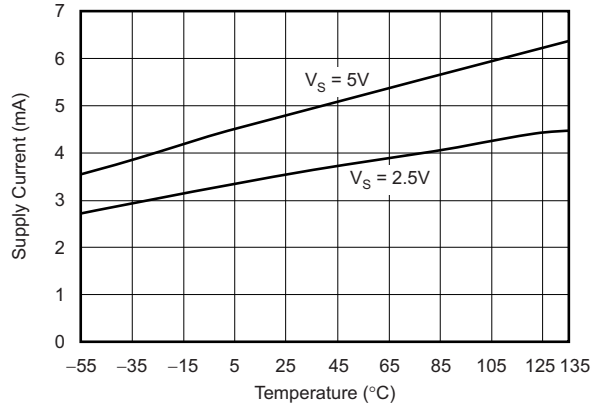


Figure 21. Supply Current vs Temperature

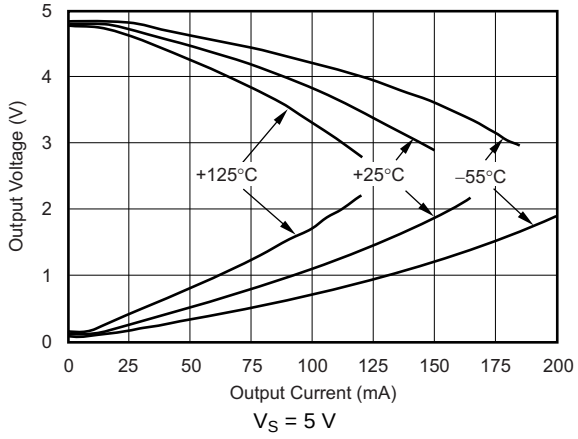


Figure 22. Output Voltage Swing vs Output Current

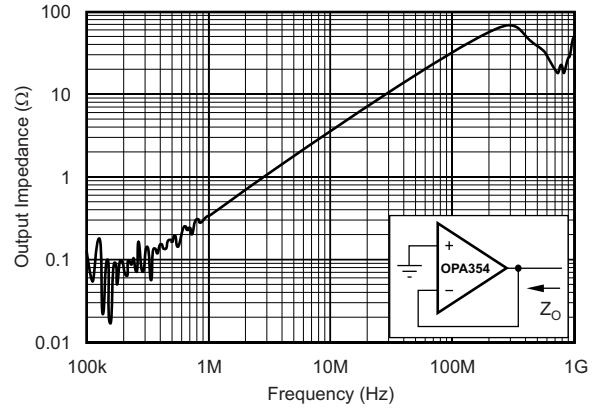


Figure 23. Closed-Loop Output Impedance vs Frequency

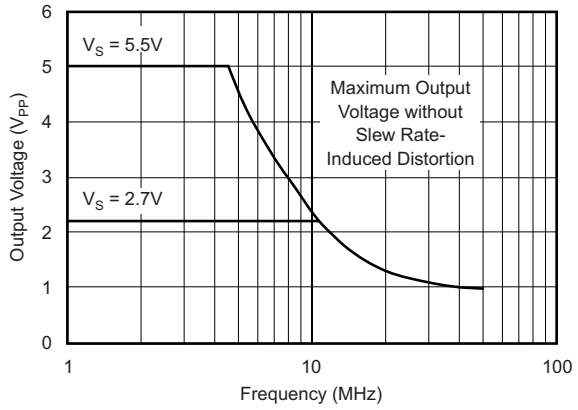


Figure 24. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2, (unless otherwise noted)

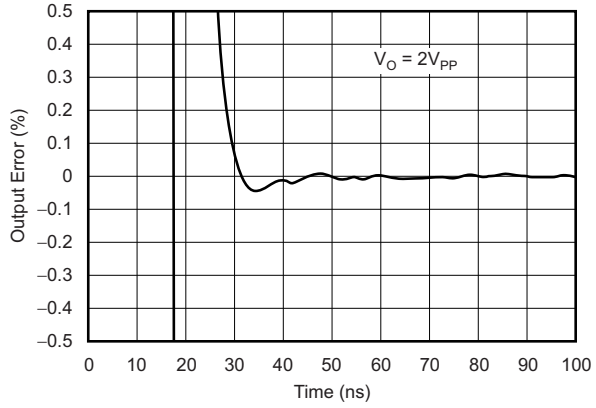


Figure 25. Output Settling Time to 0.1%

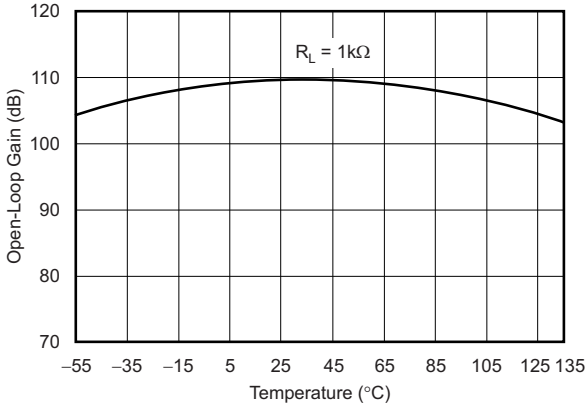


Figure 26. Open-Loop Gain vs Temperature

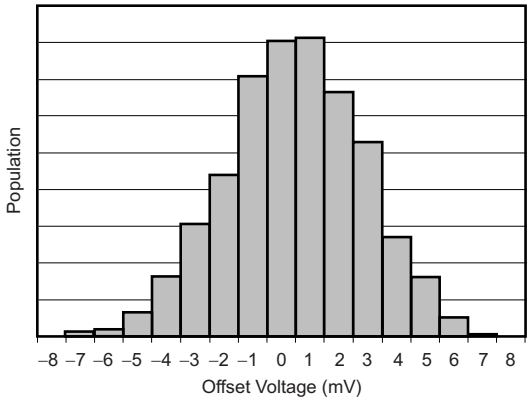


Figure 27. Offset Voltage Production Distribution

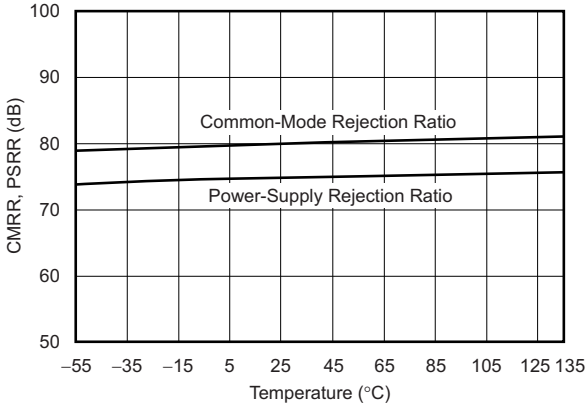


Figure 28. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

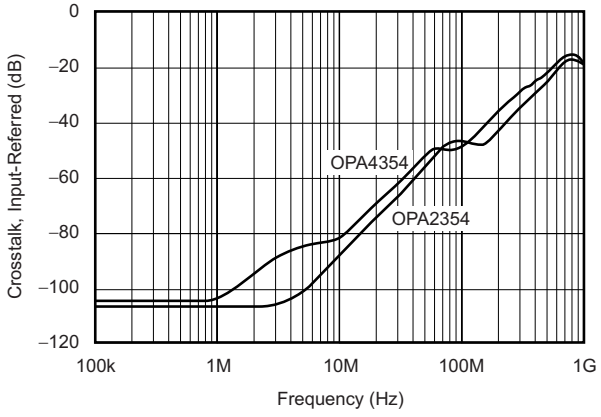


Figure 29. Channel-to-Channel Crosstalk

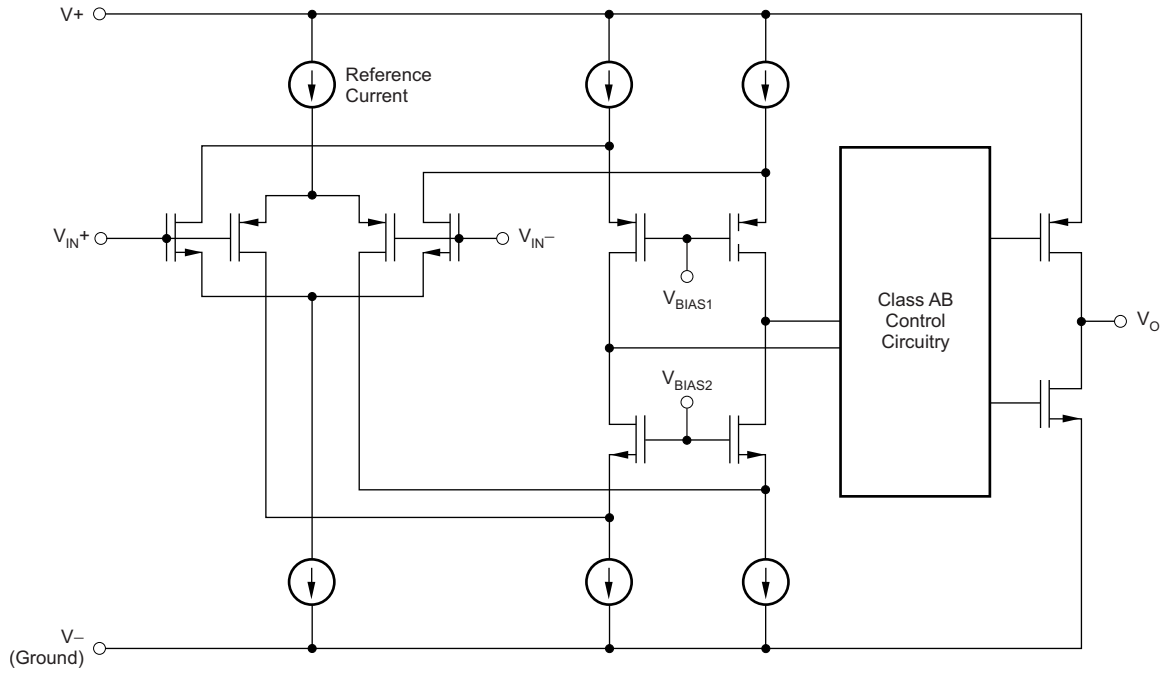
8 Detailed Description

8.1 Overview

The OPAx354 is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. It is available as a single, dual, or quad op amp.

The amplifier features a 100-MHz gain bandwidth, and 150-V/µs slew rate, but the amplifier is unity-gain stable and can operate as a 1-V/V voltage follower.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The OPAx354 is specified over a power-supply range of 2.7 V to 5.5 V (±1.35 V to ±2.75 V). However, the supply voltage may range from 2.5 V to 5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics section of this data sheet.*

8.3.2 Rail-to-Rail Input

The specified input common-mode voltage range of the OPAx354 extends 100 mV beyond the supply rails. This extended range is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.2 V to 100 mV above the positive supply, while the P-channel pair is on for inputs from 100 mV below the negative supply to approximately (V+) − 1.2 V. There is a small transition region, typically (V+) − 1.5 V to (V+) − 0.9 V, in which both pairs are on. This 600-mV transition region vary ±500 mV with process variation. Therefore, the transition region (both input stages on) range from (V+) − 2 V to (V+) − 1.5 V on the low end, up to (V+) − 0.9 V to (V+) − 0.4 V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

8.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors achieves rail-to-rail output. For high-impedance loads (> 200 Ω), the output voltage swing is typically 100 mV from the supply rails. With 10-Ω loads, a useful output swing is achieved while maintaining high open-loop gain. See the typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 20 and Figure 22).

8.3.4 Output Drive

The OPAx354 output stage supplies a continuous output current of ±100 mA and yet provide approximately 2.7 V of output swing on a 5-V supply, as shown in Figure 30. For maximum reliability, TI does not recommend running a continuous DC current in excess of ±100 mA. See the typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 20 and Figure 22). For supplying continuous output currents greater than ±100 mA, the OPAx354 may be operated in parallel, as shown in Figure 31.

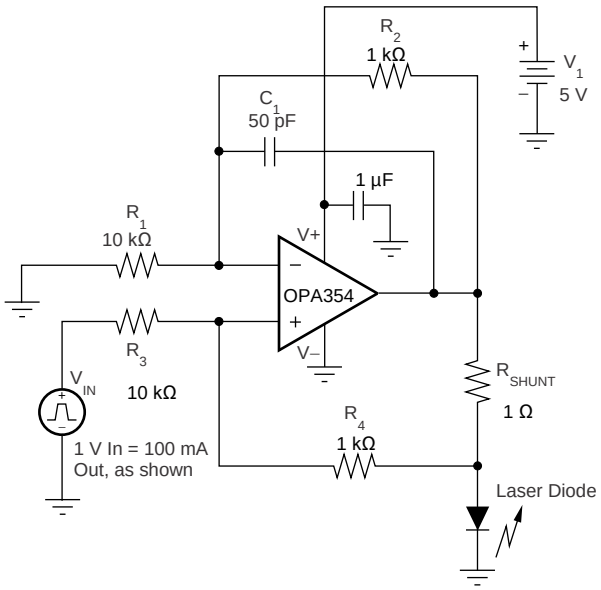


Figure 30. Laser Diode Driver

Feature Description (continued)

The OPAx354 provides peak currents up to 200 mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the OPAx354 from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

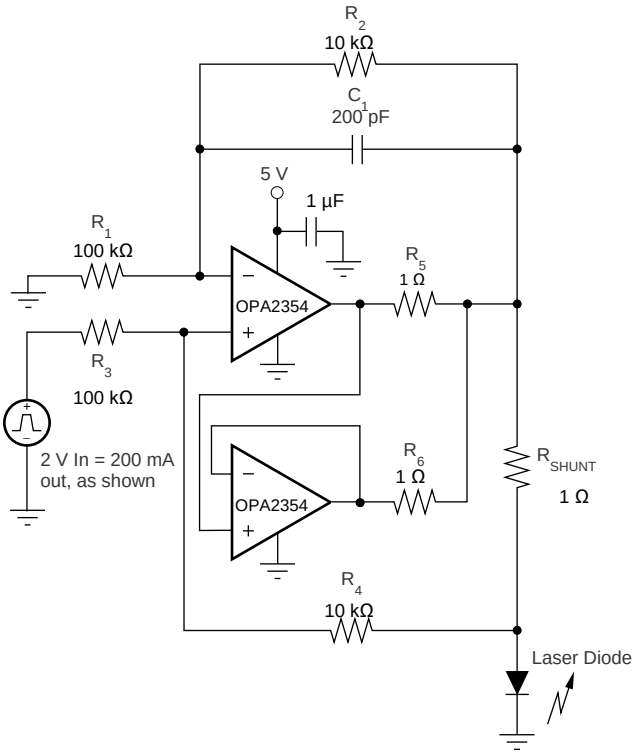


Figure 31. Parallel Operation

8.3.5 Video

The OPAx354 output stage is capable of driving standard back-terminated 75-Ω video cables, as shown in Figure 32. By back-terminating a transmission line, the output stage does not exhibit a capacitive load to the driver. A properly back-terminated 75-Ω cable does not appear as capacitance; the cable presents a 150-Ω resistive load to the OPAx354 output.

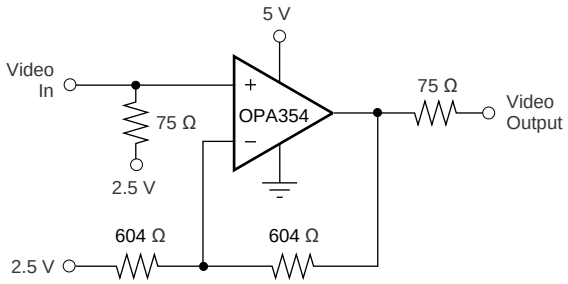
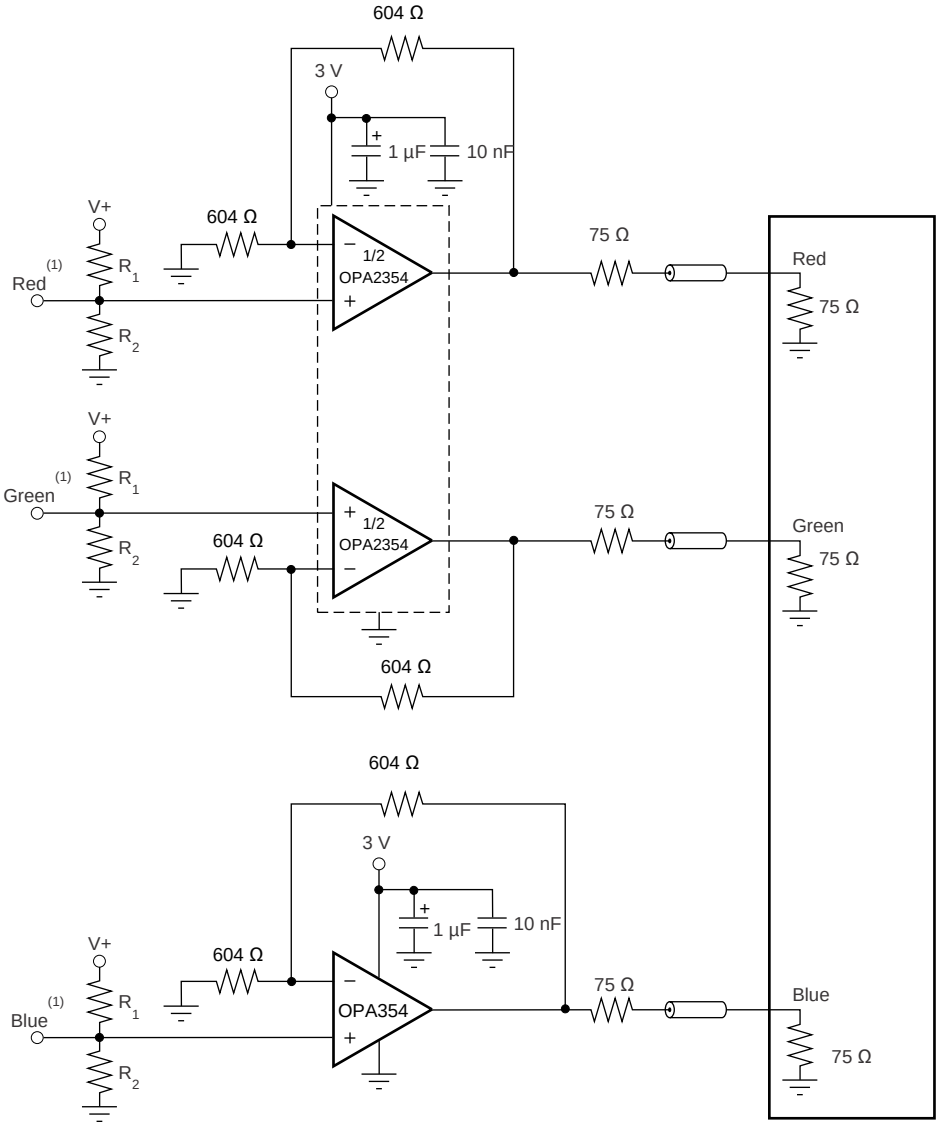


Figure 32. Single-Supply Video Line Driver

The OPAx354 is used as an amplifier for RGB graphic signals, which feature a voltage of zero at the video black level, by offsetting and AC-coupling the signal. See Figure 33.

Feature Description (continued)



(1) Source video signal offset 300 mV above ground to accommodate op amp swing−to−ground capability.

Figure 33. RGB Cable Driver

Feature Description (continued)

8.3.6 Driving Analog-to-Digital converters

The OPAx354 series op amps offer 60 ns of settling time to 0.01%, making the series a good choice for driving high- and medium-speed sampling A/D converters and reference circuits. The OPAx354 series provide an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain. For applications requiring high DC accuracy, the OPA350 series is recommended.

Figure 34 shows the OPAx354 driving an A/D converter. With the OPAx354 in an inverting configuration, a capacitor across the feedback resistor is used to filter high-frequency noise in the signal.

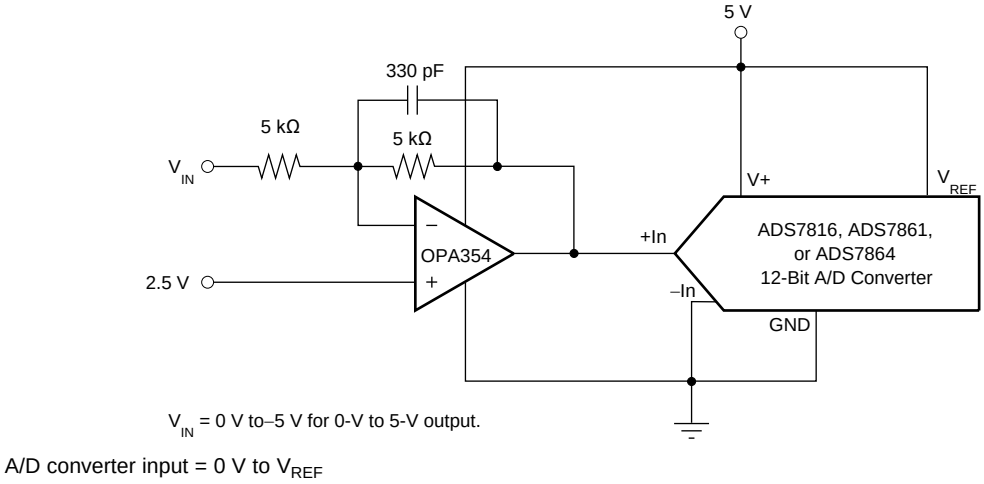


Figure 34. The OPAx354 in Inverting Configuration Driving the ADS7816

8.3.7 Capacitive Load and Stability

The OPAx354 series op amps drives a wide range of capacitive loads. However, all op amps may become unstable under certain conditions. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the device output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. See the *Frequency Response for Various C_L* typical characteristic curve (Figure 13) for details.

The OPAx354 topology enhances its ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. See the *Recommended R_S vs Capacitive Load* (Figure 14) and *Frequency Response vs Capacitive Load* (Figure 15) typical characteristic curves for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in Figure 35. This configuration significantly reduces ringing with large capacitive loads; see the *Frequency Response vs Capacitive Load* typical characteristic curve (Figure 15). However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This voltage division introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For instance, with R_L = 10 kΩ and R_S = 20 Ω, there is an error of approximately 0.2% at the output.

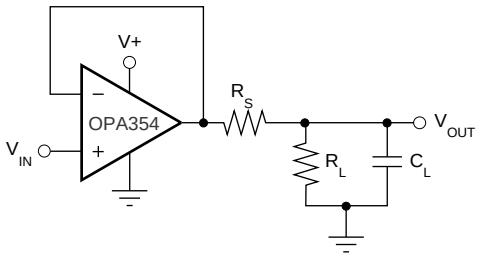


Figure 35. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

Feature Description (continued)

8.3.8 Wideband Transimpedance Amplifier

Wide bandwidth, low input bias current, low input voltage, and current noise make the OPAx354 a preferred wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design (as shown in Figure 36) are the expected diode capacitance [including the parasitic input common-mode and differential-mode input capacitance (2 + 2) pF for the OPAx354], the desired transimpedance gain (R_F), and the gain-bandwidth product (GBW) for the OPAx354 (100 MHz, typical). With these three variables set, the feedback capacitor value (C_F) may be set to control the frequency response.

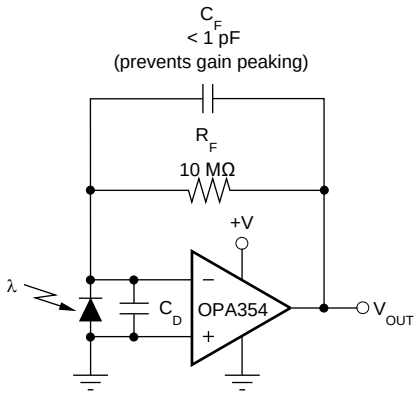


Figure 36. Transimpedance Amplifier

To achieve a maximally flat, second-order, Butterworth frequency response, the feedback pole must be set as shown in Equation 1:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2 pF that must be deducted from the calculated feedback capacitance value. Bandwidth is calculated by Equation 2:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \text{ Hz} \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA355 (200-MHz GBW) or the OPA655 (400-MHz GBW) may be used.

8.4 Device Functional Modes

The OPAx354 family of devices is powered on when the supply is connected. The devices can operate as single-supply operational amplifiers or dual-supply amplifiers depending on the application. The devices are used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (example: V– set to –3.5 V and V+ set to 1.5 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx354 family of devices is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The OPAx354 family of devices is available as a single, dual, or quad op amp. The amplifier features a 100-MHz gain bandwidth, and 150-V/µs slew rate, but it is unity-gain stable and operates as a 1-V/V voltage follower.

9.2 Typical Application

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAx354 family of devices an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency. The key elements to a transimpedance design, as shown in Figure 37, are the expected diode capacitance, (which include the parasitic input common-mode and differential-mode input capacitance) the desired transimpedance gain, and the gain-bandwidth (GBW) for the OPAx354 family of devices (20 MHz). With these three variables set, the feedback capacitor value is set to control the frequency response. Feedback capacitance includes the stray capacitance , which is 0.2 pF for a typical surface-mount resistor.

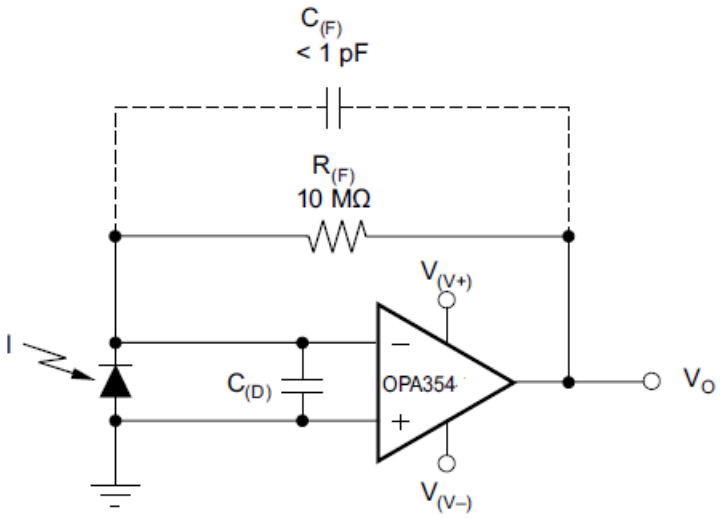


Figure 37. Dual-Supply Transimpedance Amplifier

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply voltage, $V_{(V+)}$	2.5 V
Supply voltage, $V_{(V-)}$	–2.5 V

$C_{(F)}$ is optional to prevent gain peaking. $C_{(F)}$ includes the stray capacitance of $R_{(F)}$.

9.2.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, set the feedback pole using Equation 3.

$$\frac{1}{2 \times \pi \times R_{(F)} \times C_{(F)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (3)$$

Calculate the bandwidth using Equation 4.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(F)} \times C_{(D)}}} \quad (4)$$

9.2.2.1 Optimizing the Transimpedance Circuit

To achieve the best performance, components must be selected according to the following guidelines:

1. For lowest noise, select $R_{(F)}$ to create the total required gain. Using a lower value for $R_{(F)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(F)}$ increases with the square-root of $R_{(F)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.

2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.

3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only the required bandwidth. Use a capacitor across the $R_{(F)}$ to limit bandwidth, even if a capacitor not required for stability.

4. Circuit board leakage degrades the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage helps control leakage.

9.2.3 Application Curve

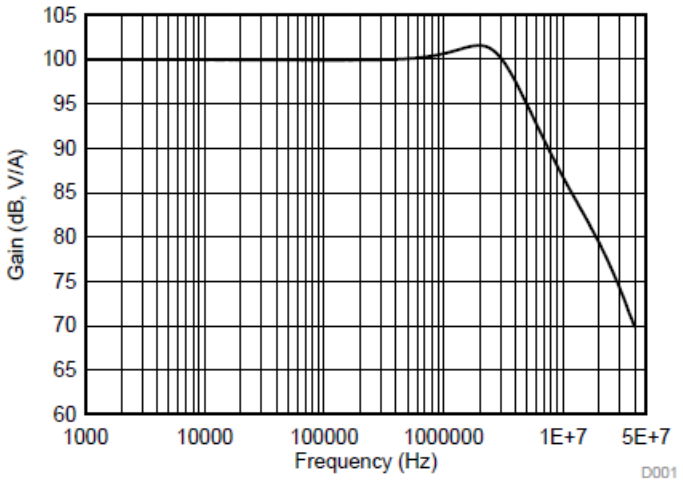


Figure 38. AC Transfer Function

10 Power Supply Recommendations

The OPAx354 family of devices is specified for operation from 2.5 V to 5.5 V (±1.25 to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that exhibit significant variance with regard to operating voltage or temperature are shown *Typical Characteristics*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section..

11 Layout

11.1 Layout Guidelines

Good high-frequency printed-circuit board (PCB) layout techniques must be employed for the OPAx354. Generous use of ground planes, short and direct signal traces, and a suitable bypass capacitor located at the V+ pin ensure clean, stable operation. Large areas of copper provides a means of dissipating heat that is generated in normal operation.

TI does not recommend using sockets with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1-µF or larger tantalum capacitor in parallel is beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving low harmonic and intermodulation distortion.

11.2 Layout Example

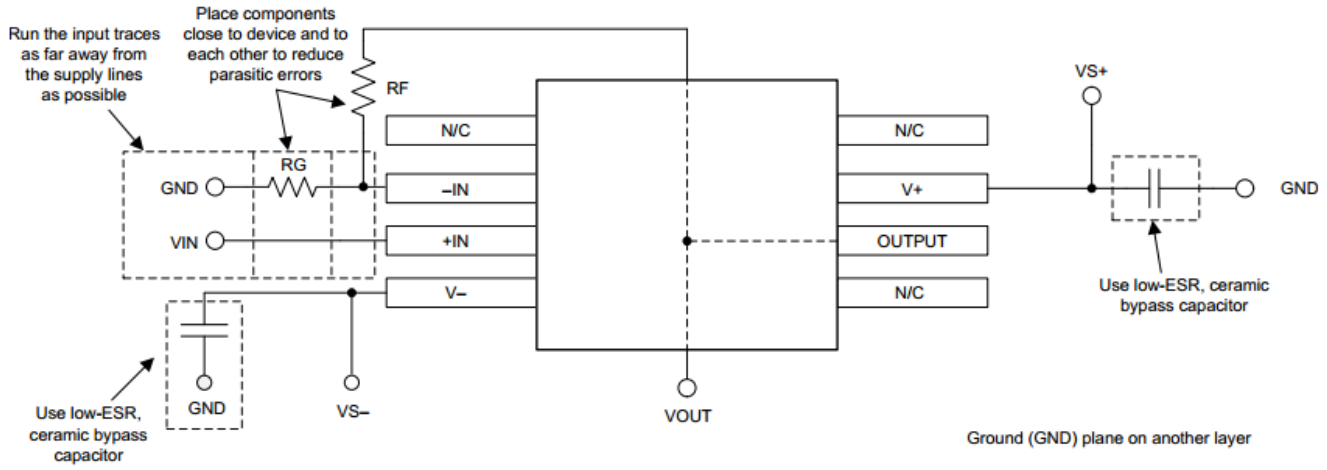


Figure 39. Operational Amplifier Board Layout for Noninverting Configuration

11.3 Power Dissipation

Power dissipation depends on power-supply voltage, signal and load conditions. With DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor, $V_S - V_O$. Power dissipation is minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. AB-039 *Power Amplifier Stress and Power Handling Limitations* explains how to calculate or measure power dissipation with unusual signals and loads See www.ti.com for more details.

Power Dissipation (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 150°C (maximum.) To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at 160°C. The thermal protection must trigger more than 35°C above the maximum expected ambient condition of the application.

11.4 PowerPAD Thermally-Enhanced Package

In addition to the regular 5-pin SOT-23 and 9-pin VSSOP packages, the single and dual versions of the OPAx354 also come in an 8-pin SOIC PowerPAD package. The 98-pin SO with PowerPAD is a standard size 8-pin SOIC package where the exposed leadframe on the bottom of the package is soldered directly to the PCB to create a low thermal resistance. This direct attachment enhances the OPAx354 power dissipation capability significantly, and eliminates the use of bulky heat sinks and slugs that are traditionally used in thermal packages. This package is easily mounted using standard PCB assembly techniques.

NOTE

Because the 8-pin HSOP PowerPAD is pin-compatible with standard 8-pin SOIC packages, the OPA354 and OPA2354 can directly replace operational amplifiers in existing sockets. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. This configuration provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the device, as shown in Figure 40. This exposed die provides an extremely low thermal resistance ($R_{\theta JC}$) path between the die and the exterior of the package. The thermal pad on the bottom of the device can then be soldered directly to the PCB, using the PCB as a heat sink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.

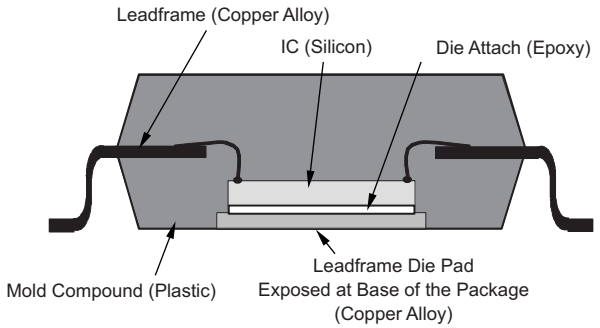


Figure 40. Section View of a PowerPAD Package

11.5 PowerPAD Assembly Process

The PowerPAD must be connected to the most negative supply voltage for the device, which is ground in single-supply applications and V− in split-supply applications.

Prepare the PCB with a top-side etch pattern, as shown in Figure 41. The exact land design may vary based on the specific assembly process requirements. There must be etch for the leads and etch for the thermal land.

Place the recommended number of plated-through holes (or thermal vias) in the area of the thermal pad. These holes must be 13 mils (.013 in) in diameter. The holes are small so that solder wicking through the holes is not a problem during reflow. TI recommends a minimum of five holes for the 8-pin HSOP PowerPAD package, as shown in Figure 41.

PowerPAD Assembly Process (continued)

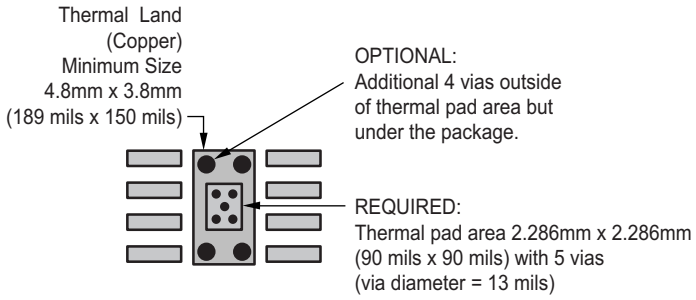


Figure 41. 8-Pin PowerPAD PCB Etch and Via Pattern

TI recommends, but does not require, placing a small number of additional holes under the package and outside the thermal pad area. These holes provide additional heat paths between the copper thermal land and the ground plane. The holes may be larger because the holes are not in the area to be soldered, so wicking is not a problem. This technique is shown in Figure 41.

Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane for single-supply applications, and to V− for split-supply applications.

When laying out these holes, do not use the typical web or spoke via connection methodology, as shown in Figure 42. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This feature makes soldering the vias that have ground plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package must make connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

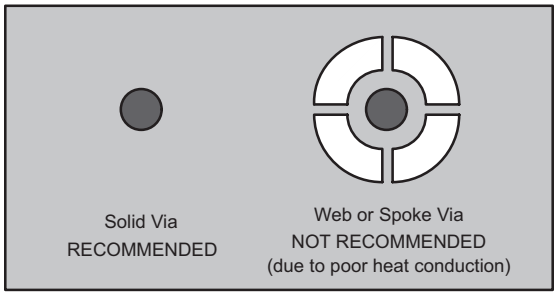


Figure 42. Via Connection

The top-side solder mask must leave the pad connections and the thermal pad area exposed. The thermal pad area must leave the 13-mil holes exposed. The larger holes outside the thermal pad area may be covered with a solder mask.

Apply solder paste to the exposed thermal pad area and all of the package pins.

With these preparatory steps in place, the PowerPAD device is placed in position and run through the solder reflow operation as any standard surface-mount component. This preparation and processing results in a part that is properly installed.

For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see *PowerPAD Thermally Enhanced Package* on www.ti.com.

12 Device and Documentation Support

12.1 Documentation Support

For related documentation see the following:

- Texas Instruments, *ADS8326 16-Bit, High-Speed, 2.7V to 5.5V microPower Sampling ANALOG-TO-DIGITAL CONVERTER*
- Texas Instruments, *Circuit Board Layout Techniques*
- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively*
- Texas Instruments, *FilterPro™ User's Guide*
- Texas Instruments, *Noise Analysis for High-Speed Op Amps*
- Texas Instruments, *OPA380 and OPA2380 Precision, High-Speed Transimpedance Amplifier*
- Texas Instruments, *OPA355, OPA2355, and OPA3355 200MHz, CMOS OPERATIONAL AMPLIFIER WITH SHUTDOWN*
- Texas Instruments, *OPA656 Wideband, Unity-Gain Stable, FET-Input OPERATIONAL AMPLIFIER*
- Texas Instruments, *POWER AMPLIFIER STRESS AND POWER HANDLING LIMITATIONS*
- Texas Instruments, *PowerPAD Thermally Enhanced Package*

12.2 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA354	Click here	Click here	Click here	Click here	Click here
OPA2354	Click here	Click here	Click here	Click here	Click here
OPA4354	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2354AIDDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	Samples
OPA2354AIDDAG3	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	Samples
OPA2354AIDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	Samples
OPA2354AIDDARG3	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	OPA 2354A	Samples
OPA2354AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	Samples
OPA2354AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	Samples
OPA2354AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OACI	Samples
OPA354AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	Samples
OPA354AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	Samples
OPA354AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OABI	Samples
OPA354AIDDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A	Samples
OPA354AIDDAG3	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A	Samples
OPA354AIDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	OPA 354A	Samples
OPA4354AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	Samples
OPA4354AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4354A	Samples
OPA4354AIPWR	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	Samples
OPA4354AIPWRG4	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	Samples
OPA4354AIPWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 4354A	Samples

PACKAGE OPTION ADDENDUM

10-Dec-2020

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(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA4354 :

- Automotive: OPA4354-Q1

NOTE: Qualified Version Definitions:

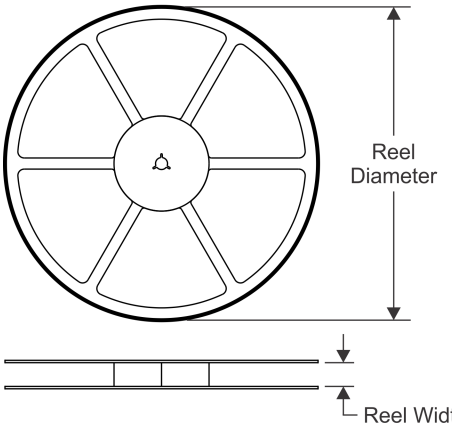
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

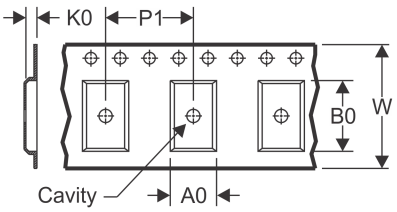
30-Dec-2020

TAPE AND REEL INFORMATION

REEL DIMENSIONS

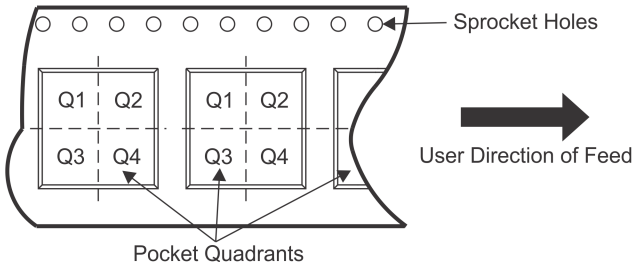


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



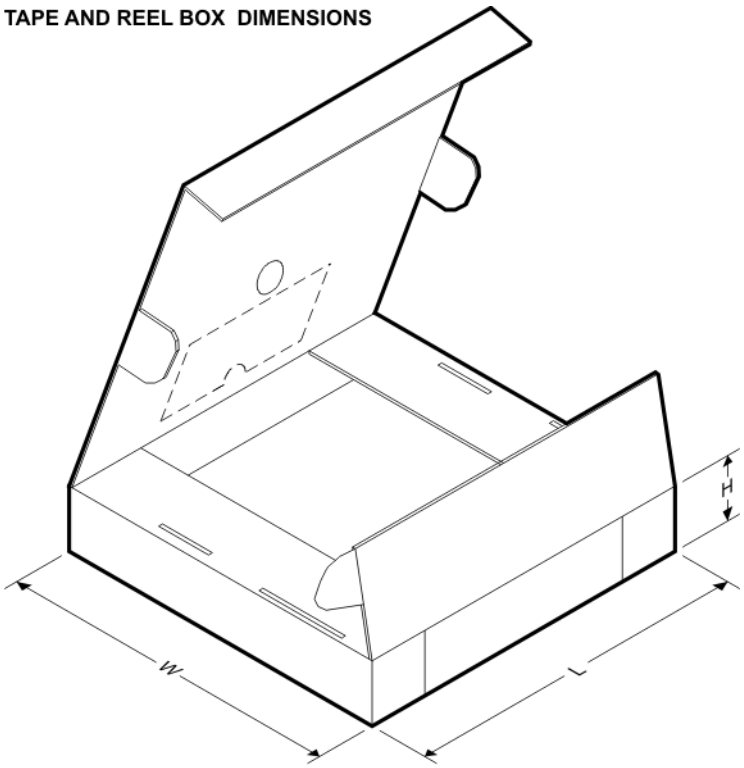
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2354AIDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2354AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2354AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA354AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA354AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA354AIDDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4354AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4354AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4354AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

30-Dec-2020

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

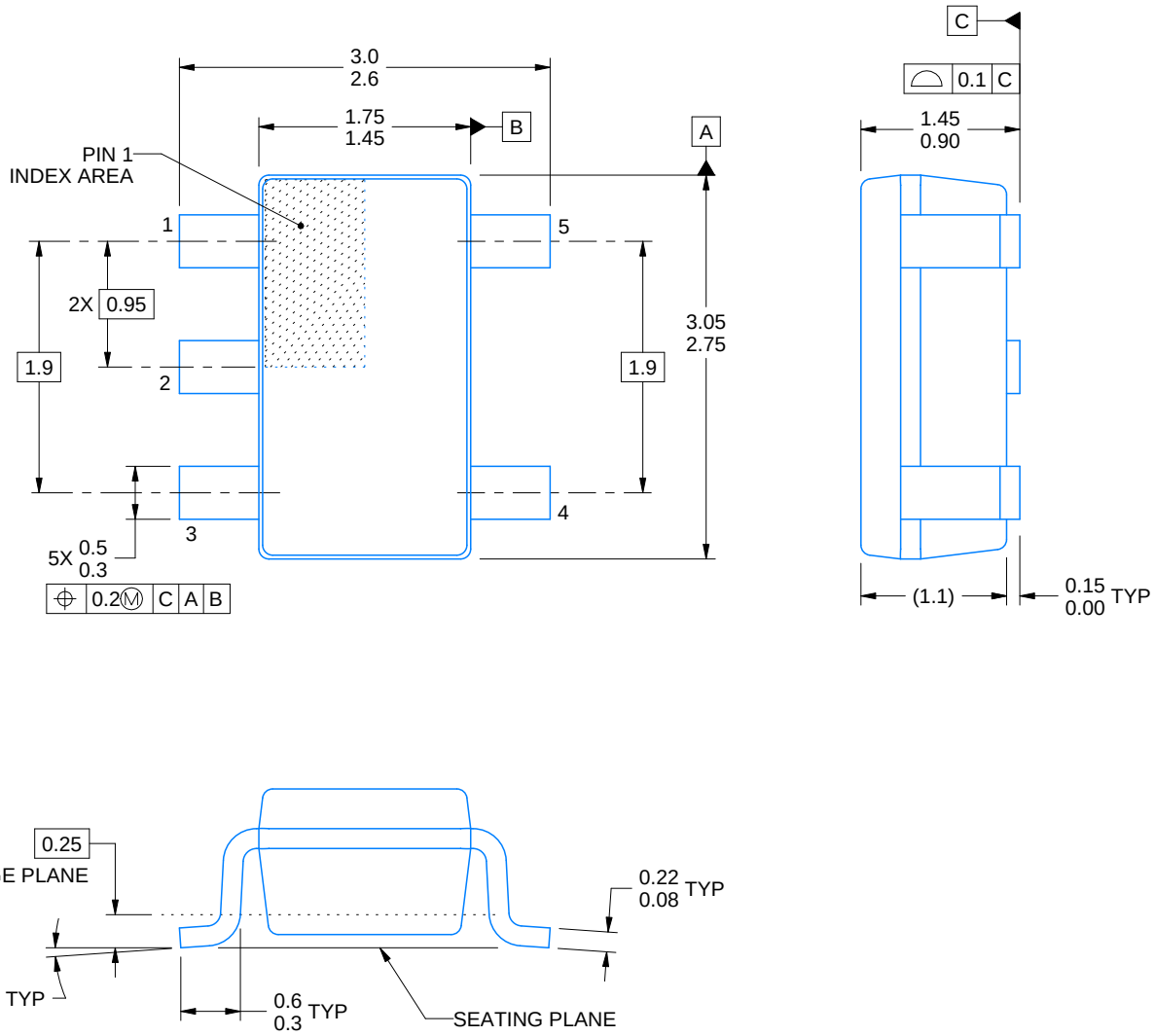
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2354AIDDAR	SO PowerPAD	DDA	8	2500	853.0	449.0	35.0
OPA2354AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2354AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA354AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA354AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA354AIDDAR	SO PowerPAD	DDA	8	2500	853.0	449.0	35.0
OPA4354AIDR	SOIC	D	14	2500	853.0	449.0	35.0
OPA4354AIPWR	TSSOP	PW	14	2500	853.0	449.0	35.0
OPA4354AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

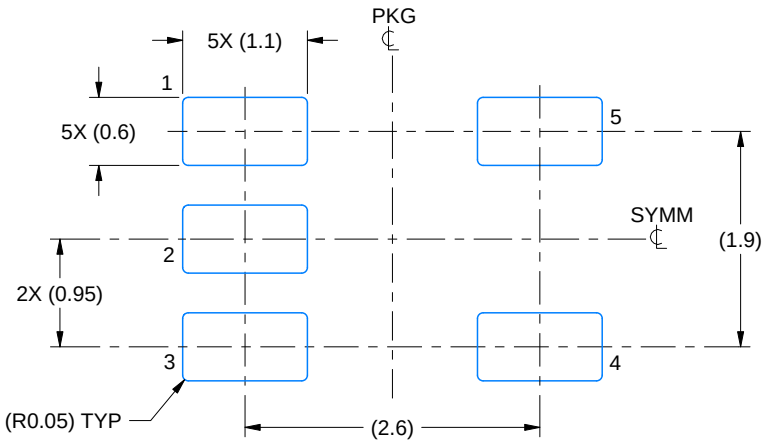
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

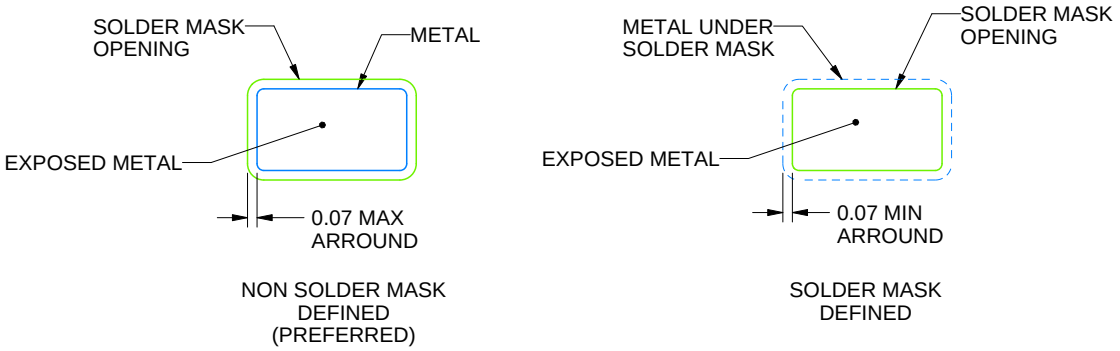
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

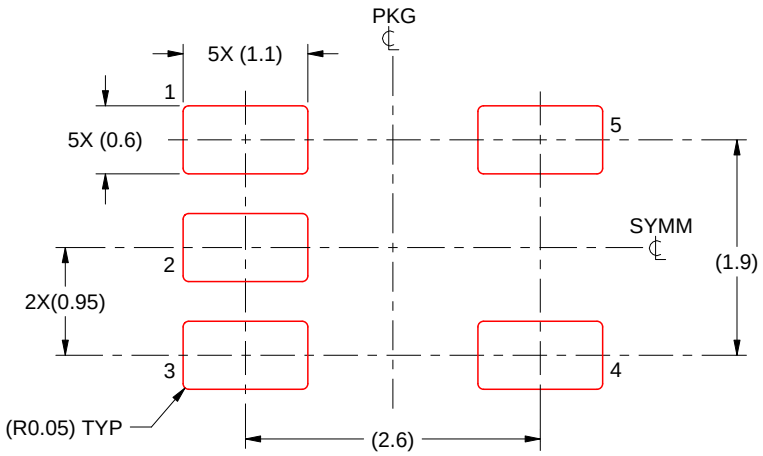
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



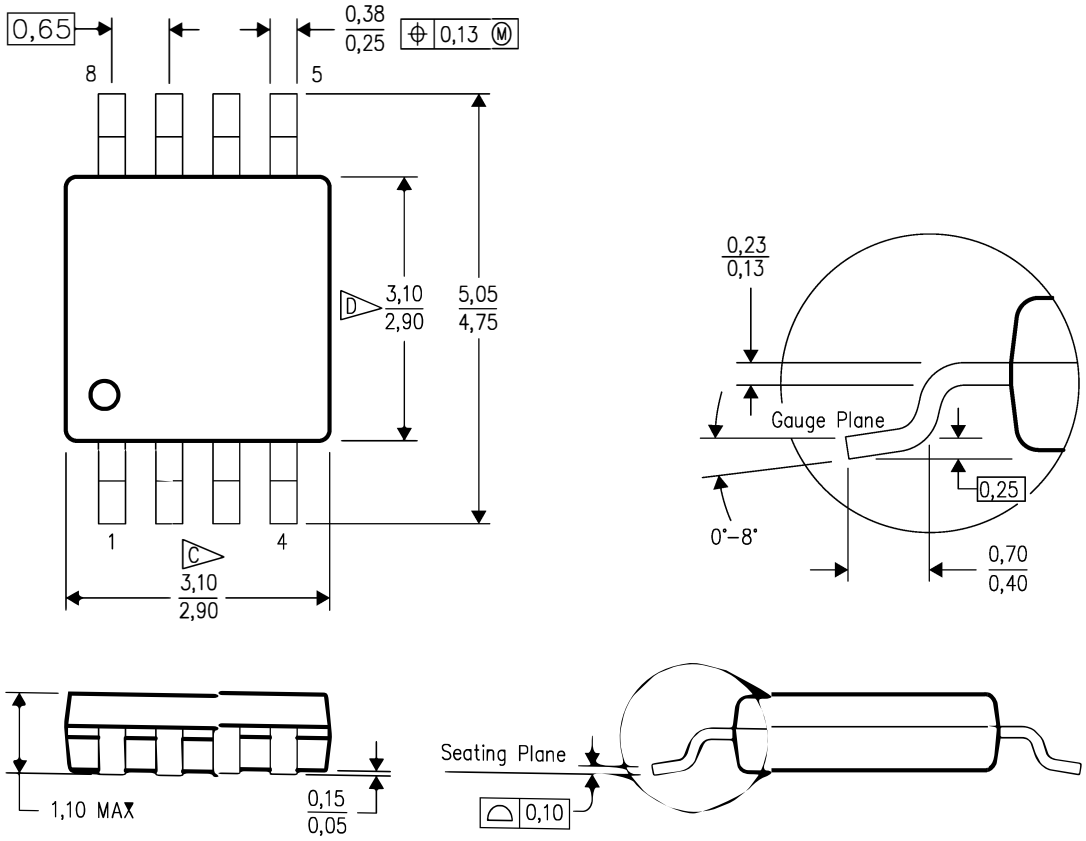
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

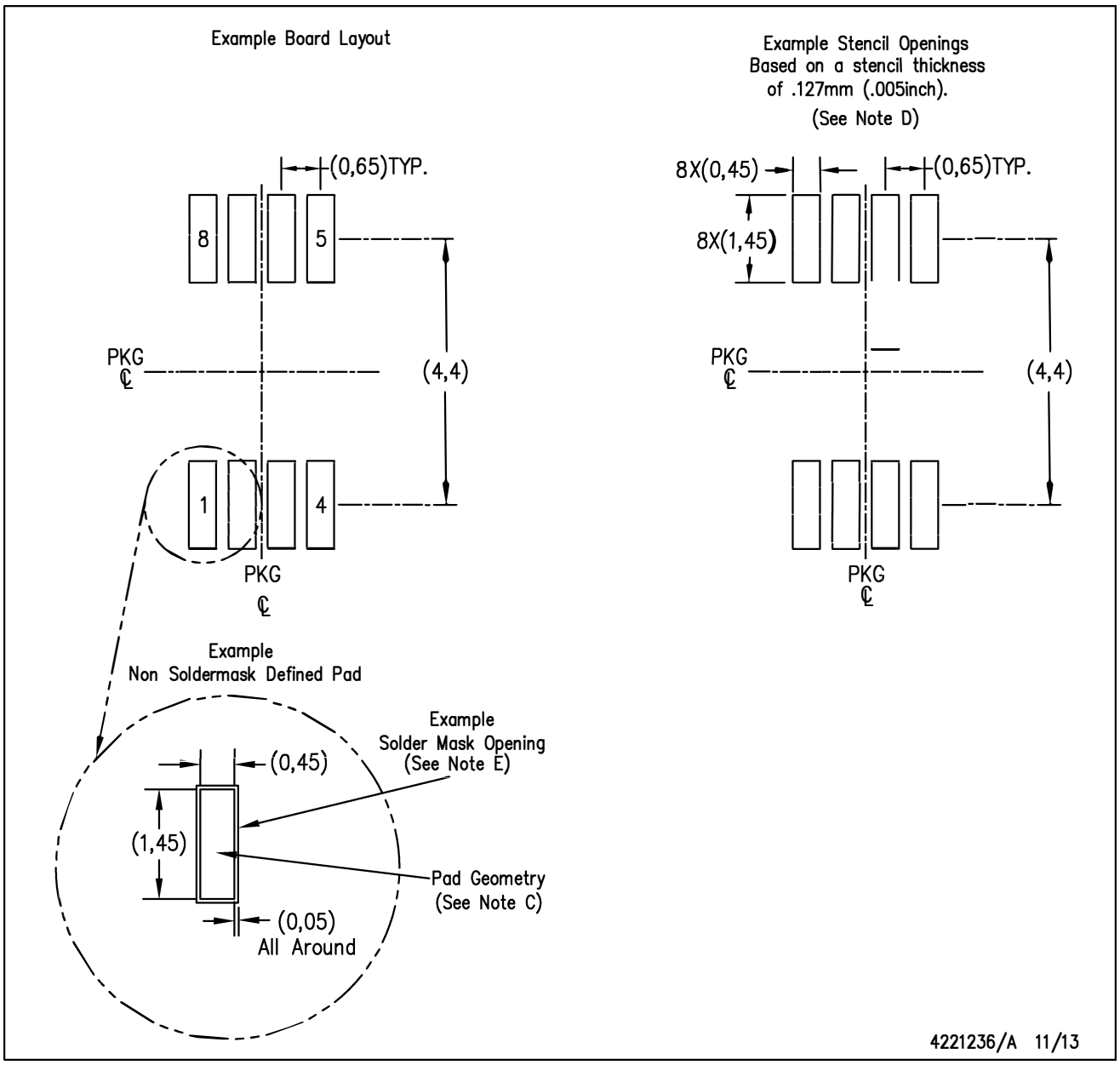
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE

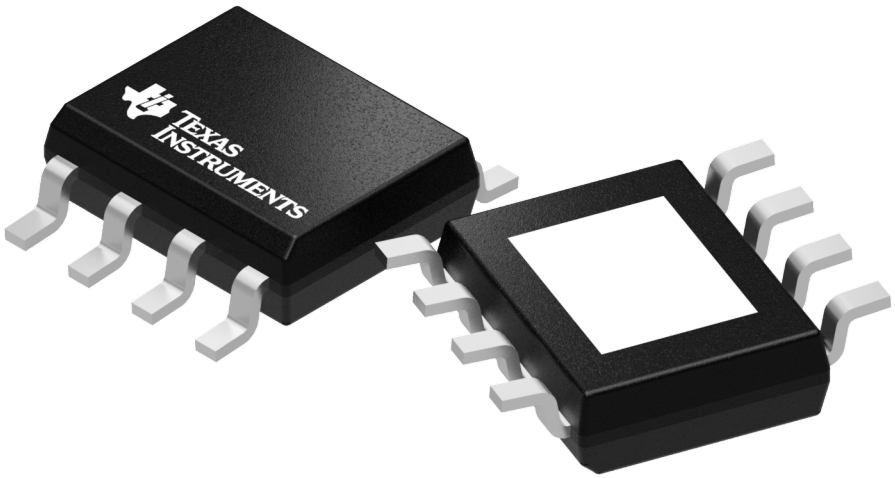


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

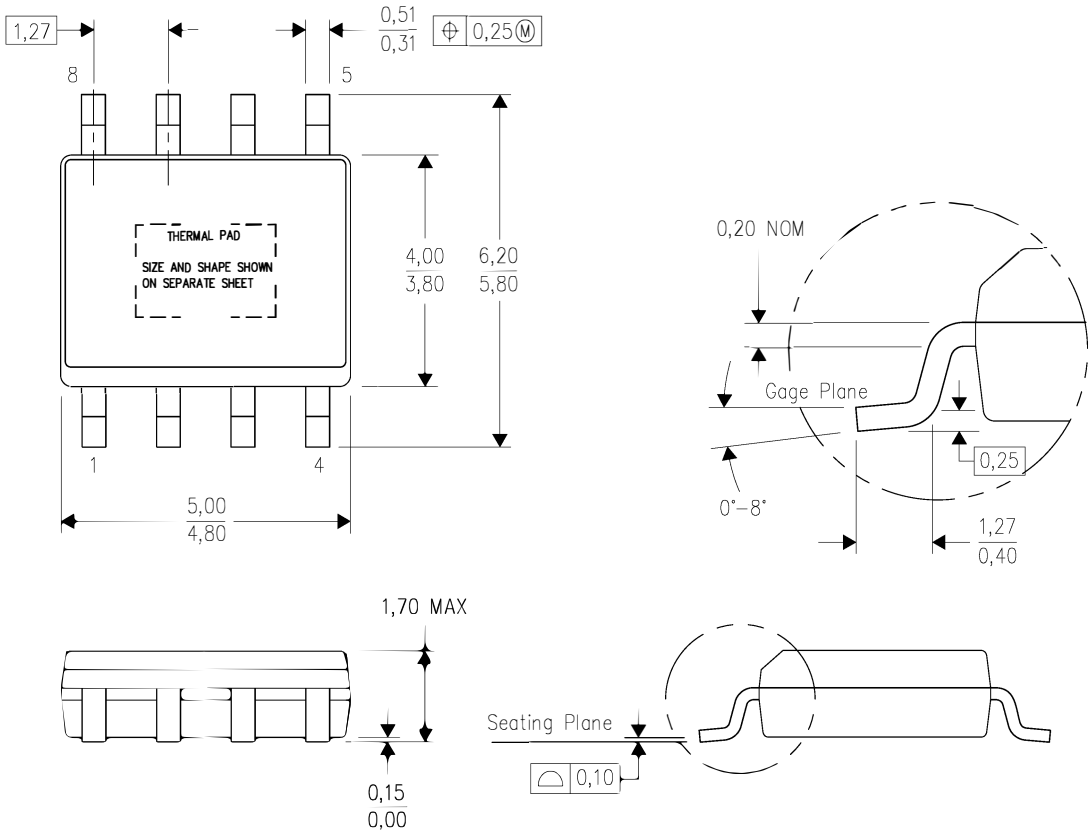
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

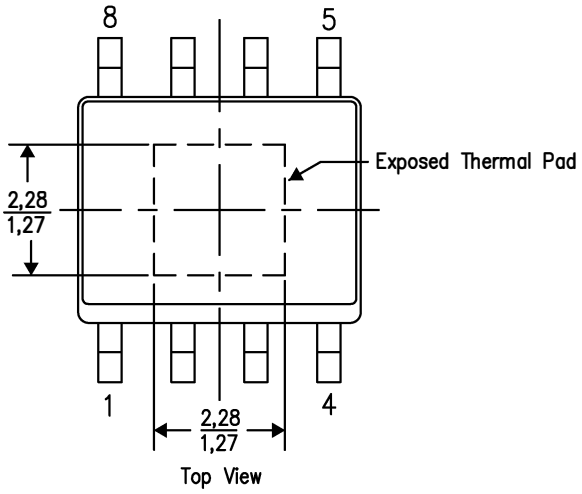
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



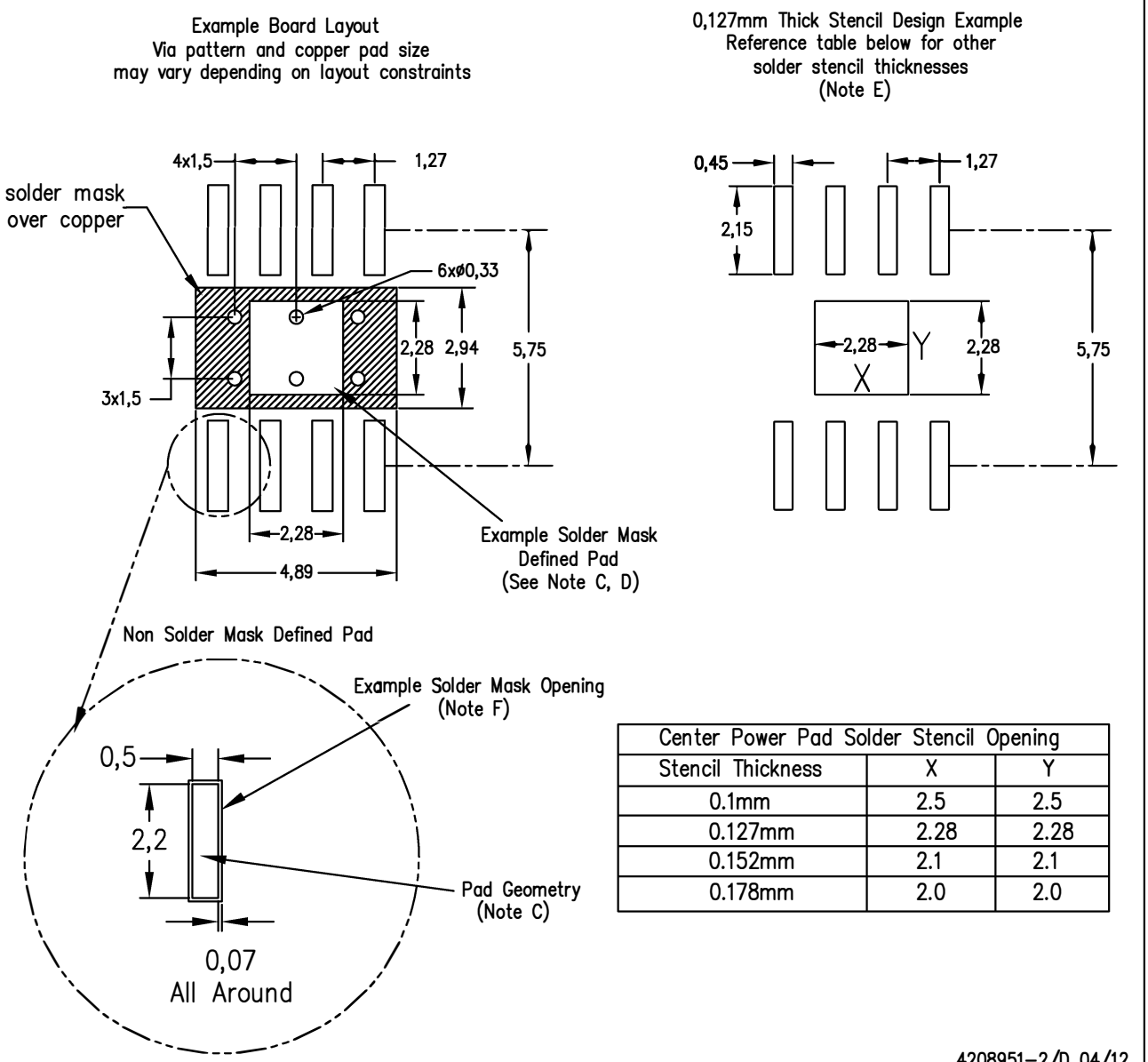
Exposed Thermal Pad Dimensions

4206322–2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

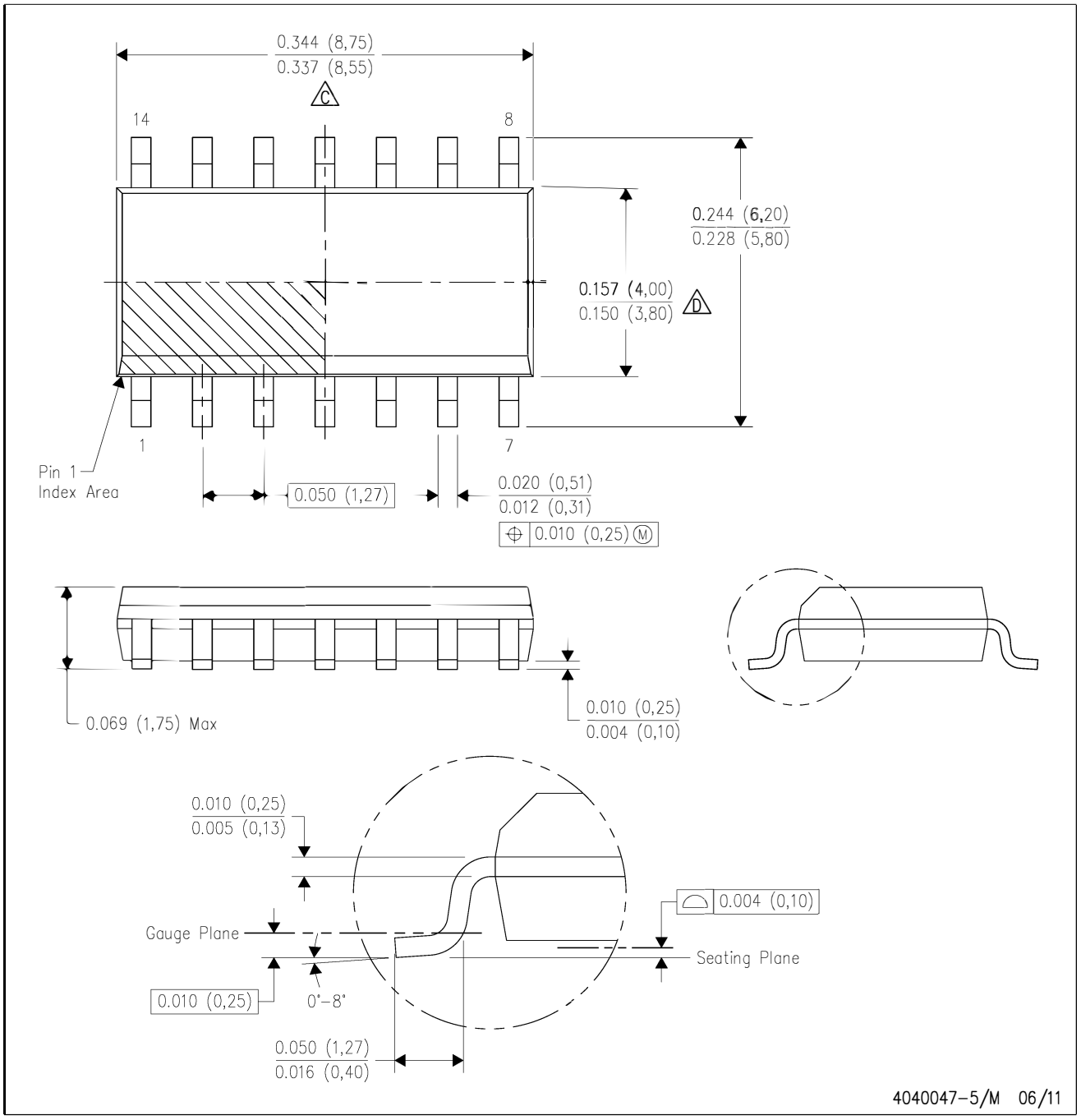
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.5
0.127mm	2.28	2.28
0.152mm	2.1	2.1
0.178mm	2.0	2.0

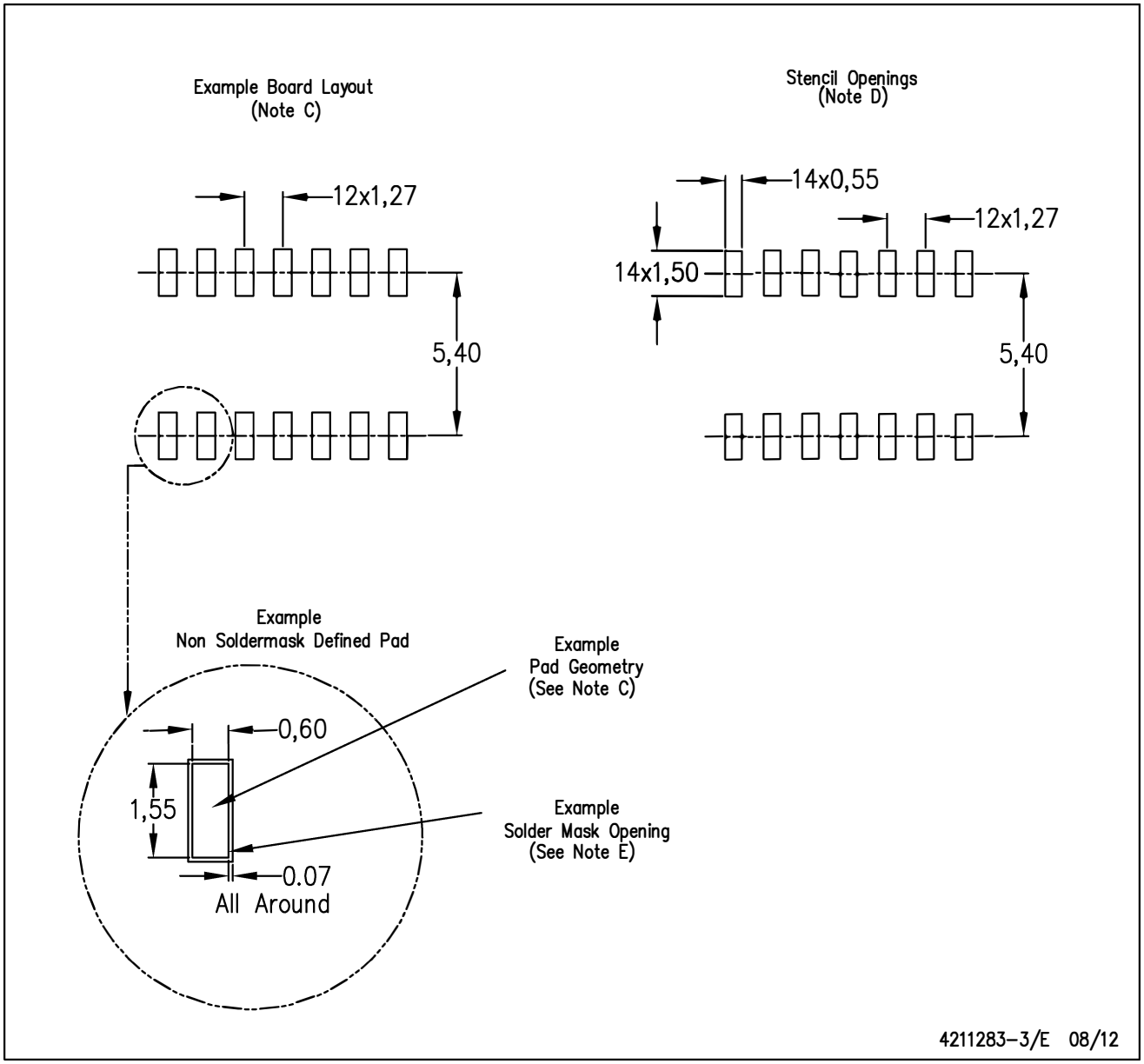
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



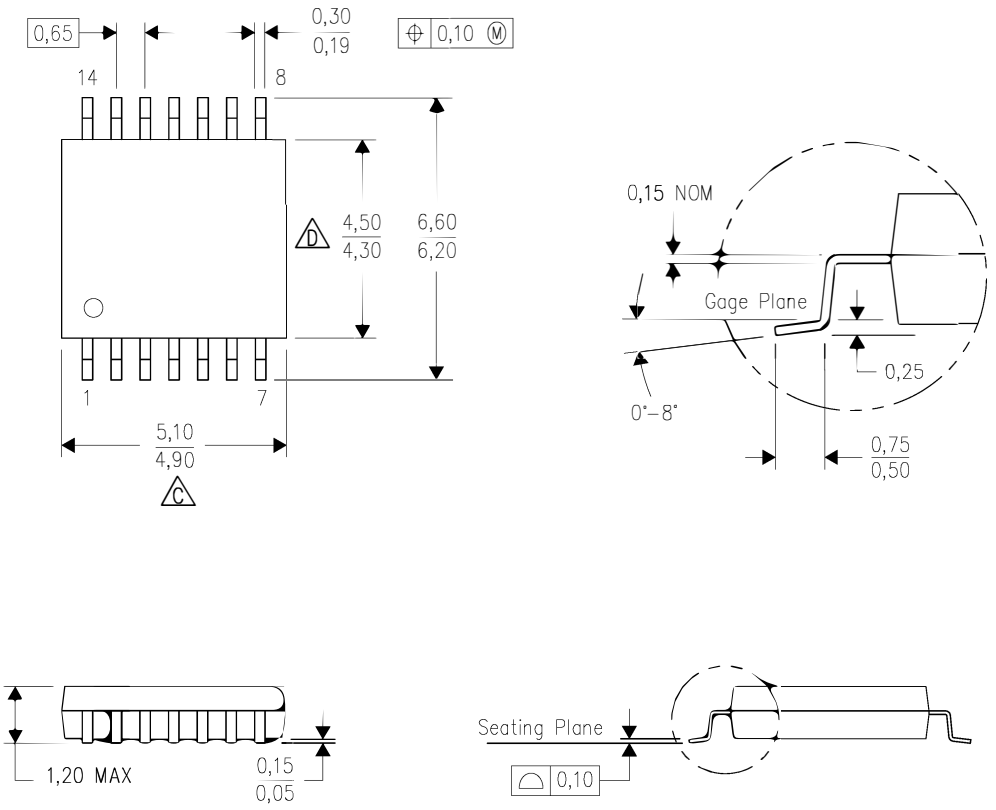
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

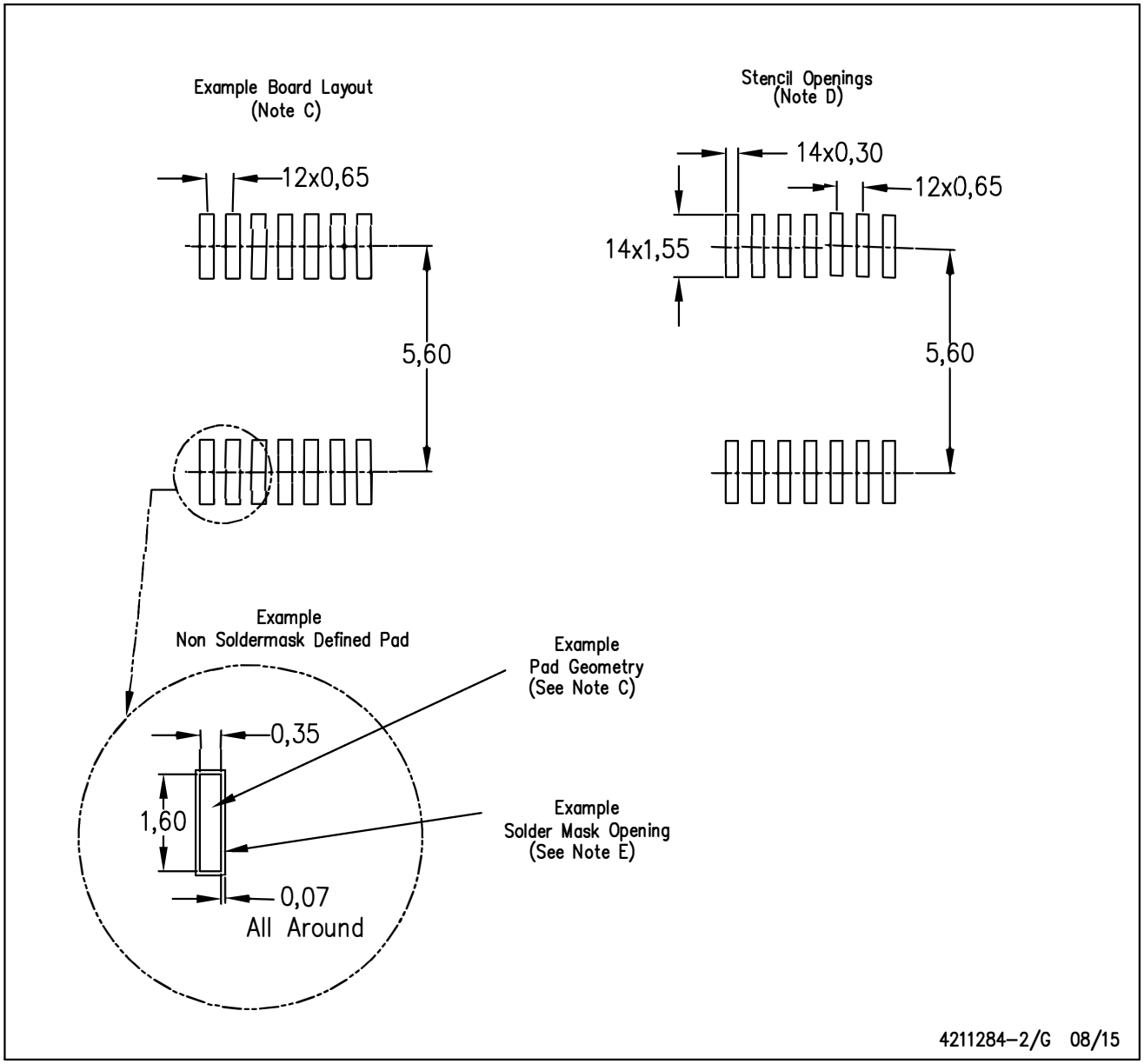
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.