

Triple DC-DC Boost Converter for AMOLED

General Description

The RT4722C is a triple channels DC-DC converter which is designed to provide the power of AMOLED. It integrates step up DC-DC and an inverting converter to provide the positive and negative output voltage required by AMOLED.

For the portable application, board space and efficiency are always major concerns. The high switching frequency of the RT4722C allows the use of low inductance inductor to save the board space. For the negative and AVDD output voltage, both can be programmed by external MCU through single wire (SWIRE pin). The output voltage range of negative output voltage is $-1.4V$ to $-5.4V$ and AVDD voltage is $5.8V$ to $7.9V$. RT4722C has OTP, SCP, UVLO and over-current protections. The RT4722C is available in a WQFN-16L 3x3 package to achieve saving PCB space.

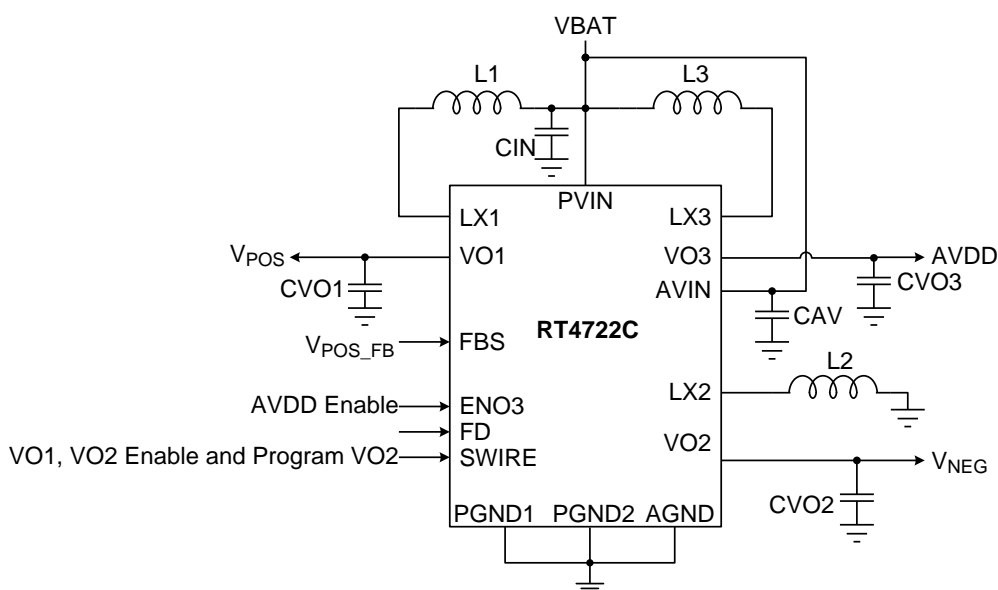
Applications

- AMOLED Panel
- PDAs and Smart Phones
- Probable Instrument

Features

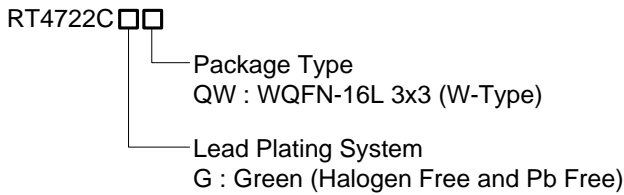
- Boost Converter to Supply Positive AVDD Voltage from $5.8V$ to $7.9V$
- Boost Converter to Supply AMOLED Positive Voltage $4.6V$
- Inverter Converter to Supply AMOLED Negative Voltage from $-1.4V$ to $-5.4V$
- Maximum Output Current up to $300mA$ for AMOLED Positive & Negative Power Supply
- Maximum Output Current up to $55mA$ for AVDD Output Voltage
- Typical Peak Efficiency : $90%$ ($40mA$ to $150mA$)
- PWM Mode @ $1.5MHz$ Switching Frequency
- High Output Voltage Accuracy
- Excellent Line and Load Transient
- Excellent Line and Load Regulation
- Programmable Negative and AVDD Voltage by SWIRE Pin
- Fast Outputs Discharge Function
- Low Quiescent Current $< 1\mu A$ in Shutdown Mode
- Internal Soft-Start to limit Inrush Current
- Over-Temperature Protection (OTP)
- Over-Current Protection (OCP)
- Short Circuit Protection (SCP)

Simplified Application Circuit



RT4722C

Ordering Information



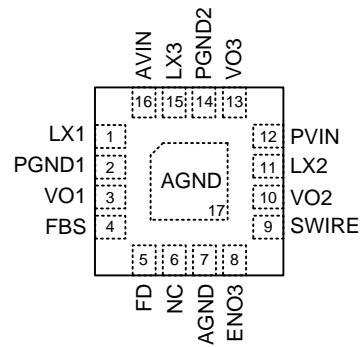
Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

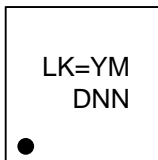
Pin Configuration

(TOP VIEW)



WQFN-16L 3x3

Marking Information

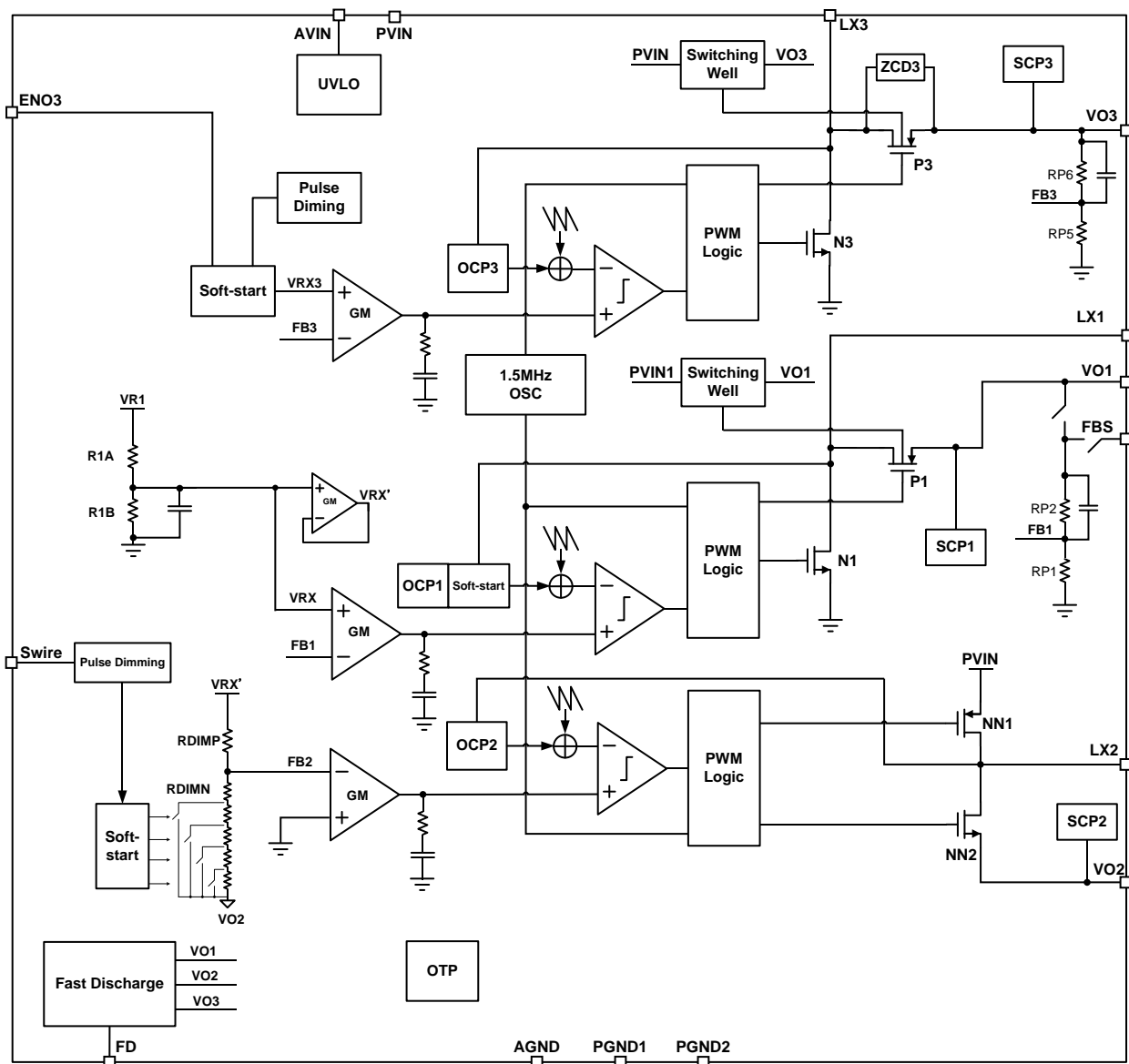


LK= : Product Code
YMDNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	LX1	1 st boost converter switching node.
2	PGND1	Power ground.
3	VO1	1 st boost converter output.
4	FBS	1 st boost converter output feedback sense. Connect to VO1 pin if un-used.
5	FD	Active discharge enable/disable during shutdown. Default floating.
6	NC	No connected.
7, 17 (Exposed Pad)	AGND	Signal ground. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation.
8	ENO3	2 nd boost enable/disable pin.
9	SWIRE	VPOS, VNEG control pin (enable/disable pin).
10	VO2	Buck/Boost converter output (negative voltage).
11	LX2	Buck/Boost converter switching node.
12	PVIN	Power input voltage.
13	VO3	2 nd boost converter output.
14	PGND2	Power ground.
15	LX3	2 nd boost converter switching node.
16	AVIN	Analog input voltage.

Functional Block Diagram



Operation

The RT4722C is a triple channels DC-DC converter which is designed to provide the power of AMOLED that can support the input voltage range from 2.9V to 4.5V. The VO1 & VO2 output current can be up to 300mA, and the VO3 output current can be up to 55mA. The RT4722C uses current mode architecture for the purpose of high efficiency and high transient response. The VO1 positive output voltage is produced from the DC-DC Boost converter and is set at a typical value of 4.6V. When the SWIRE goes high, the positive output voltage will be enabled with an internal soft-start

process. The VO2 negative output voltage is produced from the DC-DC Buck-Boost converter and the negative output voltage range is $-1.4V$ to $-5.4V$. It can be programmed by external MCU through single wire (SWIRE pin). The VO3 positive output voltage is produced from the DC-DC Boost converter and is set from 5.8V to 7.9V by SWIRE pin. When SWIRE goes high and VO1 soft-start had finished already, negative output voltage VO2 will be enabled with an internal soft-start process.

Table 1. SWIRE Command LUT for VO2

Bit (Pulse)	VNEG (V)	Bit (Pulse)	VNEG (V)	Bit (Pulse)	AVDD (V)
0	-4 (Default)	21	-3.4	0	6.1 (Default)
1	-5.4	22	-3.3	42	7.9
2	-5.3	23	-3.2	43	7.6
3	-5.2	24	-3.1	44	7.3
4	-5.1	25	-3	45	7
5	-5	26	-2.9	46	6.7
6	-4.9	27	-2.8	47	6.4
7	-4.8	28	-2.7	48	6.1
8	-4.7	29	-2.6	49	5.8
9	-4.6	30	-2.5		
10	-4.5	31	-2.4		
11	-4.4	32	-2.3		
12	-4.3	33	-2.2		
13	-4.2	34	-2.1		
14	-4.1	35	-2		
15	-4	36	-1.9		
16	-3.9	37	-1.8		
17	-3.8	38	-1.7		
18	-3.7	39	-1.6		
19	-3.6	40	-1.5		
20	-3.5	41	-1.4		

Table 2. SWIRE Pin Characteristics

Rating	Symbol	Min	Typ	Max	Unit
Initial Waiting Time	twait_int	--	50	--	μs
Signal Stop Indicate Time	tstop	100	--	--	μs
Turn-off Detection Time	toff_dly	30	--	80	μs
SWIRE Rising Time	tr	--	--	200	ns
SWIRE Falling Time	tf	--	--	200	ns
Clock SWIRE High	tsH	2	10	20	μs
Clock SWIRE Low	tsL	2	10	20	μs
Input SWIRE Frequency	fswire	25	--	250	kHz

Table 3. Fast Discharge Selection

SWIRE (Pulse)	FD Pin	Discharge	Note
0	High	ON	FD Control
	Low	OFF	
50	High	ON	SWIRE Control
	Low	ON	
51	High	OFF	SWIRE Control
	Low	OFF	

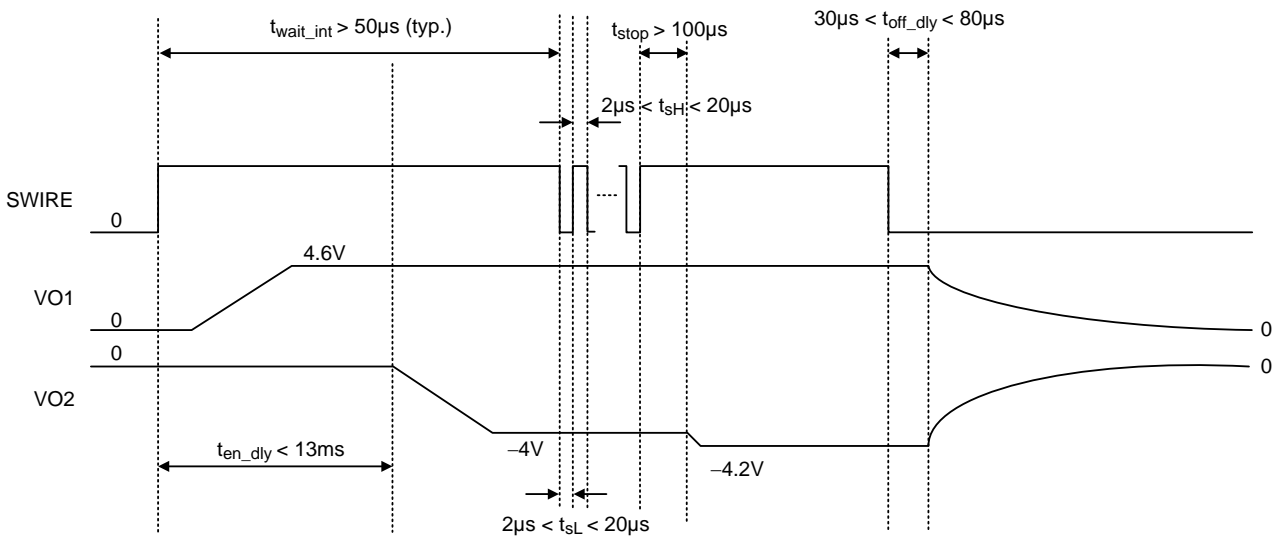
Table 4. Control of Transient Time

CTRL (Pulse)	Step Voltage per 100mV (mV)	Note
0	0	No Division Change
52	50	2 Division Change
53	25	4 Division Change

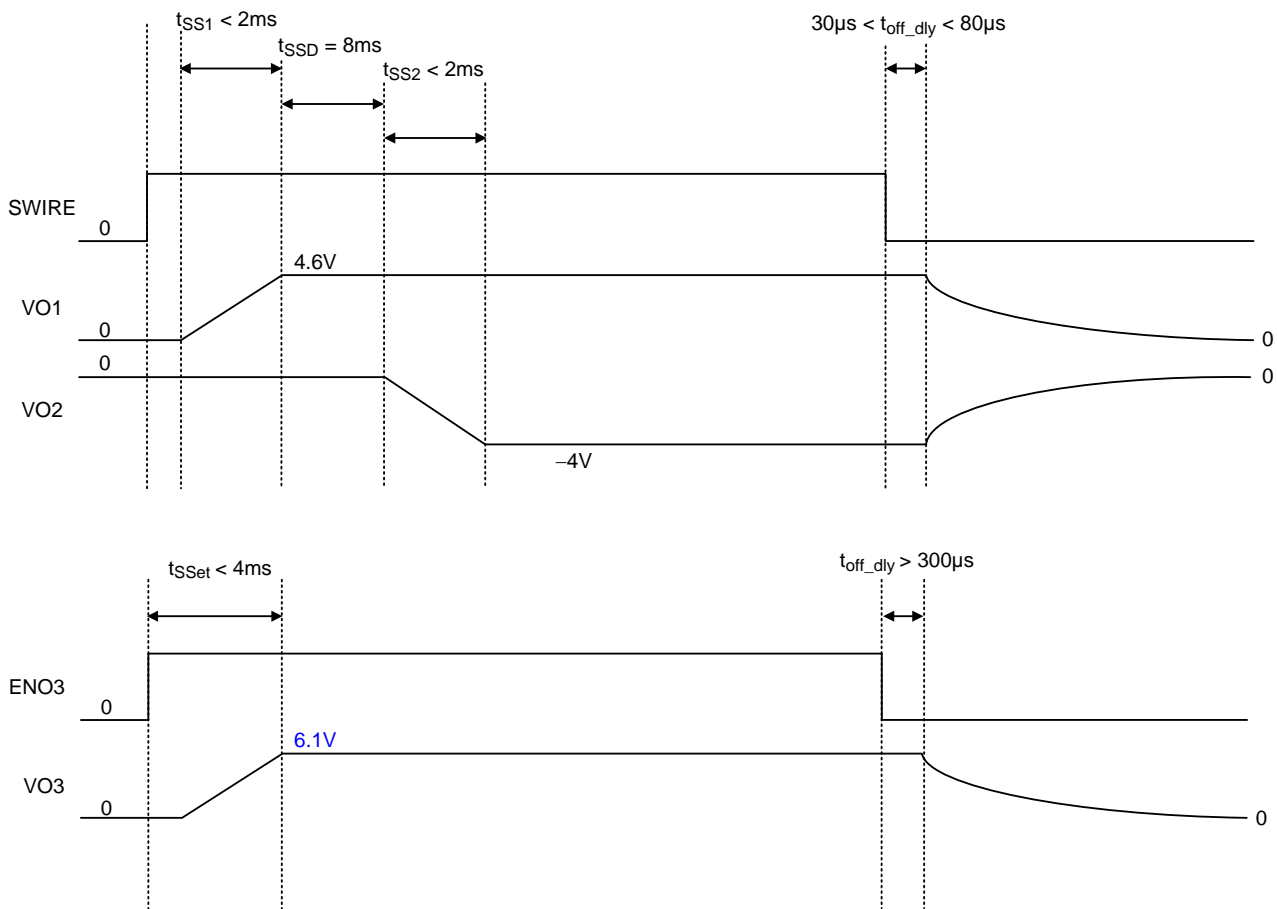
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Timing Diagram

SWIRE Command Timing Diagram



Power Sequence



Absolute Maximum Ratings (Note 1)

- PVIN, AVIN, VO1, LX1, FBS, FD, ENO3, SWIRE----- -0.3V to 6V
- VO3, LX3----- -0.3V to 12V
- VO2----- -6V to 0.3V
- LX2----- -6V to 6V
- Power Dissipation, P_D @ T_A = 25°C
 - WQFN-16L 3x3 ----- 3.33W
- Package Thermal Resistance (Note 2)
 - WQFN-16L 3x3, θ_{JA} ----- 30°C/W
 - WQFN-16L 3x3, θ_{JC} ----- 7.5°C/W
- Lead Temperature (Soldering, 10sec.)----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 - HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ----- 2.9V to 4.5V
- Ambient Temperature Range ----- -40°C to 85°C
- Junction Temperature Range ----- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 3.7V, V_{O1} = 4.6V, V_{O2} = -4V, V_{O3} = 6.1V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply						
Input Voltage Range	V _{IN}		2.9	3.7	4.5	V
Under Voltage Lockout High	UVLO_H	V _{IN} rising	2.3	2.4	2.5	V
Under Voltage Lockout Hys	UVLO_Hys	V _{IN} hysteresis	--	0.2	--	V
V _{IN} Shutdown Current	I _{SHDN}	ENO3 = GND, SWIRE = GND	--	--	1	μA
ENO3, SWIRE, FD Input High Threshold	V _{IH}	V _{IN} = 2.9V to 4.5V	1.2	--	--	V
ENO3, SWIRE, FD Input Low Threshold	V _{IL}	V _{IN} = 2.9V to 4.5V	--	--	0.4	V
ENO3 Pull Down Current	I _{ENO3}		--	--	10	μA
SWIRE Pull-down Resistor	R _{SWIRE}		--	150	--	kΩ
Operation Section						
Switching Frequency	f _{SW}	PWM mode	1.35	1.5	1.65	MHz
VO1 Maximum Duty	D _{MAX_N1}	No load	--	87	--	%
VO2 Maximum Duty	D _{MAX_NN1}	No load	--	87	--	%
VO3 Maximum Duty	D _{MAX_N3}	No load	--	87	--	%

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Over-Temperature Protection	OTP		--	140	--	°C
Over-Temperature Protection Hysteresis	OTPHYST		--	15	--	°C
VO3 AVDD Output						
AVDD Output Voltage Range	VO3	42 to 49 pulses by SWIRE pin	5.8	6.1	7.9	V
AVDD Output Voltage Total Variation	VO3_ACY	No load	-2	--	2	%
Maximum Output Current	IO3MAX	V _{IN} = 2.9V to 4.5V	--	--	55	mA
N3 N-MOSFET On-Resistance	RDSON3	V _{IN} = 3.7V, I _{LX-N3} = 20mA	--	0.4	--	Ω
P3 P-MOSFET On-Resistance		V _{IN} = 3.7V, I _{LX-P3} = 20mA	--	1	--	Ω
Current Limit	IOCP3		0.28	0.35	0.42	A
Line Regulation	VO3Line_R	IO3 = 15mA	--	0.01	--	%/V
Load Regulation	VO3Load_R		--	0.4	--	%/A
VO1 Positive Output						
Positive Output Range	VO1		--	4.6	--	V
Positive Output Voltage Variation			-0.5	--	0.5	%
Maximum Output Current	IO1MAX	V _{IN} = 2.9V to 4.5V	--	--	300	mA
N1 N-MOSFET On-Resistance	RDS(ON)1	V _{IN} = 3.7V, I _{LX-N1} = 100mA	--	0.2	--	Ω
P1 P-MOSFET On-Resistance		V _{IN} = 3.7V, I _{LX-P1} = 100mA	--	0.2	--	Ω
Current Limit	IOCP1		0.8	1	1.2	A
Line Regulation	VO1Line_R	IO1 = 100mA	--	0.02	--	%/V
Load Regulation	VO1Load_R	IO1 = 5mA to 300mA	--	0.4	--	%/A
VO2 Negative Output						
Adjustable Negative Output Voltage Range	VO2	41 different values set by SWIRE pin	-5.4	-4	-1.4	V
Negative Output Voltage Variation	VO2_ACY	VO2 = -2.4V, No Load	-50	--	50	mV
Maximum Output Current	IO2MAX	V _{IN} = 2.9V to 4.5V	--	--	300	mA
NN1 N-MOSFET On-Resistance	RDS(ON)2	V _{IN} = 3.7V, I _{LX-NN1} = 100mA	--	0.2	--	Ω
NN2 N-MOSFET On-Resistance		V _{IN} = 3.7V, I _{LX-NN2} = 100mA	--	0.2	--	Ω
Current Limit	IOCP2		1.6	1.9	2.2	A
Line Regulation	VO2Line_R	IO2 = 100mA	--	0.02	--	%/V
Load Regulation	VO2Load_R		--	0.4	--	%/A
VO1 Discharge Resistor Value	RDIS1		--	40	--	Ω
VO2 Discharge Resistor Value	RDIS2		--	40	--	Ω
VO3 Discharge Resistor Value	RDIS3		--	30	--	Ω

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at $T_A = 25^\circ\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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Typical Application Circuit

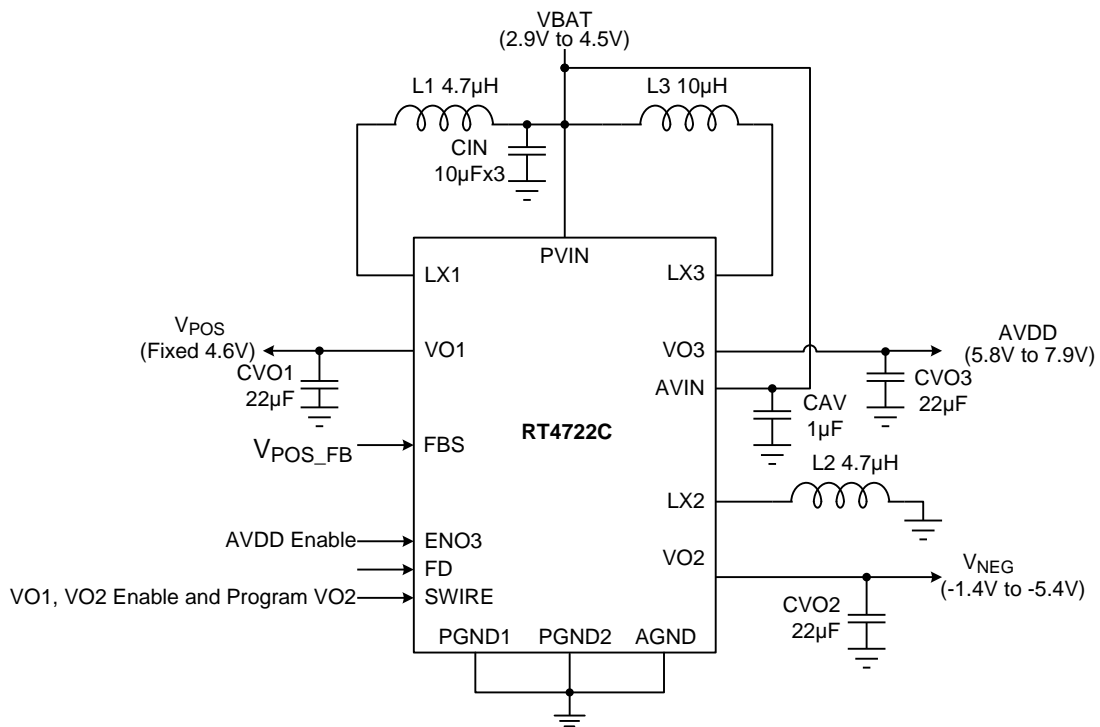
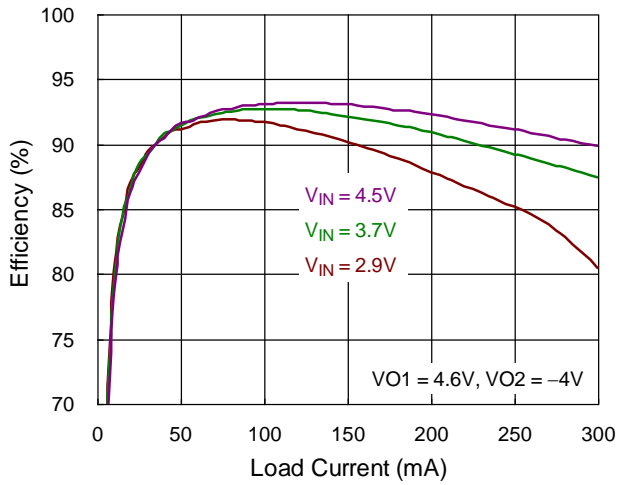


Table 5. Typical BOM List

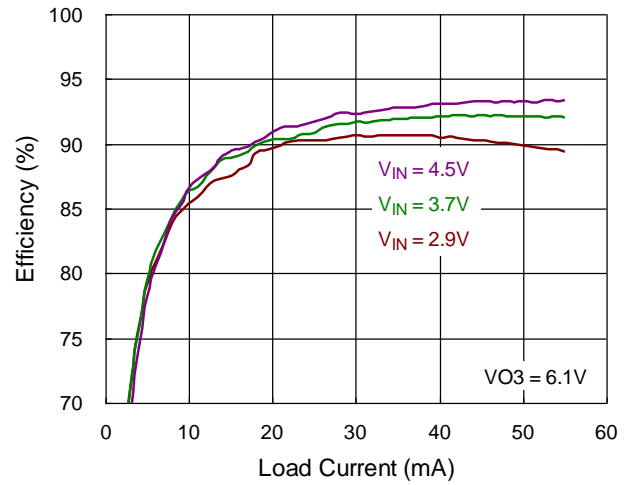
Reference	Qty	Part Number	Description	Package	Supplier
CIN	3	GRM188R61C106KAAL	10µF/16V/X5R	0603	Murata
CVO1, CVO2, CVO3	1	GRM219R61C226ME15	22µF/16V/X5R	0805	Murata
CAV	1	GRM185R61C105KE44	1µF/16V/X5R	0603	Murata
L1, L2	1	1239AS-H-4R7M = P2	4.7µH	2.5 x 2.0 x 1.2mm	Toko
L3	1	1239AS-H-100M = P2	10µH	2.5 x 2.0 x 1.2mm	Toko

Typical Operating Characteristics

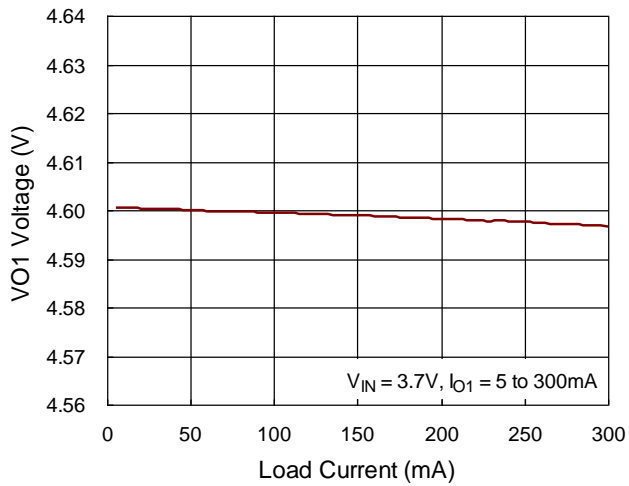
VO1 & VO2 Efficiency vs. Load Current



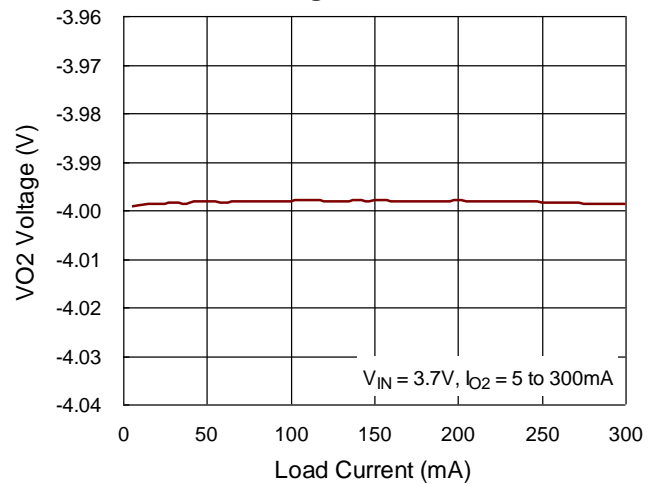
VO3 Efficiency vs. Load Current



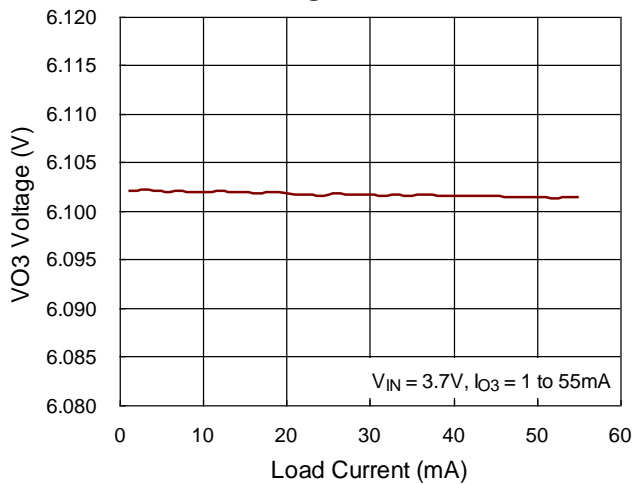
VO1 Voltage vs. Load Current



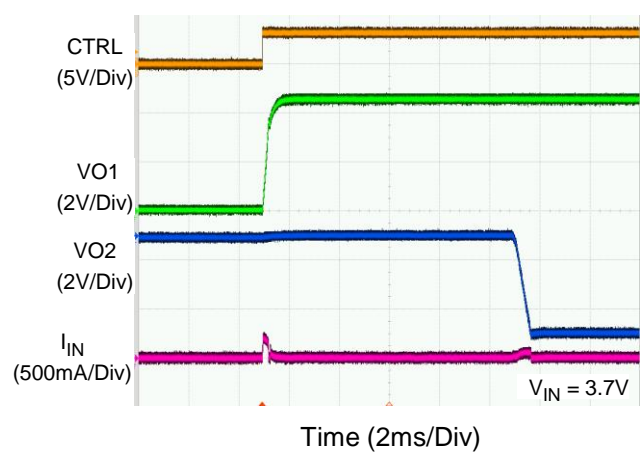
VO2 Voltage vs. Load Current



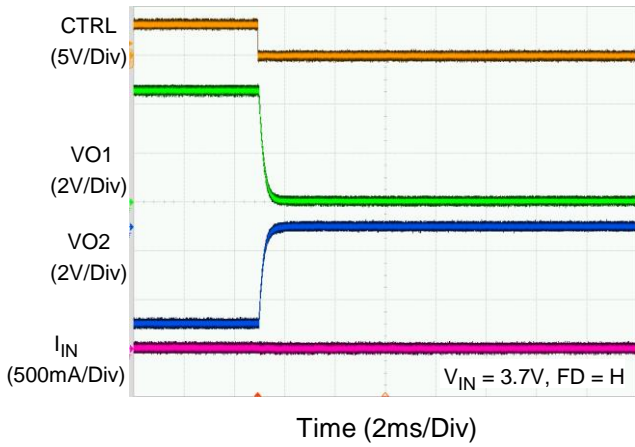
VO3 Voltage vs. Load Current



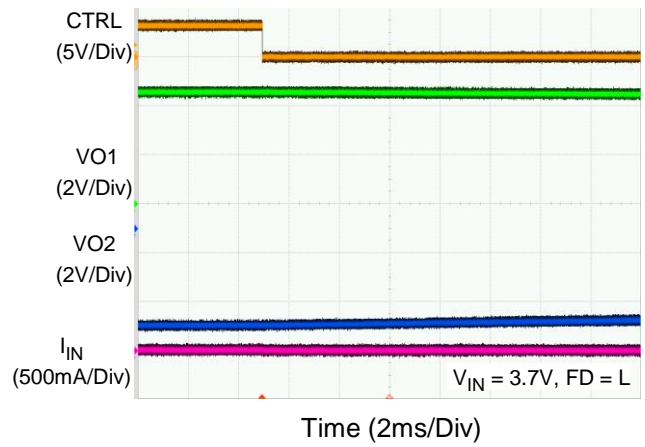
VO1 & VO2 Power On



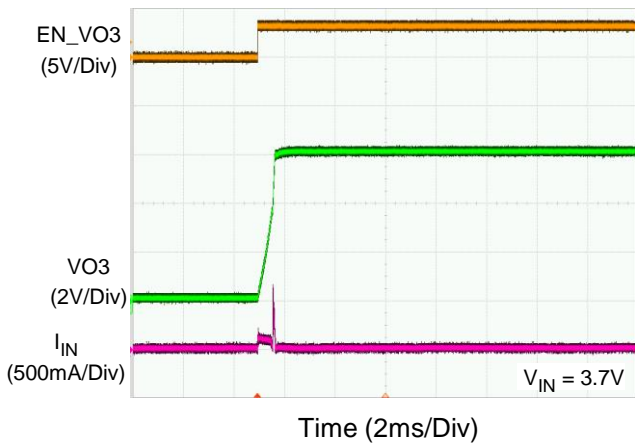
VO1 & VO2 Power Off



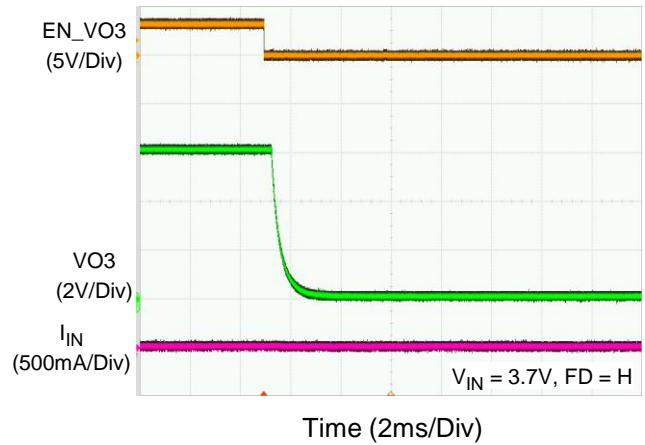
VO1 & VO2 Power Off



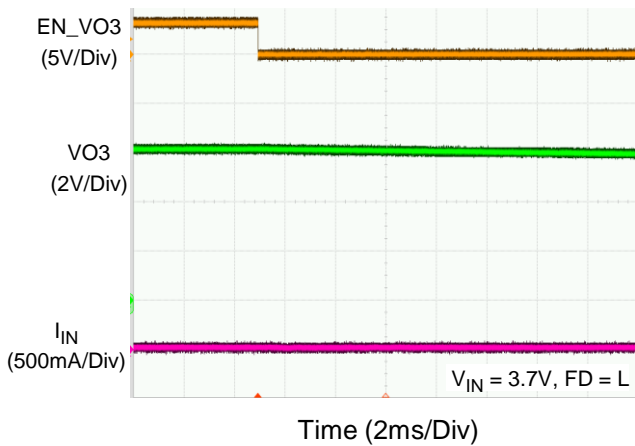
VO3 Power On



VO3 Power Off



VO3 Power Off



Application Information

The RT4722C is a triple channels DC-DC converter, which integrates dual step up converter and an inverting converter to provide the positive and negative output voltage required by AMOLED. Both positive (VO1) and negative (VO2) voltage can be programmed by external MCU through single wire (SWIRE pin) and another step up converter is from 5.8V to 7.9V output voltage by SWIRE pin. The RT4722C protection function includes Over-Temperature Protection (OTP), Over-Current Protection (OCP) and Short Circuit Protection (SCP), VO2 and VO3 have Pulse Skipping Mode (PSM) to provide high efficiency during light load.

Soft-Start

The RT4722C use an internal soft-start feature to avoid high inrush currents during step-up.

It is suggested that system need start loading after soft start finished and output voltage was ready.

Fast Discharge Function

All outputs voltage use an embedded discharge function to discharge the remaining output to 0V rapidly, preventing phenomena such as residual image on the display during shutdown.

Over-Temperature Protection (OTP)

The RT4722C includes an Over-Temperature Protection (OTP) feature to prevent excessive power dissipation from overheating the device. The OTP will shut down switching operation when junction temperature exceeds 140°C. Once the junction temperature cools down by approximately 15°C, the converter resumes operation.

To maintain continuous operation, prevent the maximum junction temperature from rising above 125°C.

Over-Current Protection (OCP)

The RT4722C includes a current sensing circuitry which monitors the inductor current during each ON period after soft start finished. If the current value becomes greater than the current limit, the switch that pertains to inductor charging will turn off, forcing the inductor to leave charging stage and enter discharge stage.

If OCP occurs keep more than 1ms IC will shut down and need reset enable signal to recovery.

Short Circuit Protection (SCP)

The RT4722C has an advanced short circuit protection mechanism which prevents damage to the device from unexpected applications. When the output becomes lower than about 90% shorted to ground, over 1ms the device enters shutdown mode.

Under-Voltage Lockout (UVLO)

To prevent abnormal operation of the IC in low voltage condition, an under voltage lockout is included, which shuts down the device at voltages lower than 2.2V. All functions will be turned off in this state.

Input Capacitor Selection

Each channel input ceramic capacitors with 10μF capacitance are suggested for the RT4722C applications. However, to achieve best performance with the RT4722C, larger capacitance can be used. For better voltage filtering, select ceramic capacitors with low ESR, X5R and X7R types which are suitable because of their wider voltage and temperature ranges.

Boost Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\eta \times V_{IN}}$$

$$\Delta I_L = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the converter, $I_{IN(MAX)}$ is the maximum input current, and ΔI_L is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of the inductor must be greater than I_{PEAK} .

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The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

where f_{OSC} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Output Capacitor Selection

The output ripple voltage is an important index for estimating chip performance. This portion consists of two parts. One is the product of the inductor peak current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in Figure 1, ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2} \Delta I_L - I_{OUT} \right) + \left(I_{IN} - \frac{1}{2} \Delta I_L - I_{OUT} \right) \right] \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f_{OSC}} = C_{OUT} \times V_{OUT1}$$

where f_{OSC} is the switching frequency and ΔI_L is the inductor ripple current. Bring C_{OUT} to the left side to estimate the value of ΔV_{OUT1} according to the following equation :

$$\Delta V_{OUT1} = \Delta V_{ESR} + \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

where $\Delta V_{ESR} = \Delta I_C \times R_{C_ESR} = I_{PEAK} \times R_{C_ESR}$

The output capacitor, C_{OUT} , should be selected accordingly. It is suggested that use better DC bias performance capacitor for stability and output ripple. Two ceramic 10 μ F capacitor is enough generally.

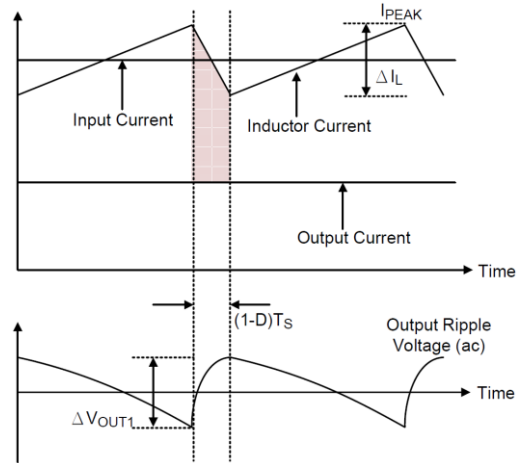


Figure 1. The Output Ripple Voltage without the Contribution of ESR

Buck-boost Converter Inductor Selection

The first step in the design procedure is to verify whether the maximum possible output current of the buck-boost converter supports the specific application requirements. To simplify the calculation, the fastest approach is to estimate converter efficiency by taking the efficiency numbers from provided efficiency curves or to use a worst case assumption for the expected efficiency, e.g., 80%. The calculation must be performed for the minimum assumed input voltage where the peak switch current is the highest. The inductor has an internal switch to be able to handle this current.

► Converter Duty Cycle :

$$D = \frac{-V_{OUT}}{V_{IN} \times \eta - V_{OUT}}$$

► Maximum output current :

$$I_{OUT} = \left(I_{PEAK} - \frac{V_{IN} \times D}{2 \times f_{OSC} \times L} \right) \times (1-D)$$

► Inductor peak current :

$$I_{PEAK} = \frac{I_{OUT}}{1-D} + \frac{V_{IN} \times D}{2 \times f_{OSC} \times L}$$

As for inductance, we are going to derive the transition point, where the converter toggles from CCM to DCM. We need to define the point at which the inductor current ripple touches zero, and as the power switch SW is immediately reactivated, the current ramps up again. Figure 2 portrays the input current activity of the buck-boost converter.

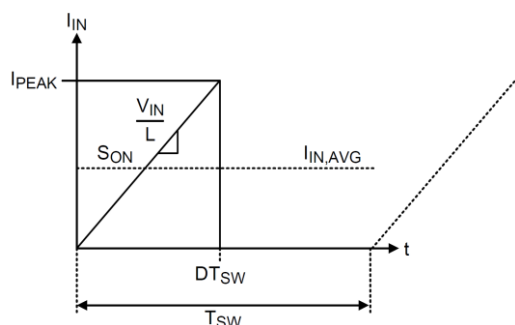


Figure 2. The Buck-Boost Input Signature in BCM
The inductance can eventually be determined according to the following equation :

$$L_{\text{critical}} = \frac{|V_{\text{OUT}}| \times \eta}{2 \times f_{\text{OSC}} \times I_{\text{OUT}}} \times \left(\frac{V_{\text{IN}}}{V_{\text{IN}} + |V_{\text{OUT}}|} \right)^2$$

Buck-Boost Converter Output Capacitor Selection

For the best output voltage filtering, low ESR ceramic capacitors are recommended. One 22 μ F output capacitors with sufficient voltage ratings in parallel are adequate for most applications. Additional capacitors can be added to improve load transient response.

To calculate the output voltage ripple, the following equations can be used :

$$\Delta V = \frac{D \times |V_{\text{OUT}}|}{f_{\text{OSC}} \times R_{\text{LOAD}} \times C_{\text{OUT}}} + \Delta V_{\text{ESR}}$$

where $\Delta V_{\text{ESR}} = \Delta I_C \times R_{C_ESR} = I_{\text{PEAK}} \times R_{C_ESR}$

ΔV_{ESR} can be neglected in many cases since ceramic capacitors provides very low ESR.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{\text{J(MAX)}}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{\text{D(MAX)}} = (T_{\text{J(MAX)}} - T_{\text{A}}) / \theta_{\text{JA}}$$

where $T_{\text{J(MAX)}}$ is the maximum junction temperature, T_{A} is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-16L 3x3 package, the thermal resistance, θ_{JA} , is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_{\text{A}} = 25^\circ\text{C}$ can be calculated as below :

$$P_{\text{D(MAX)}} = (125^\circ\text{C} - 25^\circ\text{C}) / (30^\circ\text{C/W}) = 3.33\text{W}$$

for a WQFN-16L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{\text{J(MAX)}}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

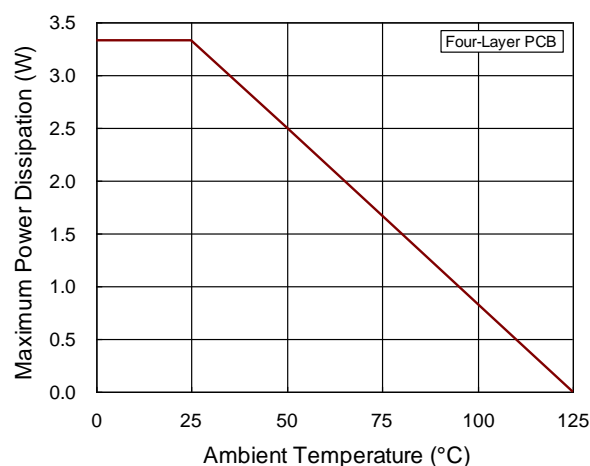


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

For the best performance of the RT4722C, the following PCB layout guidelines should be strictly followed.

- ▶ For good regulation, place the power components as close to the IC as possible. The traces should be wide and short, especially for the high current output loop.
- ▶ The input and output bypass capacitor should be placed as close to the IC as possible and connected to the ground plane of the PCB.

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- ▶ Minimize the size of the LX1, LX2, LX3 nodes and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near LX or high-current traces.
- ▶ Separate power ground (PGND) and analog ground (AGND). Connect the AGND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes.
- ▶ Connect the exposed pad to a strong ground plane for maximum thermal dissipation.

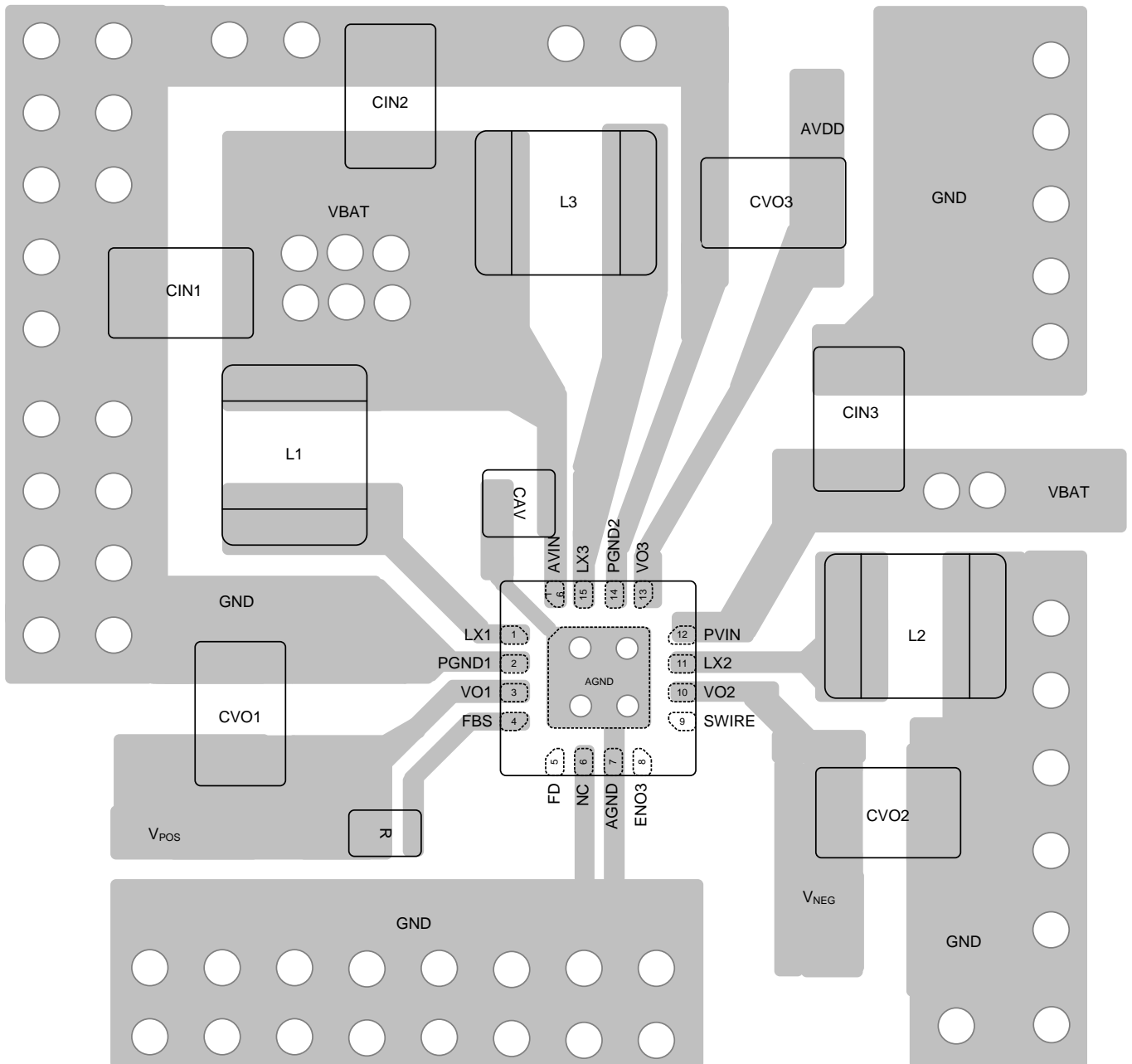
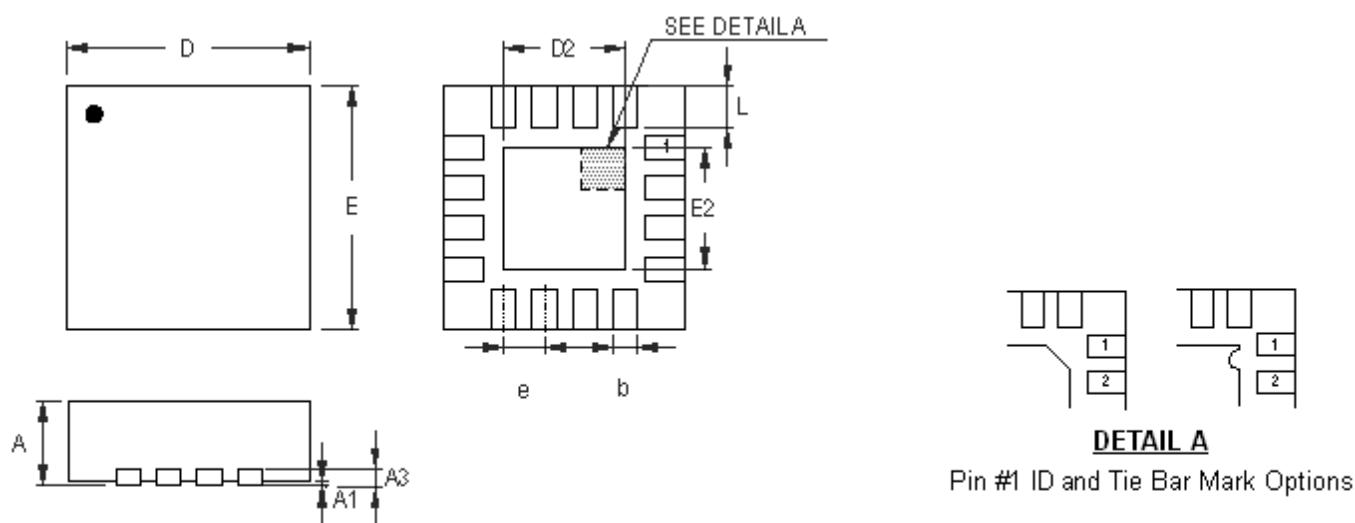


Figure 4. PCB Layout Guide

Outline Dimension



DETAIL A
Pin #1 ID and Tie Bar Mark Options

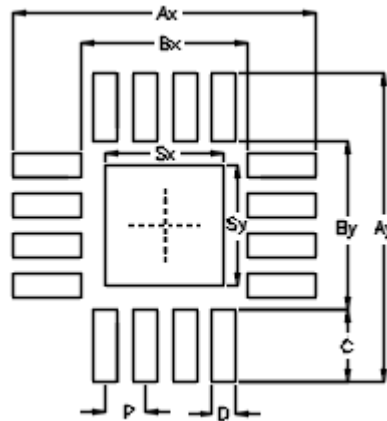
Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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Footprint Information



Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN3*3-16	16	0.50	3.80	3.80	2.10	2.10	0.85	0.30	1.50	1.50	±0.05