

## TPS7A8001 Low-Noise, Wide-Bandwidth, High PSRR, Low-Dropout 1A Linear Regulator

### 1 Features

- Low-Dropout 1-A Regulator With Enable
- Adjustable Output Voltages: 0.8 V to 6 V
- Wide-Bandwidth High PSRR:
  - 63 dB at 1 kHz
  - 57 dB at 100 kHz
  - 38 dB at 1 MHz
- Low Noise:  $(14 \times V_{OUT}) \mu\text{V}_{\text{RMS}}$  Typical (100 Hz to 100 kHz)
- Stable with a 4.7- $\mu\text{F}$  Ceramic Capacitor
- Excellent Load/Line Transient Response
- 3% Overall Accuracy (Over Load/Line/Temp)
- Overcurrent and Overtemperature Protection
- Very Low Dropout: 170 mV Typical at 1 A
- 3-mm  $\times$  3-mm VSON-8 DRB Package

### 2 Applications

- Telecom Infrastructure
- Audio
- High-Speed I/F (PLL/VCO)

### 3 Description

The TPS7A8001 is a low-dropout linear regulator (LDO) offering very high power-supply ripple rejection (PSRR) at the output. This LDO uses an advanced BiCMOS process and a PMOSFET pass device to achieve very low noise, excellent transient response, and excellent PSRR performance.

The TPS7A8001 is stable with a 4.7- $\mu\text{F}$  ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations.

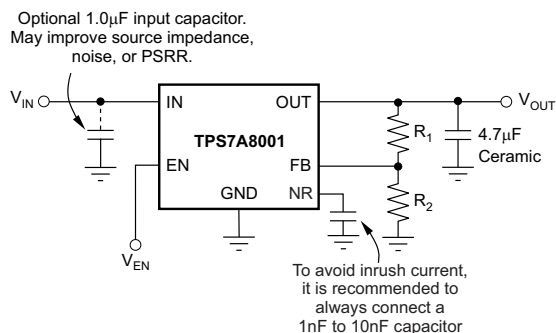
This device is fully specified over the temperature range of  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  and is offered in a 3mm  $\times$  3mm, VSON-8 package with a thermal pad.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A80	VSON (8)	3.00 mm $\times$ 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Diagram



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (January 2013) to Revision I	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted "Fixed Output Voltages: 0.8 V to 5 V Using Innovating Facatory EEPROM Programming" bullet from <i>Features</i> ...	1
• Changed "12.6" to "14" in Low Noise bullet	1
• Deleted SNS row from <i>Pin Functions</i>	4
• Deleted Fixed Version from V <sub>OUT</sub> row in <i>Electrical Characteristics</i>	6
• Deleted ISNS row from <i>Electrical Characteristics</i>	6

Changes from Revision G (April 2012) to Revision H	Page
• Updated <a href="#">Figure 8</a>	7

Changes from Revision F (March 2012) to Revision G	Page
• Changed Thermal Information table values, added new footnote 2, changed footnote 3	5

Changes from Revision E (February 2012) to Revision F	Page
• Changed <i>Low Noise</i> Features bullet	1
• Updated <a href="#">Equation 3</a>	15

Changes from Revision D (December 2010) to Revision E	Page
• Changed <i>Low Noise</i> Features bullet	1
• Changed caption of front-page application circuit	1
• Updated <a href="#">Figure 12</a>	7

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• Updated <a href="#">Figure 26</a> .....	10
• Added <a href="#">Equation 1</a> note in <i>Start-up</i> section.....	13
• Updated <a href="#">Equation 3</a> .....	15

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<b>Changes from Revision C (September, 2010) to Revision D</b>	<b>Page</b>
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• Updated front-page figure with new characteristic graph.....	1
• Revised <a href="#">Figure 17</a> .....	8
• Changed <a href="#">Figure 18</a> .....	8

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<b>Changes from Revision B (August, 2010) to Revision C</b>	<b>Page</b>
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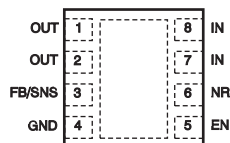
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• Changed data sheet title.....	1
• Changed <i>ultra-high PSRR</i> to <i>wide-bandwidth lgh PSRR</i> in <i>Features</i> list.....	1
• Corrected typos in <a href="#">Figure 21</a> through <a href="#">Figure 23</a> .....	9
• Revised first paragraph of <i>Application Information</i> to remove phrase <i>ultra-wide bandwidth</i> .....	14

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## 5 Pin Configuration and Functions

DRB Package  
8-Pin VSON  
Top View



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to <i>Shutdown</i> in the <i>Application and Implementation</i> section for more details. EN must not be left floating and can be connected to IN if not used.
FB	3	I	This pin is the input to the control loop error amplifier and is used to set the output voltage of the device.
GND	4, pad	—	Ground.
IN	7, 8	I	Unregulated input supply.
OUT	1, 2	O	Regulator output. A 4.7µF or larger capacitor of any type is required for stability.
NR	6	—	Connect an external capacitor between this pin and ground to reduce output noise to very low levels. Also, the capacitor slows down the $V_{OUT}$ ramp (RC softstart).

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	IN	-0.3	7	V
	FB, NR	-0.3	3.6	V
	EN	-0.3	$V_{IN} + 0.3^{(2)}$	V
	OUT	-0.3	7	V
Current	OUT	Internally Limited		A
Temperature	Operating virtual junction, $T_J$	-55	150	°C
	Storage, $T_{stg}$	-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2)  $V_{EN}$  absolute maximum rating is  $V_{IN} + 0.3$  V or 7 V, whichever is smaller.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_I$	Input voltage	2.2	6.5	V
$I_O$	Output current	0	1	A
$T_A$	Operating free air temperature	-40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)(2)</sup>		TPS7A80xx	UNIT
		DRB (VSON) <sup>(3)</sup>	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).
- (3) Thermal data for the DRB package are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
- The exposed pad is connected to the PCB ground layer through a 2 × 2 thermal via array.
  - The top and bottom copper layers are assumed to have a 5% thermal conductivity of copper representing a 20% copper coverage.
  - This data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3 inches × 3 inches copper area. To understand the effects of the copper area on thermal performance, refer to the [Power Dissipation](#) and [Estimating Junction Temperature](#) sections.

# TPS7A8001

SBVS135I–JUNE 2010–REVISED AUGUST 2015

## 6.5 Electrical Characteristics

Over the operating temperature range of  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.2\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 2.2\text{ V}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ , and  $C_{NR} = 0.01\text{ }\mu\text{F}$ , unless otherwise noted. TPS7A8001 is tested at  $V_{OUT} = 0.8\text{ V}$  and  $V_{OUT} = 6\text{ V}$ . Typical values are at  $T_J = 25^\circ\text{C}$ .

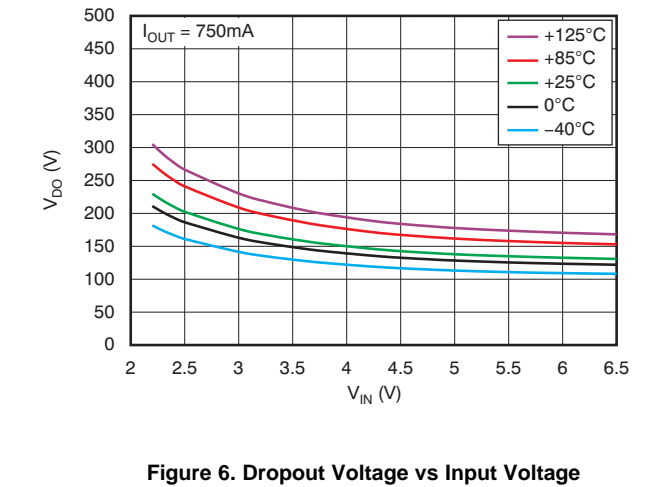
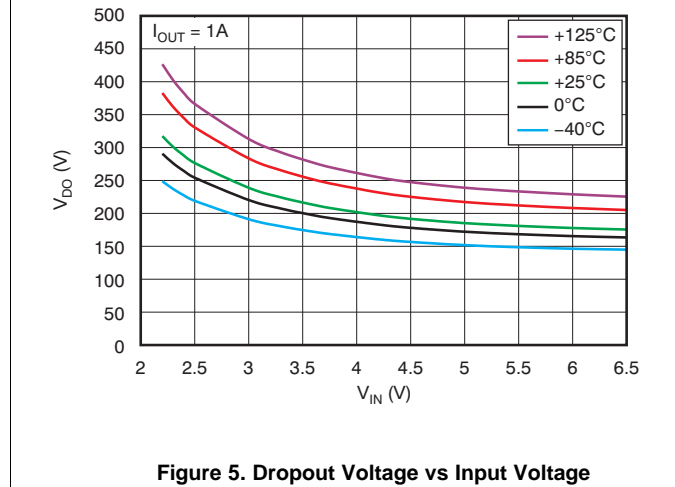
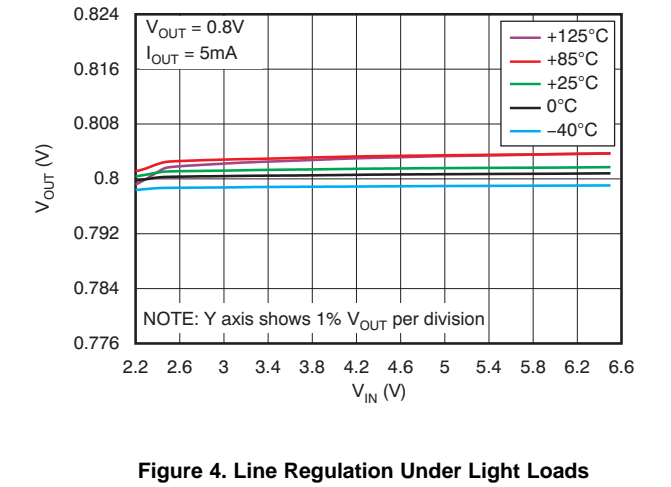
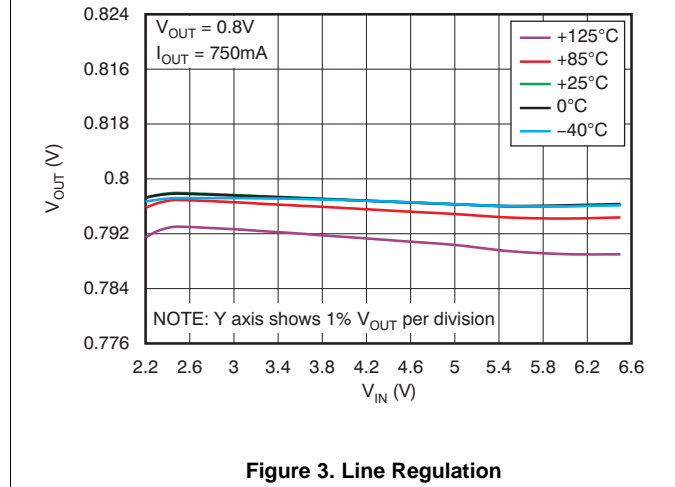
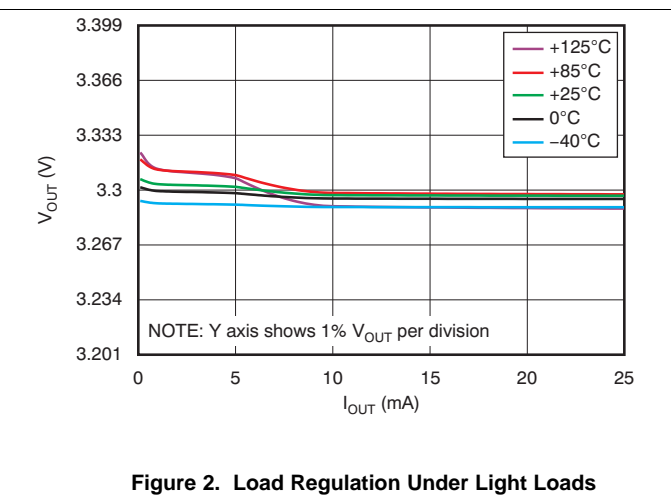
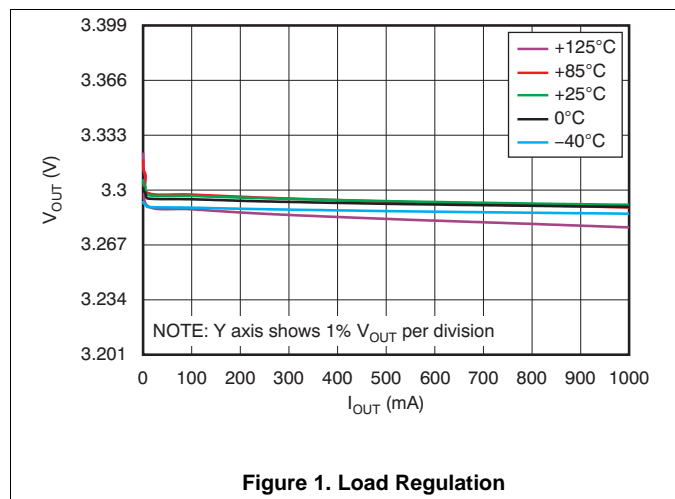
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range <sup>(1)</sup>		2.2		6.5	V
$V_{NR}$	Internal reference		0.79	0.8	0.81	V
$V_{OUT}$	Output voltage range		0.8		6	V
	Output accuracy <sup>(2)</sup>	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 6\text{ V}$ , $V_{IN} \geq 2.5\text{ V}$ , $100\text{ mA} \leq I_{OUT} \leq 500\text{ mA}$ , $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$	-2%		2%	
		$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , $V_{IN} \geq 2.2\text{ V}$ , $100\text{ mA} \leq I_{OUT} \leq 1\text{ A}$	-3%	$\pm 0.3\%$	3%	
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)} + 0.5\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , $V_{IN} \geq 2.2\text{ V}$ , $I_{OUT} = 100\text{ mA}$		150		$\mu\text{V/V}$
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	$100\text{ mA} \leq I_{OUT} \leq 1\text{ A}$		2		$\mu\text{V/mA}$
$V_{DO}$	Dropout voltage	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , $V_{IN} \geq 2.2\text{ V}$ , $I_{OUT} = 500\text{ mA}$ , $V_{FB} = \text{GND}$ or $V_{SNS} = \text{GND}$			250	mV
		$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , $V_{IN} \geq 2.5\text{ V}$ , $I_{OUT} = 750\text{ mA}$ , $V_{FB} = \text{GND}$ or $V_{SNS} = \text{GND}$			350	mV
		$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , $V_{IN} \geq 2.5\text{ V}$ , $I_{OUT} = 1\text{ A}$ , $V_{FB} = \text{GND}$ or $V_{SNS} = \text{GND}$			500	mV
$I_{CL}$	Output current limit	$V_{OUT} = 0.85 \times V_{OUT(NOM)}$ , $V_{IN} \geq 3.3\text{ V}$	1100	1400	2000	mA
$I_{GND}$	Ground pin current	$I_{OUT} = 1\text{ mA}$		60	100	$\mu\text{A}$
		$I_{OUT} = 1\text{ A}$			350	$\mu\text{A}$
$I_{SHDN}$	Shutdown current ( $I_{GND}$ )	$V_{EN} \leq 0.4\text{ V}$ , $V_{IN} \geq 2.2\text{ V}$ , $R_L = 1\text{ k}\Omega$ , $0^\circ\text{C} \leq T_J \leq 85^\circ\text{C}$		0.20	2	$\mu\text{A}$
$I_{FB}$	Feedback pin current	$V_{IN} = 6.5\text{ V}$ , $V_{FB} = 0.8\text{ V}$		0.02	1	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$V_{IN} = 4.3\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 750\text{ mA}$	$f = 100\text{ Hz}$	48		dB
			$f = 1\text{ kHz}$	63		dB
			$f = 10\text{ kHz}$	63		dB
			$f = 100\text{ kHz}$	57		dB
			$f = 1\text{ MHz}$	38		dB
$V_N$	Output noise voltage	BW = 100 Hz to 100 kHz, $V_{IN} = 4.3\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 100\text{ mA}$	$C_{NR} = 0.001\text{ }\mu\text{F}$	$14.6 \times V_{OUT}$		$\mu\text{V}_{RMS}$
			$C_{NR} = 0.01\text{ }\mu\text{F}$	$14.3 \times V_{OUT}$		$\mu\text{V}_{RMS}$
			$C_{NR} = 0.1\text{ }\mu\text{F}$	$13.9 \times V_{OUT}$		$\mu\text{V}_{RMS}$
$V_{EN(HI)}$	Enable high (enabled)	$2.2\text{ V} \leq V_{IN} \leq 3.6\text{ V}$ , $R_L = 1\text{ k}\Omega$	1.2			V
		$3.6\text{ V} < V_{IN} \leq 6.5\text{ V}$ , $R_L = 1\text{ k}\Omega$	1.35			V
$V_{EN(LO)}$	Enable low (shutdown)	$R_L = 1\text{ k}\Omega$	0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	$V_{IN} = V_{EN} = 6.5\text{ V}$		0.02	1	$\mu\text{A}$
$t_{STR}$	Start-up time	$V_{OUT(NOM)} = 3.3\text{ V}$ , $V_{OUT} = 0\%$ to $90\%$ $V_{OUT(NOM)}$ , $R_L = 3.3\text{ k}\Omega$ , $C_{OUT} = 4.7\text{ }\mu\text{F}$	$C_{NR} = 1\text{ nF}$	0.1		ms
			$C_{NR} = 10\text{ nF}$	1.6		ms
UVLO	Undervoltage lockout	$V_{IN}$ rising, $R_L = 1\text{ k}\Omega$	1.86	2	2.10	V
	Hysteresis	$V_{IN}$ falling, $R_L = 1\text{ k}\Omega$		75		mV
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing		160		$^\circ\text{C}$
		Reset, temperature decreasing		140		$^\circ\text{C}$
$T_J$	Operating junction temperature		-40		125	$^\circ\text{C}$

(1) Minimum  $V_{IN} = V_{OUT} + V_{DO}$  or  $2.2\text{ V}$ , whichever is greater.

(2) As for TPS7A8001 (adjustable); it does not include external resistor tolerances and it is not tested at this condition:  $V_{OUT} = 0.8\text{ V}$ ,  $4.5\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ , and  $750\text{ mA} \leq I_{OUT} \leq 1\text{ A}$  because of power dissipation higher than maximum rating of the package.

### 6.6 Typical Characteristics

At  $V_{OUT(TYP)} = 3.3\text{ V}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.2\text{ V}$  (whichever is greater),  $I_{OUT} = 100\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ , and  $C_{NR} = 0.01\text{ }\mu\text{F}$ , all temperature values refer to  $T_J$ , unless otherwise noted.



Typical Characteristics (continued)

At  $V_{OUT(TYP)} = 3.3\text{ V}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.2\text{ V}$  (whichever is greater),  $I_{OUT} = 100\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ , and  $C_{NR} = 0.01\text{ }\mu\text{F}$ , all temperature values refer to  $T_J$ , unless otherwise noted.

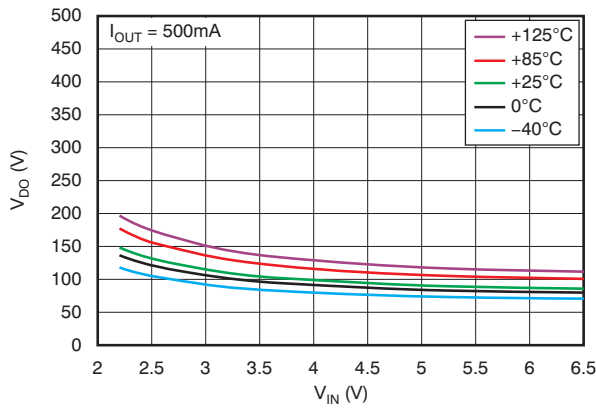


Figure 7. Dropout Voltage vs Input Voltage

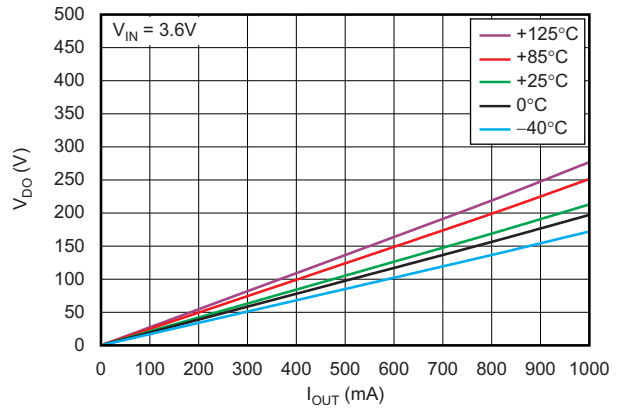


Figure 8. Dropout Voltage vs Load Current

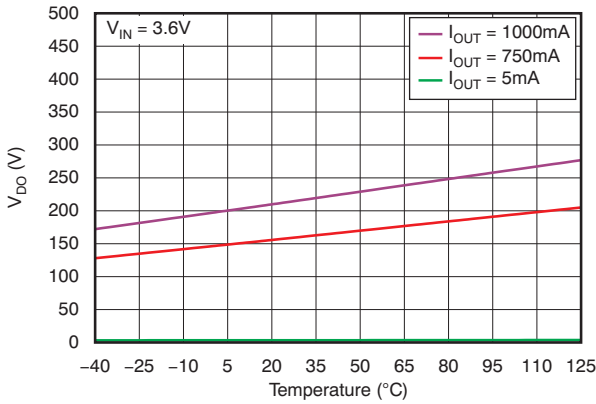


Figure 9. Dropout Voltage vs Temperature

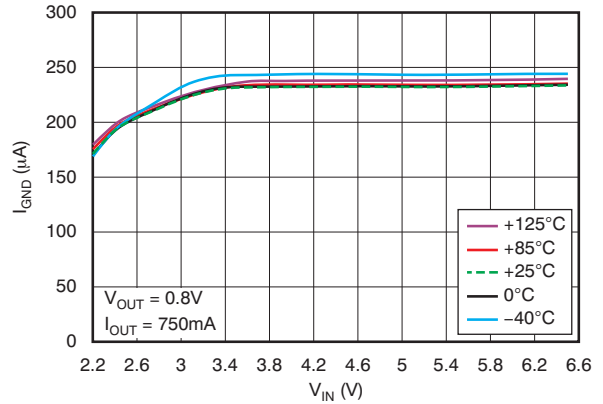


Figure 10. Ground Pin Current vs Input Voltage

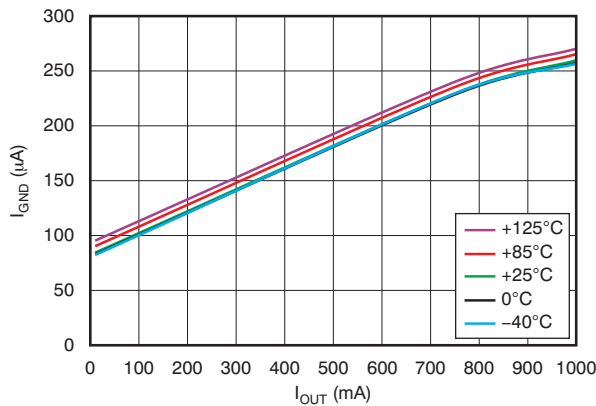


Figure 11. Ground Pin Current vs Load Current

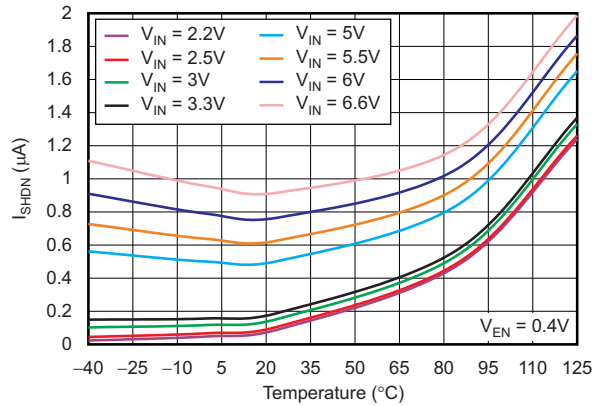


Figure 12. Shutdown Current vs Temperature



### Typical Characteristics (continued)

At  $V_{OUT(TYP)} = 3.3\text{ V}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.2\text{ V}$  (whichever is greater),  $I_{OUT} = 100\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ , and  $C_{NR} = 0.01\text{ }\mu\text{F}$ , all temperature values refer to  $T_J$ , unless otherwise noted.

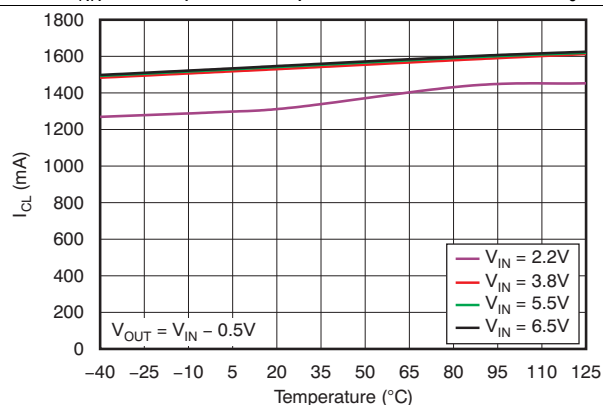


Figure 13. Current Limit vs Temperature

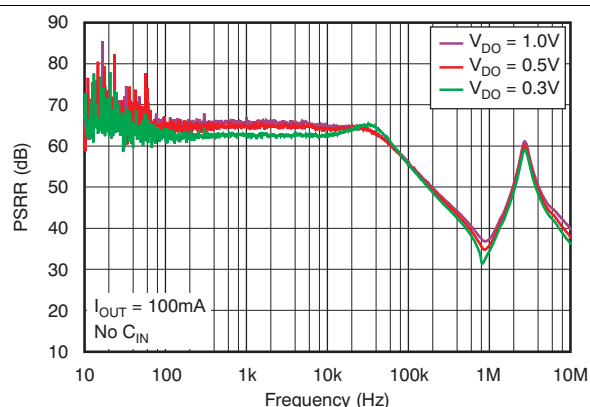


Figure 14. Power-Supply Ripple Rejection vs Frequency

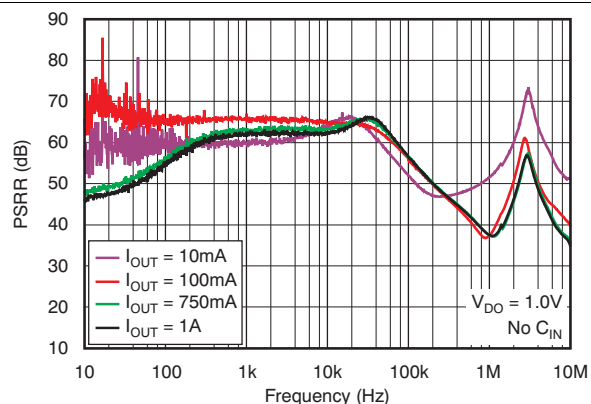


Figure 15. Power-Supply Ripple Rejection vs Frequency

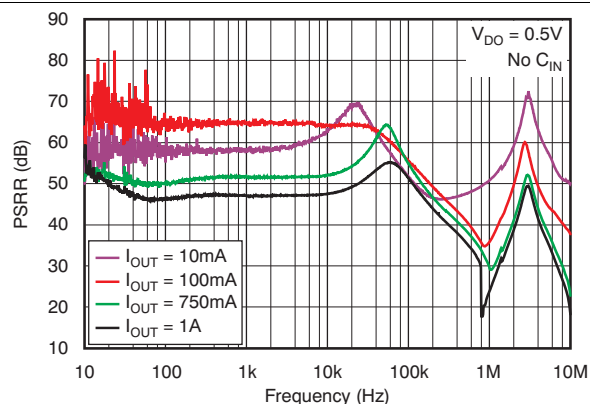


Figure 16. Power-Supply Ripple Rejection vs Frequency

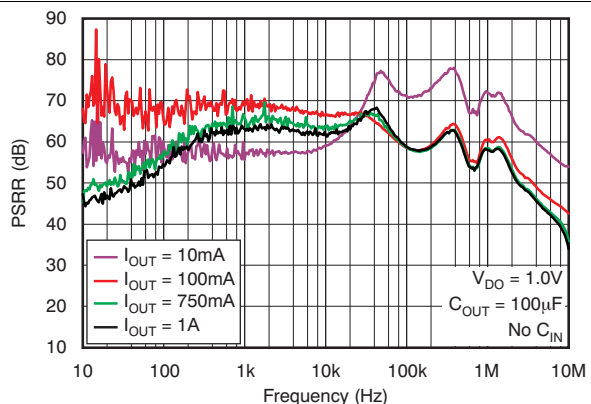


Figure 17. Power-Supply Ripple Rejection vs Frequency

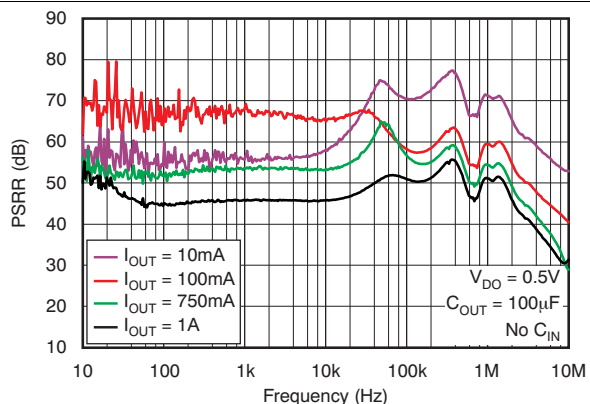
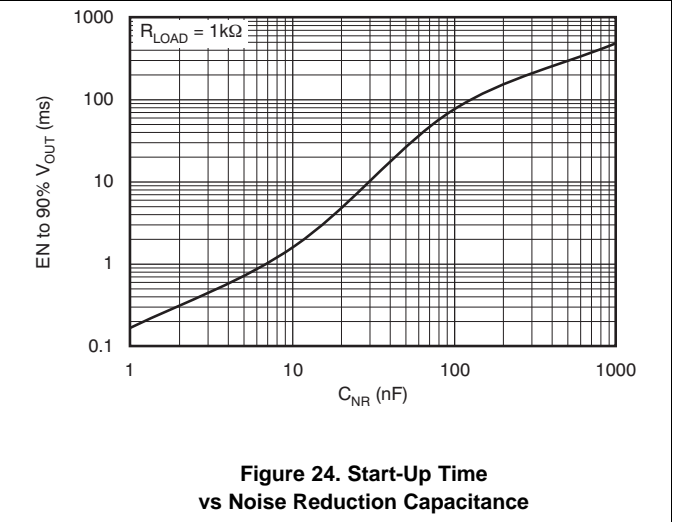
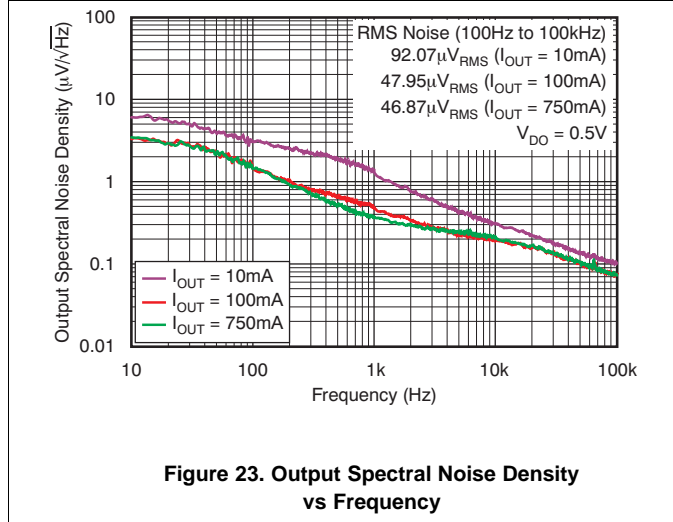
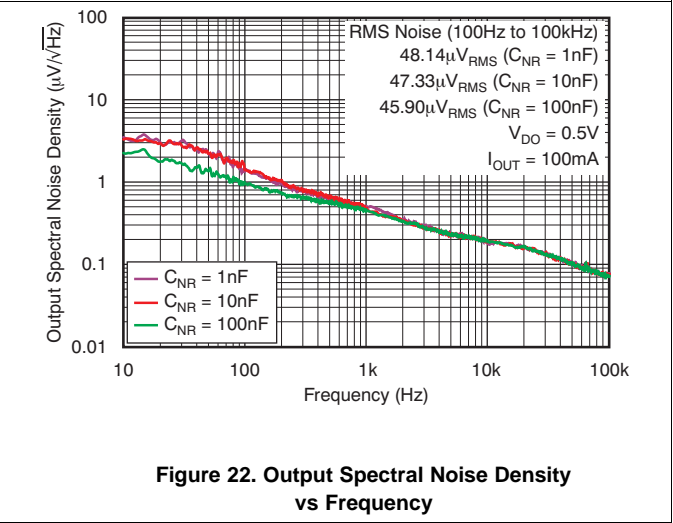
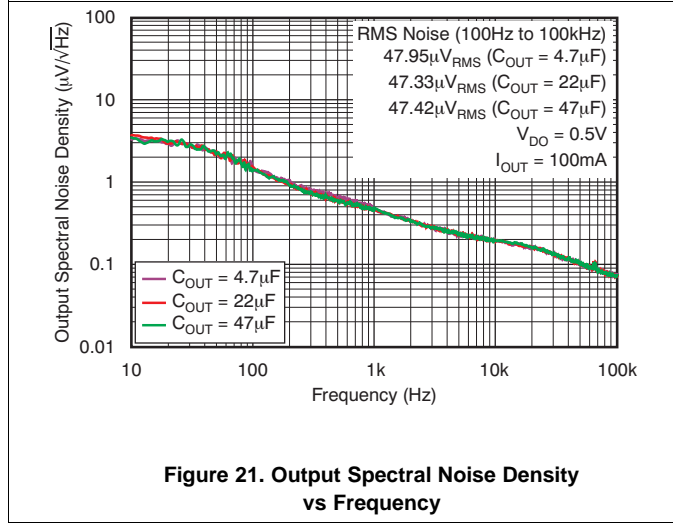
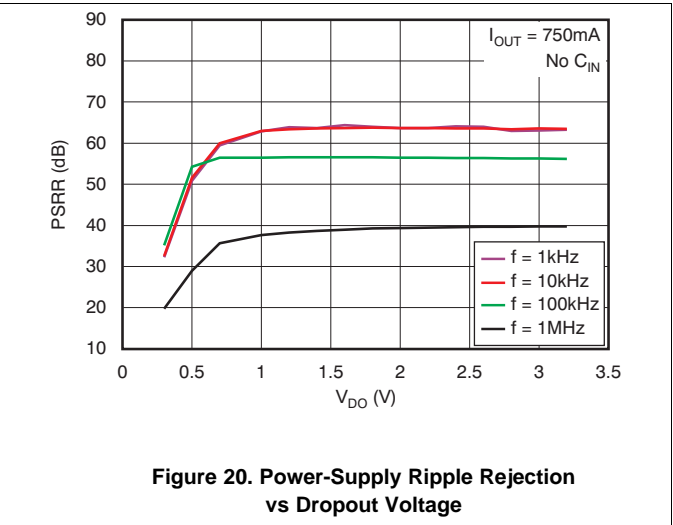
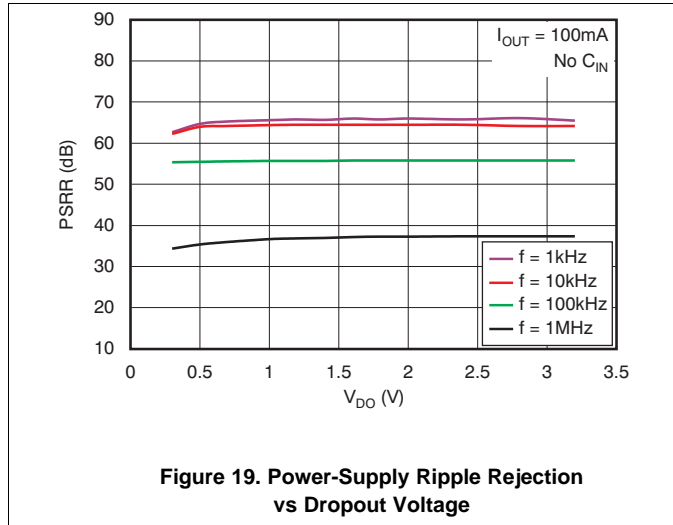


Figure 18. Power-Supply Ripple Rejection vs Frequency

Typical Characteristics (continued)

At  $V_{OUT(TYP)} = 3.3\text{ V}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.2\text{ V}$  (whichever is greater),  $I_{OUT} = 100\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ , and  $C_{NR} = 0.01\text{ }\mu\text{F}$ , all temperature values refer to  $T_J$ , unless otherwise noted.



### Typical Characteristics (continued)

At  $V_{OUT(TYP)} = 3.3\text{ V}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$  or  $2.2\text{ V}$  (whichever is greater),  $I_{OUT} = 100\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ , and  $C_{NR} = 0.01\text{ }\mu\text{F}$ , all temperature values refer to  $T_J$ , unless otherwise noted.

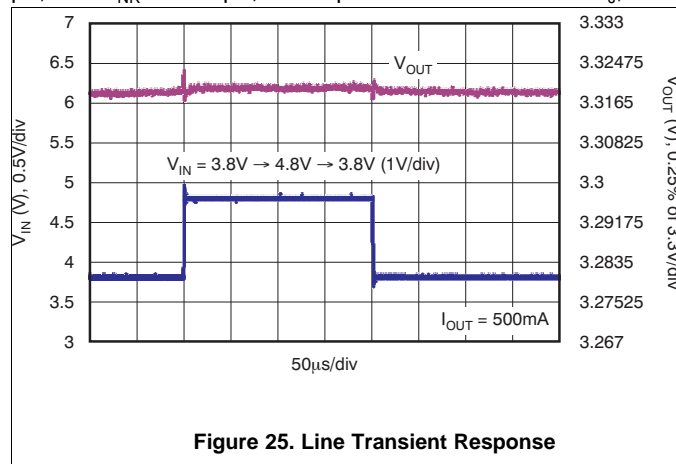


Figure 25. Line Transient Response

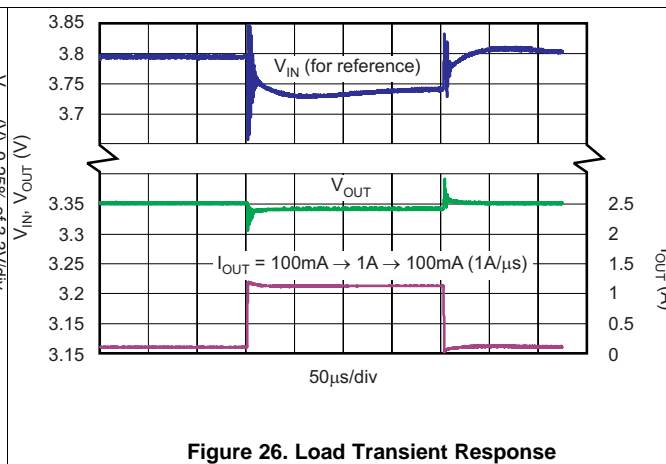


Figure 26. Load Transient Response

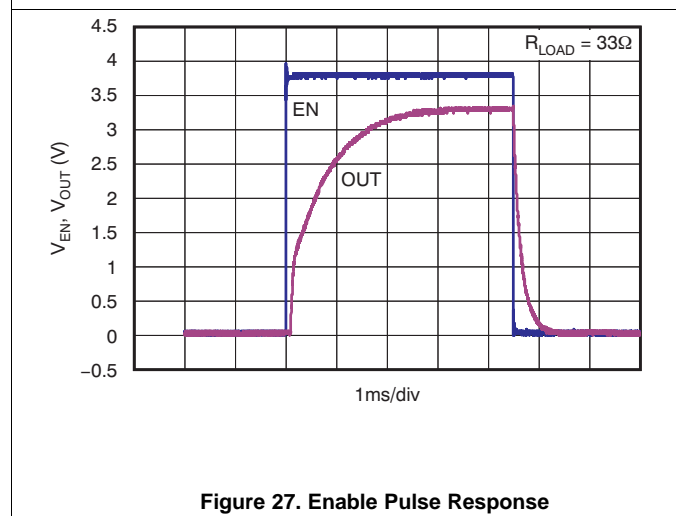
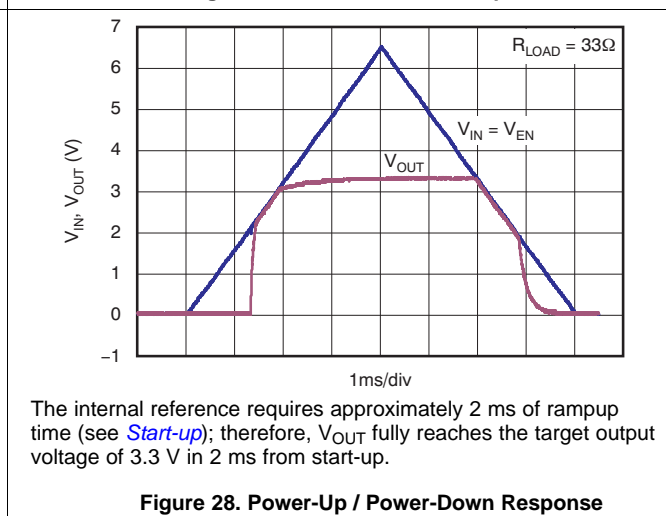


Figure 27. Enable Pulse Response



The internal reference requires approximately 2 ms of rampup time (see [Start-up](#)); therefore,  $V_{OUT}$  fully reaches the target output voltage of 3.3 V in 2 ms from start-up.

Figure 28. Power-Up / Power-Down Response

## 7 Detailed Description

### 7.1 Overview

The TPS7A8001 device belongs to a family of new-generation LDO regulators that use innovative circuitry to achieve wide bandwidth and high loop gain, resulting in extremely high PSRR (over a 1-MHz range) even with very low headroom ( $V_I - V_O$ ). A noise-reduction capacitor ( $C(NR)$ ) at the NR pin and a bypass capacitor ( $C(BYPASS)$ ) decrease noise generated by the bandgap reference to improve PSRR, while a quick-start circuit fastcharges the noise-reduction capacitor. This family of regulators offers sub-bandgap output voltages, current limit, and thermal protection, and is fully specified from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### 7.2 Functional Block Diagram

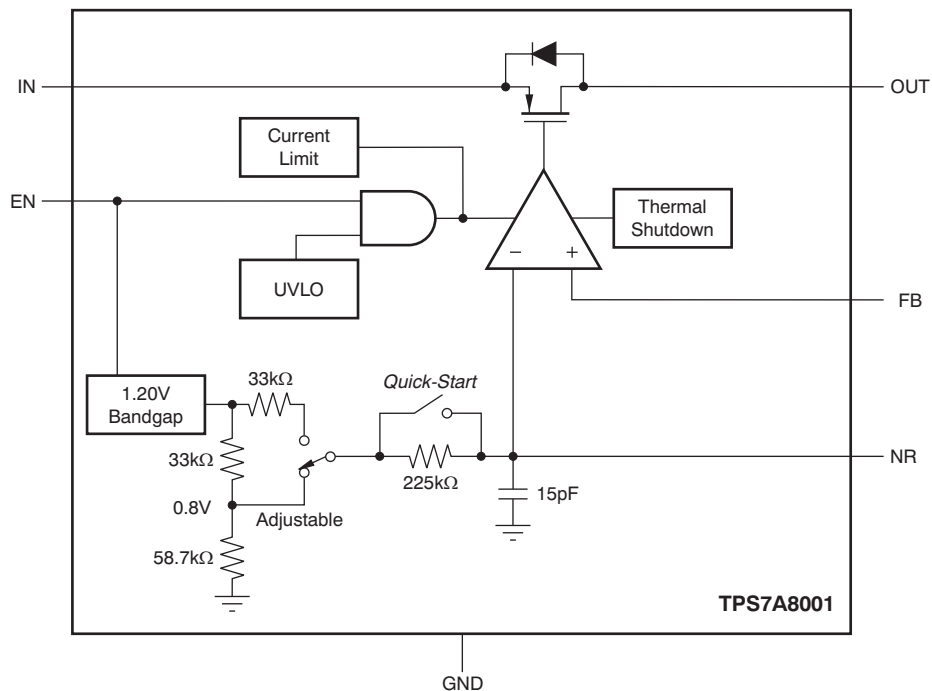


Figure 29. Adjustable Voltage Version

### 7.3 Feature Description

#### 7.3.1 Internal Current Limit

The TPS7A8001 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS7A8001 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting is required.

#### 7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

## Feature Description (continued)

### 7.3.3 Start-up

Through a lower resistance, the bandgap reference can quickly charge the noise reduction capacitor ( $C_{NR}$ ). The TPS7A8001 has a *quick-start* circuit to quickly charge  $C_{NR}$ , if present; see the [Functional Block Diagram](#). At start-up, this quick-start switch is closed, with only 33 k $\Omega$  of resistance between the bandgap reference and the NR pin. The quick-start switch opens approximately 2ms after any device enabling event, and the resistance between the bandgap reference and the NR pin becomes higher in value (approximately 250 k $\Omega$ ) to form a very good low-pass (RC) filter. This low-pass filter achieves very good noise reduction for the reference voltage.

Inrush current can be a problem in many applications. The 33-k $\Omega$  resistance during the start-up period is intentionally put there to slow down the reference voltage ramp up, thus reducing the inrush current. For example, the capacitance of connecting the recommended  $C_{NR}$  value of 0.01  $\mu$ F along with the 33-k $\Omega$  resistance causes approximately 1-ms RC delay. Start-up time with the other  $C_{NR}$  values can be calculated as:

$$t_{STR} \text{ (s)} = 76,000 \times C_{NR} \text{ (F)} \quad (1)$$

[Equation 1](#) is valid up to  $t_{STR} = 2 \text{ ms}$  or  $C_{NR} = 26 \text{ nF}$ , whichever is smaller.

Although the noise reduction effect is nearly saturated at 0.01  $\mu$ F, connecting a  $C_{NR}$  value greater than 0.01  $\mu$ F can help reduce noise slightly more; however, start-up time will be extremely long because the quick-start switch opens after approximately 2ms. That is, if  $C_{NR}$  is not fully charged during this 2 ms period,  $C_{NR}$  finishes charging through a higher resistance of 250 k $\Omega$ , and takes much longer to fully charge.

A low leakage  $C_{NR}$  should be used; most ceramic capacitors are suitable.

### 7.3.4 Undervoltage Lock-Out (UVLO)

The TPS7A8001 uses an undervoltage lock-out circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 50- $\mu$ s duration.

## 7.4 Device Functional Modes

Driving the EN pin over 1.2 V for  $V_I$  from 2.2 V to 3.6 V or 1.35 V for  $V_I$  from 3.6 V to 6.5 V turns on the regulator. Driving the EN pin below 0.4 V causes the regulator to enter shutdown mode.

In shutdown, the current consumption of the device is reduced to 0.02  $\mu$ A typically.

## 8 Application and Implementation

### NOTE

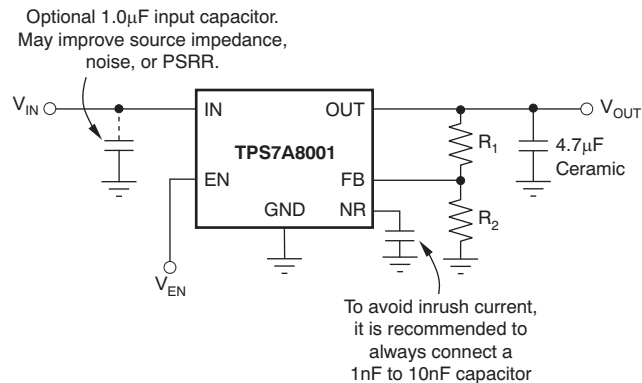
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7A8001 belongs to a family of new generation LDO regulators that use innovative circuitry to achieve wide bandwidth and high loop gain, resulting in extremely high PSRR (over a 1-MHz range) at very low headroom ( $V_{IN} - V_{OUT}$ ). A noise reduction capacitor ( $C_{NR}$ ) at the NR pin bypasses noise generated by the bandgap reference to improve PSRR, while a quick-start circuit fast-charges this capacitor. This family of regulators offers sub-bandgap output voltages, current limit, and thermal protection, and is fully specified from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

Figure 30 gives the connections for the adjustable output version (TPS7A8001).

### 8.2 Typical Application



**Figure 30. Typical Application Circuit (Adjustable Voltage Version)**

#### 8.2.1 Design Requirements

##### 8.2.1.1 Dropout Voltage

The TPS7A8001 uses a PMOS pass transistor to achieve low dropout. When ( $V_{IN} - V_{OUT}$ ) is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  scales approximately with output current because the PMOS device in dropout behaves the same way as a resistor.

As with any linear regulator, PSRR and transient response are degraded as ( $V_{IN} - V_{OUT}$ ) approaches dropout. This effect is shown in Figure 19 and Figure 20 in the *Typical Characteristics* section.

##### 8.2.1.2 Minimum Load

The TPS7A8001 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS7A8001 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

## Typical Application (continued)

### 8.2.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1- $\mu\text{F}$  to 1- $\mu\text{F}$  low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1- $\mu\text{F}$  input capacitor may be necessary to ensure stability.

The TPS7A8001 is designed to be stable with standard ceramic capacitors of capacitance values 4.7  $\mu\text{F}$  or larger. This device is evaluated using a 4.7- $\mu\text{F}$  ceramic capacitor of 10-V rating, 10% tolerance, X5R type, and 0805 size (2 mm  $\times$  1.25 mm).

X5R- and X7R-type capacitors are highly recommended because they have minimal variation in value and ESR over temperature. Maximum ESR should be  $<1 \Omega$ .

The TPS7A8001 implements an innovative internal compensation circuit that does not require a feedback capacitor across  $R_2$  for stability. A feedback capacitor should not be used for this device.

### 8.2.1.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

## 8.2.2 Detailed Design Procedure

The voltage on the FB pin sets the output voltage and is determined by the values of  $R_1$  and  $R_2$ . The values of  $R_1$  and  $R_2$  can be calculated for any voltage using the formula given in [Equation 2](#):

$$V_{\text{OUT}} = \frac{(R_1 + R_2)}{R_2} \times 0.800 \quad (2)$$

Sample resistor values for common output voltages are shown in [Table 1](#). In [Table 1](#), E96 series resistors are used, and all values meet 1% of the target  $V_{\text{OUT}}$ , assuming resistors with zero error. For the actual design, pay attention to any resistor error factors. Using lower values for  $R_1$  and  $R_2$  reduces the noise injected from the FB pin.

**Table 1. Sample 1% Resistor Values for Common Output Voltages**

$V_{\text{OUT}}$	$R_1$	$R_2$
0.8 V	0 $\Omega$ (Short)	Do not populate
1 V	2.49 k $\Omega$	10 k $\Omega$
1.2 V	4.99 k $\Omega$	10 k $\Omega$
1.5 V	8.87 k $\Omega$	10 k $\Omega$
1.8 V	12.5 k $\Omega$	10 k $\Omega$
2.5 V	21 k $\Omega$	10 k $\Omega$
3.3 V	30.9 k $\Omega$	10 k $\Omega$
5 V	52.3 k $\Omega$	10 k $\Omega$

### 8.2.2.1 Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor ( $C_{\text{NR}}$ ) is used with the TPS7A8001, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01- $\mu\text{F}$  (minimum) noise-reduction capacitor.

[Equation 3](#) approximates the total noise when  $C_{\text{NR}} = 0.01 \mu\text{F}$ :

$$V_{\text{N}} = 14.6 \times V_{\text{OUT}} + (\mu\text{V}_{\text{RMS}}) \quad (3)$$

Typical Application (continued)

8.2.3 Application Curve

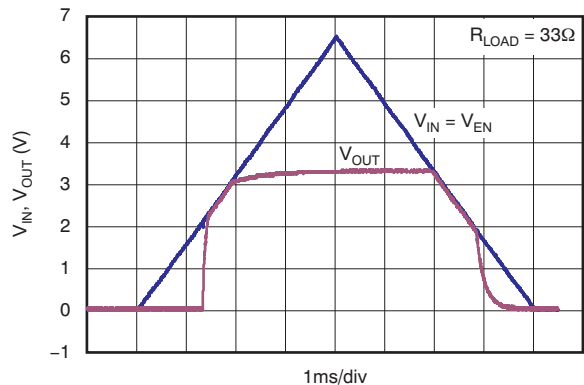


Figure 31. Power-Up / Power-Down Response

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.2 V to 6.5 V. The input voltage range should provide adequate headroom for the device to have a regulated output. This input supply should be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.



## 10 Layout

### 10.1 Layout Guidelines

#### 10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

#### 10.2 Layout Example

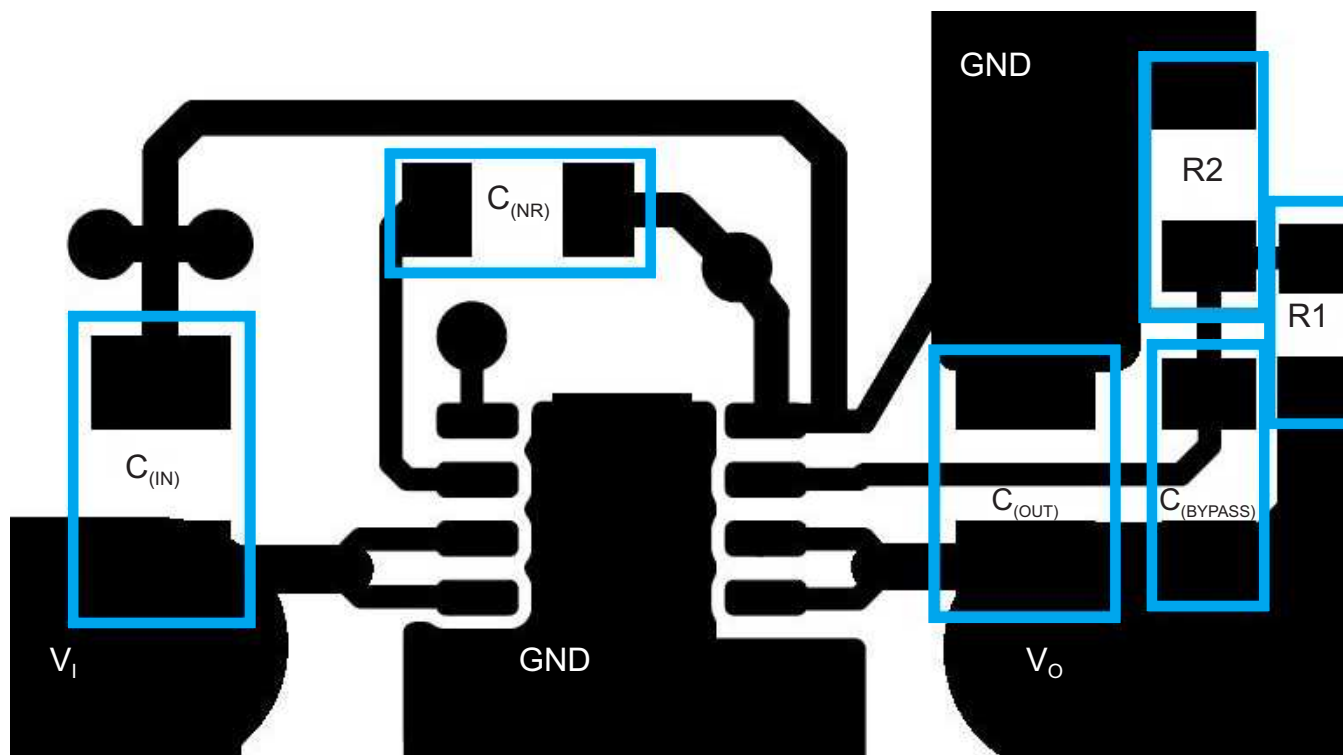


Figure 32. TPS7A8001 Layout Example

#### 10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A8001 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A8001 into thermal shutdown degrades device reliability.

### 10.4 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

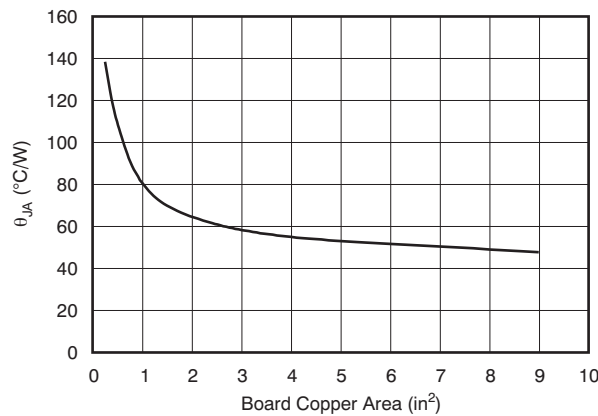
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{4}$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the VSON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed-circuit-board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125^{\circ}\text{C} - T_A)}{P_D} \tag{5}$$

Knowing the maximum  $R_{\theta JA}$ , the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 33.



Note:  $\theta_{JA}$  value at board size of 9in<sup>2</sup> (that is, 3 inches × 3 inches) is a JEDEC standard.

**Figure 33.  $R_{\theta JA}$  vs Board Size**

Figure 33 shows the variation of  $\theta_{JA}$  as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

**NOTE**

When the device is mounted on an application PCB, it is strongly recommended to use  $\Psi_{JT}$  and  $\Psi_{JB}$ , as explained in the section.

### 10.5 Estimating Junction Temperature

Using the thermal metrics  $\Psi_{JT}$  and  $\Psi_{JB}$ , as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older  $\theta_{JC, Top}$  parameter is listed as well.

$$\begin{aligned} \Psi_{JT}: \quad T_J &= T_T + \Psi_{JT} \cdot P_D \\ \Psi_{JB}: \quad T_J &= T_B + \Psi_{JB} \cdot P_D \end{aligned} \tag{6}$$

## Estimating Junction Temperature (continued)

Where  $P_D$  is the power dissipation shown by Equation 5,  $T_T$  is the temperature at the center-top of the IC package, and  $T_B$  is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 35 shows).

### NOTE

Both  $T_T$  and  $T_B$  can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring  $T_T$  and  $T_B$ , see the application note [SBVA025](#), *Using New Thermal Metrics*, available for download at [www.ti.com](http://www.ti.com).

By looking at Figure 34, the new thermal metrics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) have very little dependency on board size. That is, using  $\Psi_{JT}$  or  $\Psi_{JB}$  with Equation 6 is a good way to estimate  $T_J$  by simply measuring  $T_T$  or  $T_B$ , regardless of the application board size.

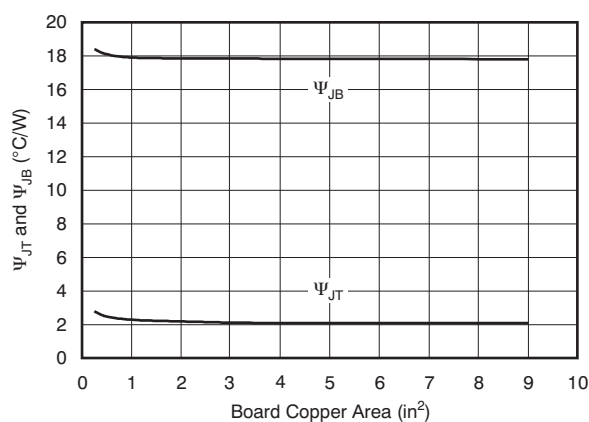


Figure 34.  $\Psi_{JT}$  and  $\Psi_{JB}$  vs Board Size

For a more detailed discussion of why TI does not recommend using  $\theta_{JC(top)}$  to determine thermal characteristics, refer to application report [SBVA025](#), *Using New Thermal Metrics*, available for download at [www.ti.com](http://www.ti.com). For further information, refer to application report [SPRA953](#), *Semiconductor and IC Package Thermal Metrics*, also available on the TI website.

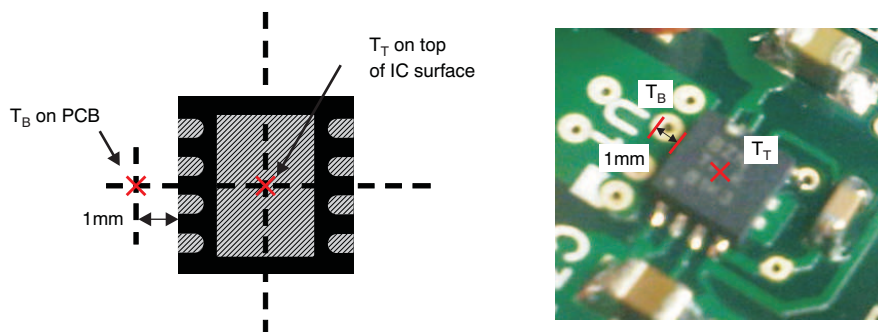


Figure 35. Measuring Points for  $T_T$  and  $T_B$

## 11 Device and Documentation Support

### 11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.2 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A8001DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFU	<a href="#">Samples</a>
TPS7A8001DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFU	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

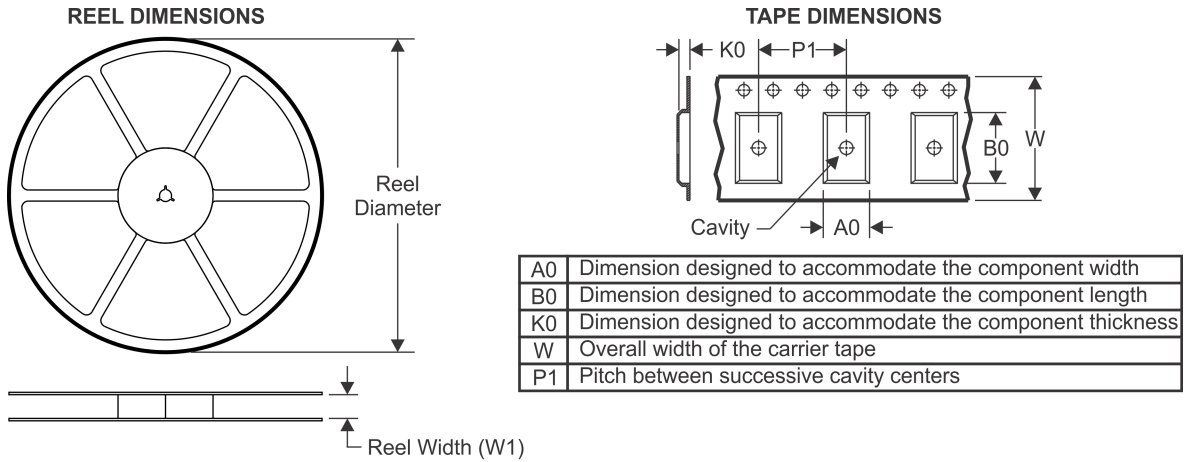
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

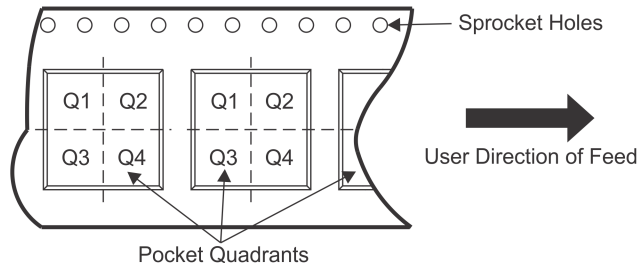
**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



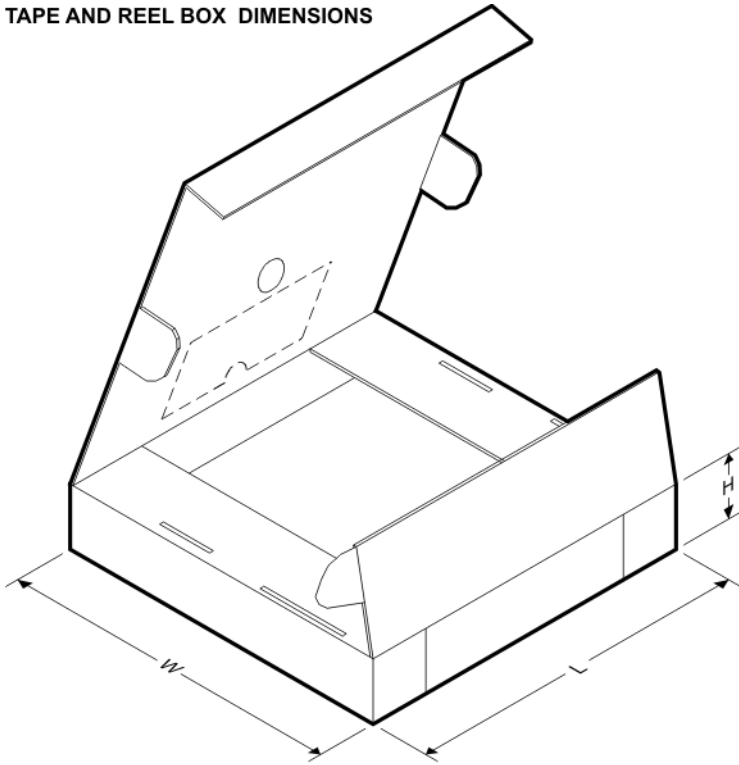
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A8001DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A8001DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

# PACKAGE MATERIALS INFORMATION

10-Jan-2018

## TAPE AND REEL BOX DIMENSIONS

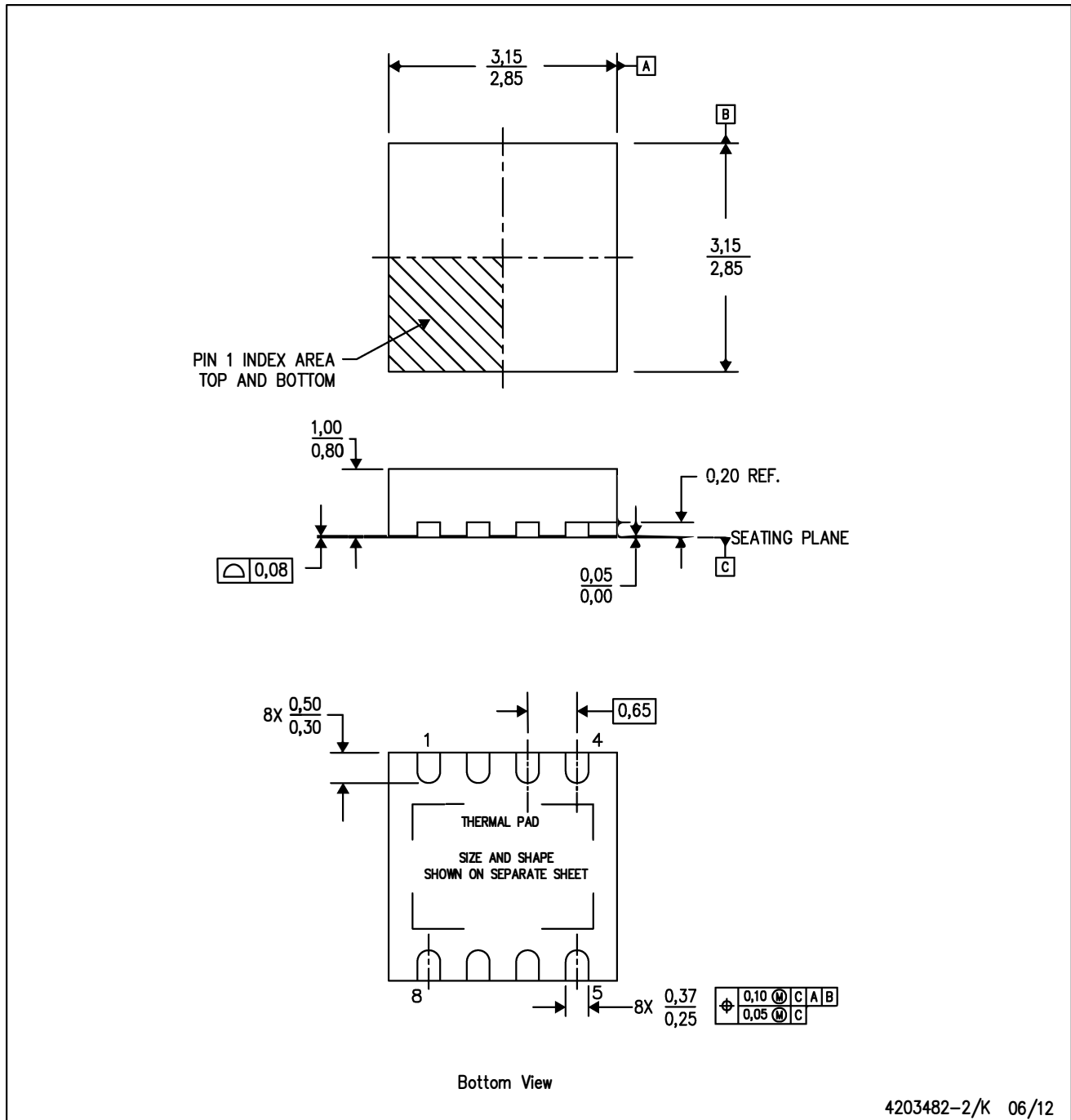


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A8001DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS7A8001DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.



# THERMAL PAD MECHANICAL DATA

DRB (S-PVSON-N8)

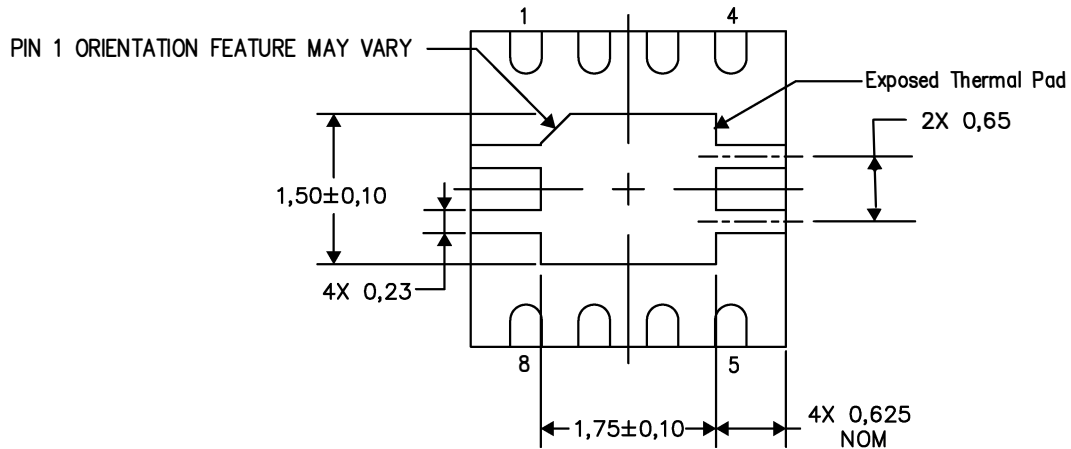
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

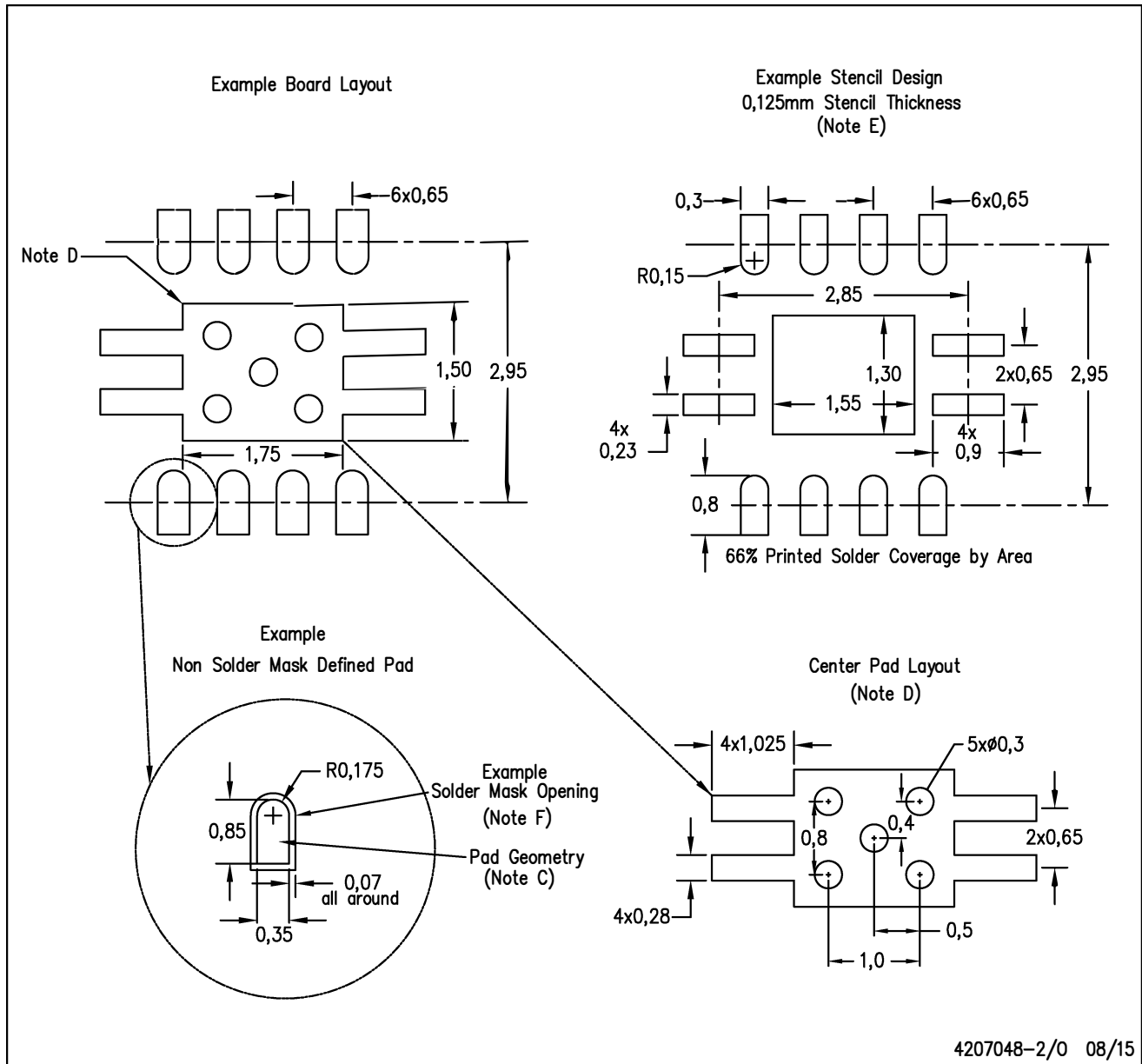
Exposed Thermal Pad Dimensions

4206340-2/T 08/15

NOTE: All linear dimensions are in millimeters

DRB (S-PVSON-N8)

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4207048-2/0 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.