MXD8666HF

High Power SP6T for 2G/3G/4G Applications

Description

The MXD8666HF is a low loss, high power SP6T switch for 2G/3G/4G TRX applications.

The MXD8666HF is compatible with MIPI control, which is a key requirement for many cellular transceivers. This part is packaged in a compact 2mm x 2mm, 14-pin, QFN package which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Features

- Multi-Band operation 0.4 to 3.8GHz
- Excellent insertion loss 0.55 dB @2.7GHz
- Input 0.1dB compression point: 36dBm
- RFFE serial control interface
- No external DC blocking Capacitors required on RF signal paths unless DC is applied externally
- Compact 2mm x 2mm in QFN-14 package, MSL1

Applications

- 2G/3G/4G antenna diversity
- Cellular modems and USB Devices

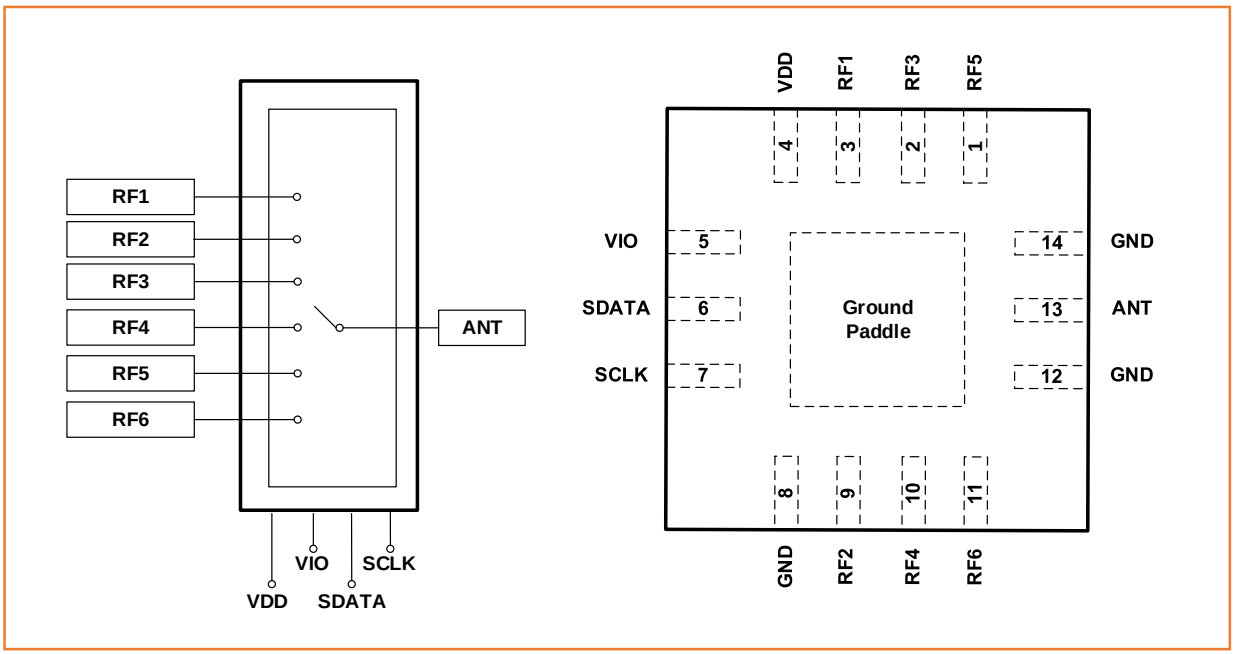


Figure 1 Functional Block Diagram and Pin Configuration

Function Characteristics

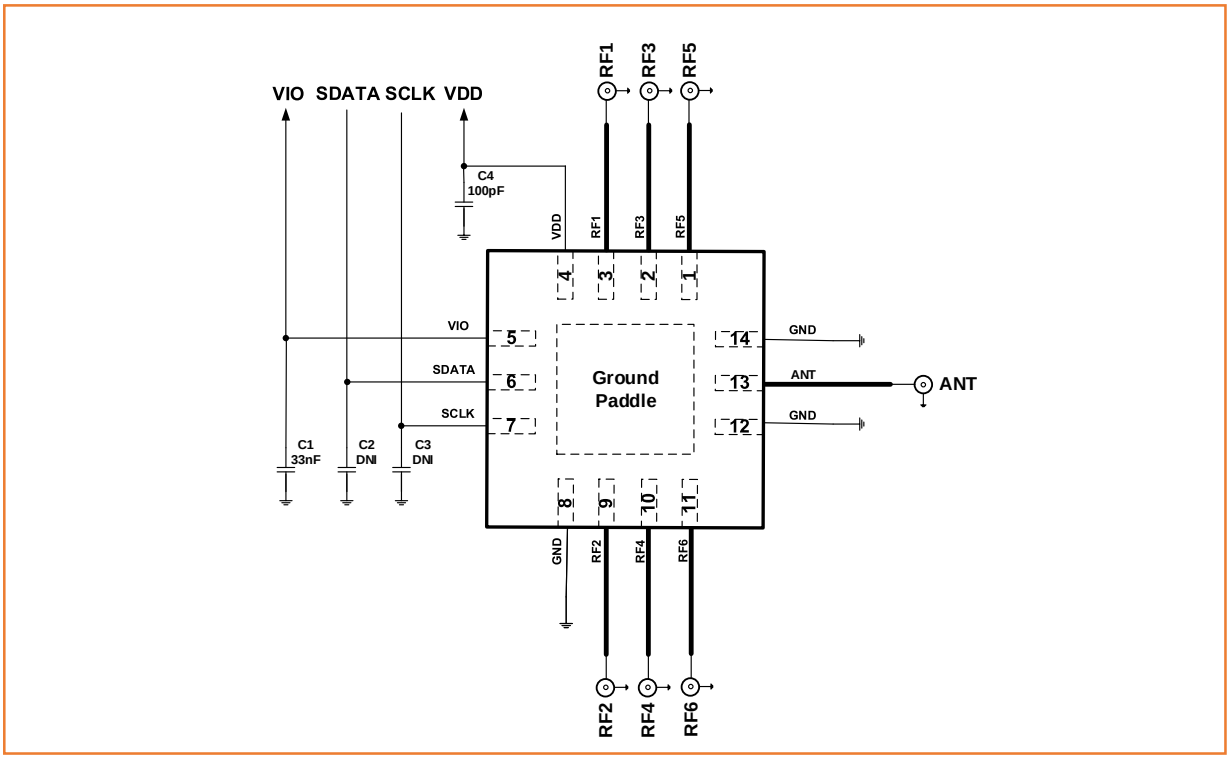


Figure 2 Application Circuit

Table 1 Pin Descriptions

NO.	Name	Description	NO.	Name	Description
1	RF5	RF Port5	8	GND	Ground
2	RF3	RF Port3	9	RF2	RF Port2
3	RF1	RF Port1	10	RF4	RF Port4
4	VDD	Power Supply Voltage	11	RF6	RF Port6
5	VIO	Supply Voltage for MIPI	12	GND	Ground
6	SDATA	MIPI Data Input/output	13	ANT	Antenna Port
7	SCLK	MIPI Clock	14	GND	Ground
Ground Paddle	GND	Ground			

Table 2 D[7:0] (Register_0) for RF Operating Mode

Control	Switched RF Outputs					
Register_0	RF1	RF2	RF3	RF4	RF5	RF6
0x07	Insertion Loss	Isolation	Isolation	Isolation	Isolation	Isolation
0x06	Isolation	Insertion Loss	Isolation	Isolation	Isolation	Isolation
0x0B	Isolation	Isolation	Insertion Loss	Isolation	Isolation	Isolation
0x0C	Isolation	Isolation	Isolation	Insertion Loss	Isolation	Isolation
0x0A	Isolation	Isolation	Isolation	Isolation	Insertion Loss	Isolation
0x04	Isolation	Isolation	Isolation	Isolation	Isolation	Insertion Loss

Electrical Characteristics

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition
DC Supply Voltage	V_{DD}	-0.3	+3.3	V	T_A=25℃
Supply Voltage For MIPI	V_{IO}	-0.3	+2.5		T_A=25℃
MIPI Logic Voltage(SDATA, SCLK)	V_I	-0.3	+2.5		T_A=25℃
Peak RF Input Power	P_{IN}		+36.5	dBm	20% Duty Cycle Mode T_A=25℃
Device Operating Temperature	T_{OP}	-40	+90	℃	
Device Storage Temperature	T_{STG}	-55	+150		
Electrostatic Discharge	$V_{ESD(HBM)}$	1000		V	Human Body Model (HBM), Class 1C
	$V_{ESD(CDM)}$	500			Charged Device Model (CDM), Class III

Notice

Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

Table 4 Recommended Operating Conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Frequency	F_0	0.4		3.8	GHz
DC Supply Voltage	V_{DD}	2.5	2.8	3.0	V
Supply Voltage For MIPI	V_{IO}	1.62	1.8	1.98	
MIPI Logic Voltage(SDATA, SCLK) High	V_{IH}	0.8*VIO	VIO	VIO	
MIPI Logic Voltage(SDATA, SCLK) Low	V_{IL}	0	0	0.3	

Table 5 Nominal Operating Parameters

Parameter	Symbol	Specification			Unit	Condition
		MIN	TYP	MAX		
Normal Condition	V_{DD}=2.8V, V_{IO}=1.8V, V_{IH}=1.8V, V_{IH}=0V, P_{IN}=0dBm, Z_O=50Ω, T_A=25℃, Unless Otherwise Stated					
DC Performances						
DC Supply Current	I_{DD}		80	100	μA	
Current on VIO	I_{IO}		4	10		
Timing Performances						
Switching Speed	T_{SW}		1	2	μs	End of MIPI Command to 90%/10% RF
Startup Time	T_{ON}			10	μs	MIPI Low Power State to any RF
RF Performances						
Insertion loss (ANT to RF1~6)	IL		0.45	0.50	dB	F_0=0.4 to 1.0GHz
			0.50	0.55		F_0=1.1 to 2.0GHz
			0.55	0.60		F_0=2.1 to 2.7GHz
			0.65	0.75		F_0=3.4 to 3.8GHz
Isolation (ANT to RF1~6)	ISO	35	38			F_0=0.4 to 1.0GHz
		25	30			F_0=1.1 to 2.0GHz
		20	24			F_0=2.1 to 2.7GHz
		18	21			F_0=3.4 to 3.8GHz
Input Return Loss (ANT to RF1~6)	RL	20	25			F_0=0.4 to 1.0GHz
		17	22			F_0=1.1 to 2.0GHz
		15	17			F_0=2.1 to 2.7GHz
		12	15			F_0=3.4 to 3.8GHz
Input 0.1dB Compression Point (ANT to RF1~6)	$P_{0.1dB}$		+36		dBm	F_0=950MHz, 20% DC
2nd Harmonic	$2F_0$		-85	-80	dBc	F_0=0.4 to 3.8GHz @+27dBm
3rd Harmonic	$3F_0$		-85	-80	dBc	F_0=0.4 to 3.8GHz @+27dBm
2nd Order Intermodulation	IMD2		-70		dBm	Reference to Table 6
3rd Order Intermodulation	IMD3		-70		dBm	Reference to Table 7

Table 6 IMD2 Test Conditions

Band	In-Band Frequency	CW Carrier		CW Interferer	
	MHz	MHz	dBm	MHz	dBm
1 Low	2140	1950	+20	190	-15
1 High	2140	1950	+20	4090	-15
5 Low	881.5	836.5	+20	45	-15
5 High	881.5	836.5	+20	1718	-15

Table 7 IMD3 Test Conditions

Band	In-Band Frequency	CW Carrier		CW Interferer	
	MHz	MHz	dBm	MHz	dBm
1 LOW	2140	1950	+20	1760	-15
5 HIGH	881.5	836.5	+20	791.5	-15

MIPI Read and Write Timing

MIPI supports the following Command Sequences:

- Register Write
- Register Read
- Register_0 Write

Figures 3 and 4 provide the timing diagrams for register write commands and read commands, respectively. Figure 5 shows the Register_0 Write Command Sequence. Refer to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), V1.10 (26 July 2011) for additional information on MIPI USID programming sequences and MIPI bus specifications.

In the timing figures, SA[3:0] is slave address. A[4:0] is register address. D[7:0] is data. “P” is odd parity bit.

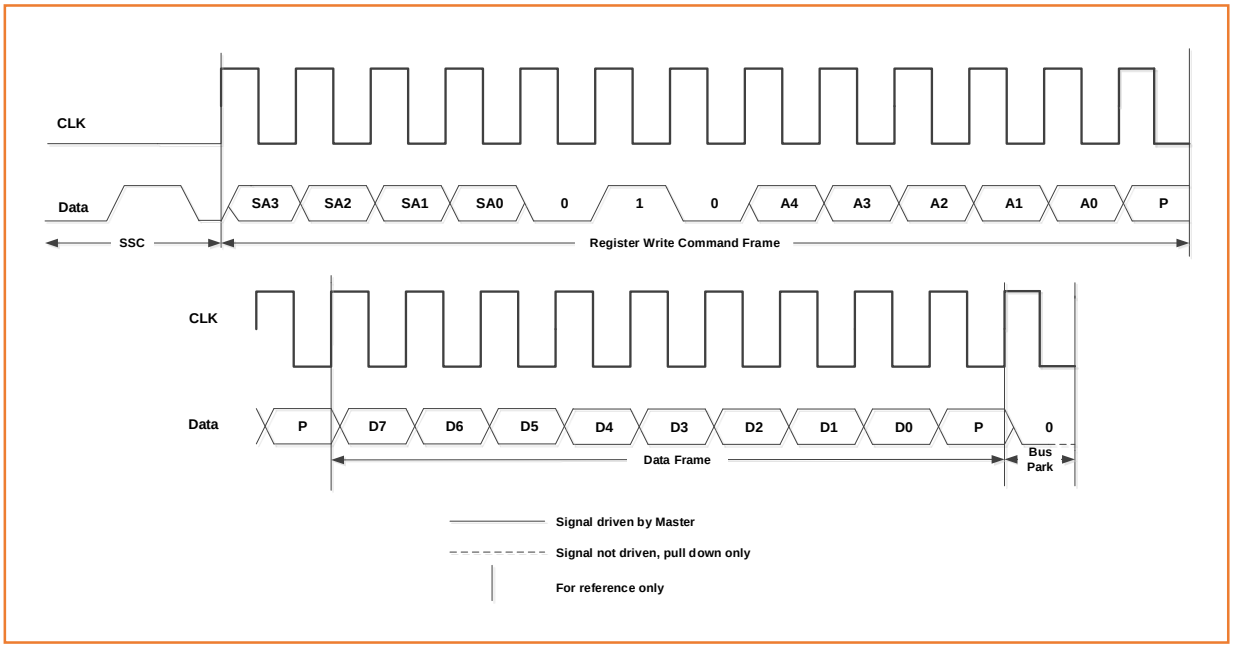


Figure 3 Register Write Command Sequence

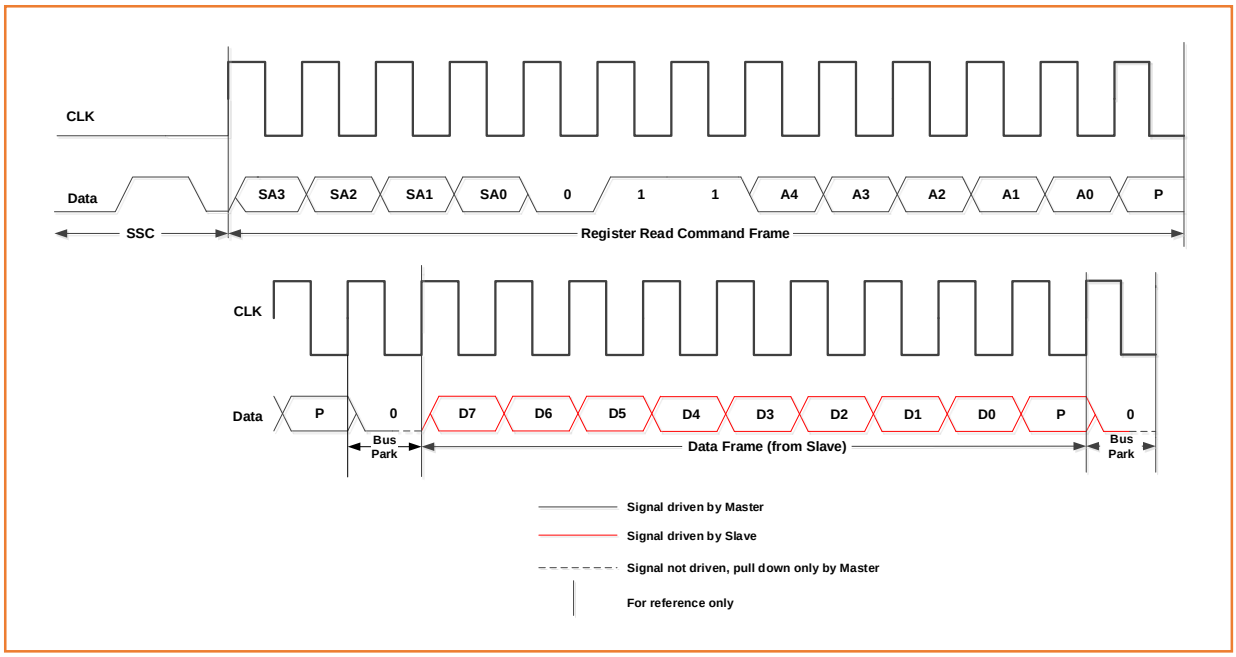


Figure 4 Register Read Command Sequence

Register_0 Write Command Sequence

Figure 5 shows the Register_0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register_0 Write Command Frame containing the Slave address, a logic one, and a seven-bit word to be written to Register_0. The Command Sequence ends with a Bus Park Cycle.

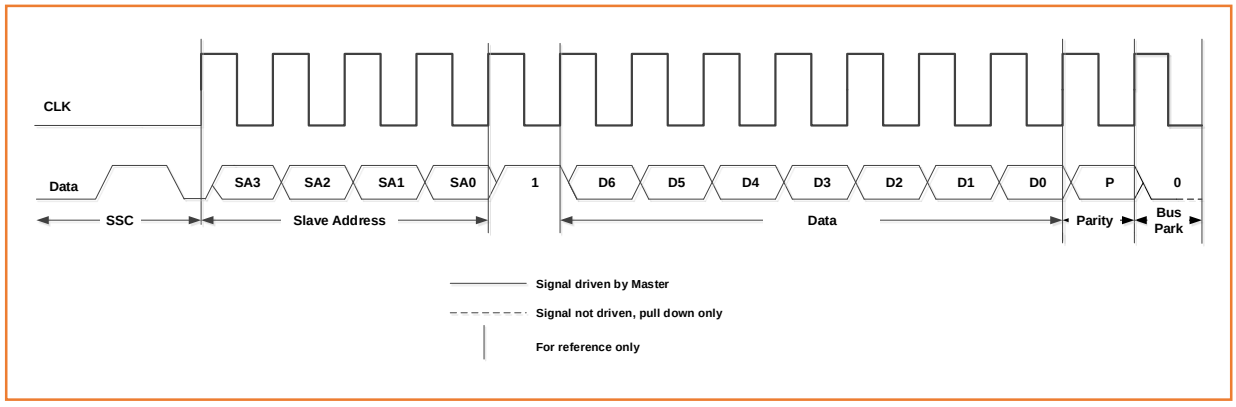


Figure 5 Register_0 Write Command Sequence

Register Definition

Table 8 Register Definition Table

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x0000	REGISTER_0	7:0	R/W	RF Control	Register_0 truth Table: Table 2	0x00	No	Yes
0x001B	GROUP_SID	7:4	R	RESERVED		0x0	No	No
		3:0	R/W	GSID	Group Slave ID	0x0	No	No
0x001C	PM_TRIG	7:6	R/W	PWR_MODE	00: Normal Operation (ACTIVE) 01: Reset all registers to default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved Note: Write PWR_MODE=2'h1 will reset all register, and puts the device into STARTUP state.	0b10	Yes	No
		5	R/W	Trigger_Mask_2	If this bit is set, trigger 2 is disabled	0	No	No
		4	R/W	Trigger_Mask_1	If this bit is set, trigger 1 is disabled	0	No	No
		3	R/W	Trigger_Mask_0	If this bit is set, trigger 0 is disabled Note: When all triggers are disabled, writing to a register that is associated with trigger 0, 1, or 2, causes the data to go directly to the destination register.	0	No	No
		2	W	Trigger_2	A write of a one to this bit loads trigger 2's registers	0	Yes	No
		1	W	Trigger_1	A write of a one to this bit loads trigger 1's registers	0	Yes	No
		0	W	Trigger_0	A write of a one to this bit loads trigger 0's registers Note: Trigger processed immediately then cleared. Trigger 0, 1, and 2 will always read as 0.	0	Yes	No
0x001D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x5d	No	No
0x001E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0x81	No	No
0x001F	MAN_USID	7:6	R	RESERVED		0b00	No	No
		5:4	R	MANUFACTURER_ID[9:8]	Upper two bits of MIPI registered Manufacturer ID	0b11	No	No
		3:0	R/W	USID	USID of the device.	0xb	No	No

Power On and Off Sequence

Here is the recommendation about power-on/off sequence in order to avoid damaging the device.

Power On

1) Apply voltage supply - VDD

2) Apply logic supply - VIO

3) Wait 10μs or longer and then apply MIPI bus signals – SCLK and SDATA

4) Wait 2μs or longer after MIPI bus goes idle and then apply the RF Signal

Power Off

1) Remove the RF Signal

2) Remove MIPI bus – SCLK and SDATA

3) Remove logic supply - VIO

4) Remove voltage supply - VDD

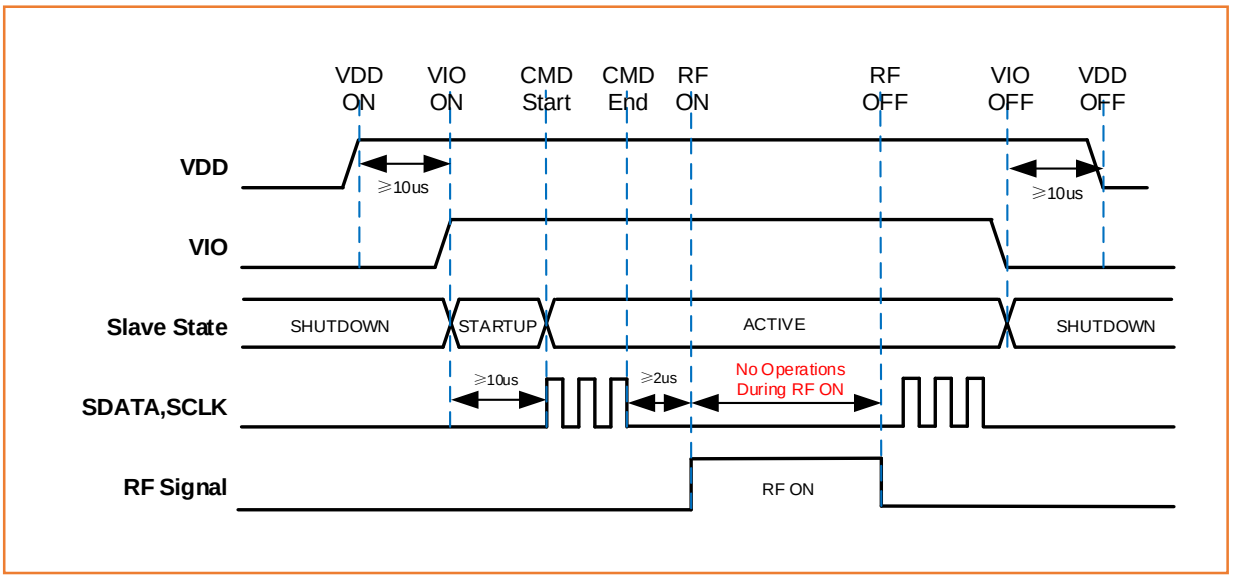


Figure 6 Power On and Off Sequence

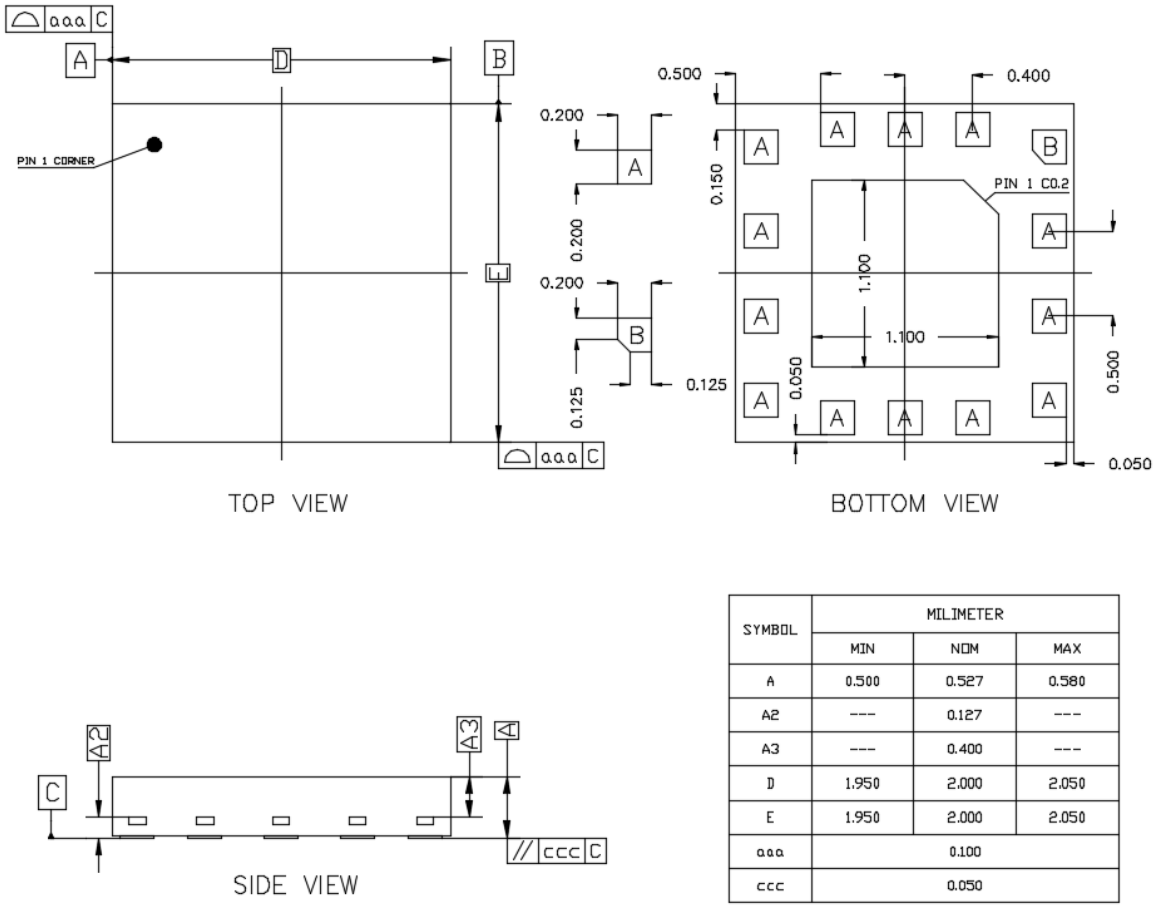
Notice

VIO can be applied to the device before VDD or removed after VDD.

It is important to wait 10μs after VIO & VDD are applied before sending SDATA to ensure correction data transmission.

Operations of SDATA or SCLK are strictly prohibited during RF On period so as to prevent the device being damaged.

Package Outline Dimensions



SYMBOL	MILIMETER		
	MIN	NOM	MAX
A	0.500	0.527	0.580
A2	---	0.127	---
A3	---	0.400	---
D	1.950	2.000	2.050
E	1.950	2.000	2.050
aaa	0.100		
ccc	0.050		

Figure 7 Package Outline Dimensions

Marking Specification

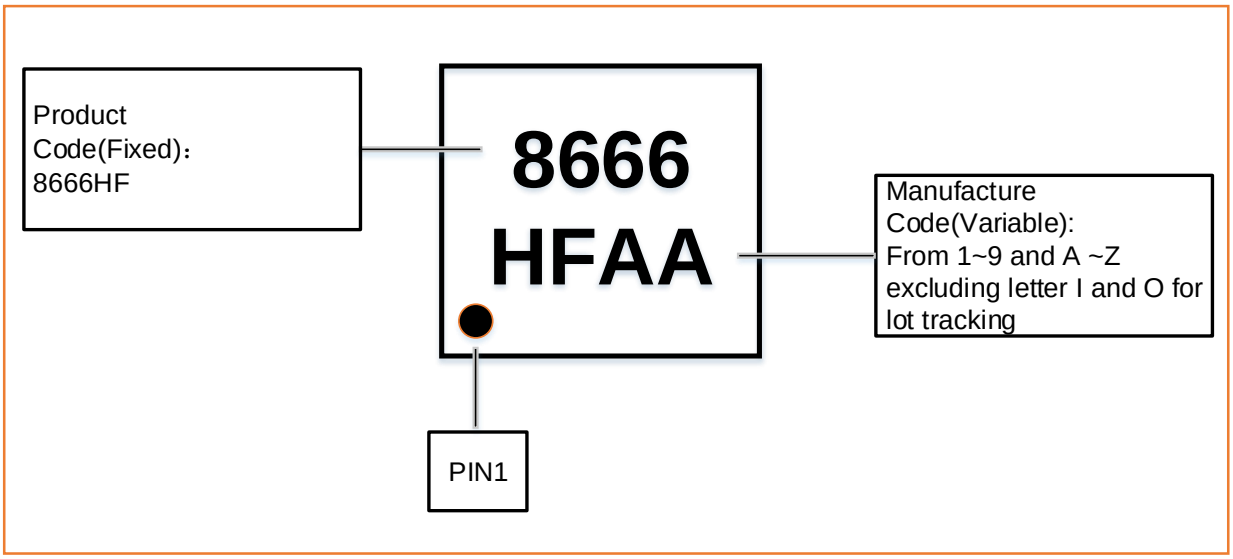


Figure 8 Marking Specification (Top View)

Tape and Reel Dimensions

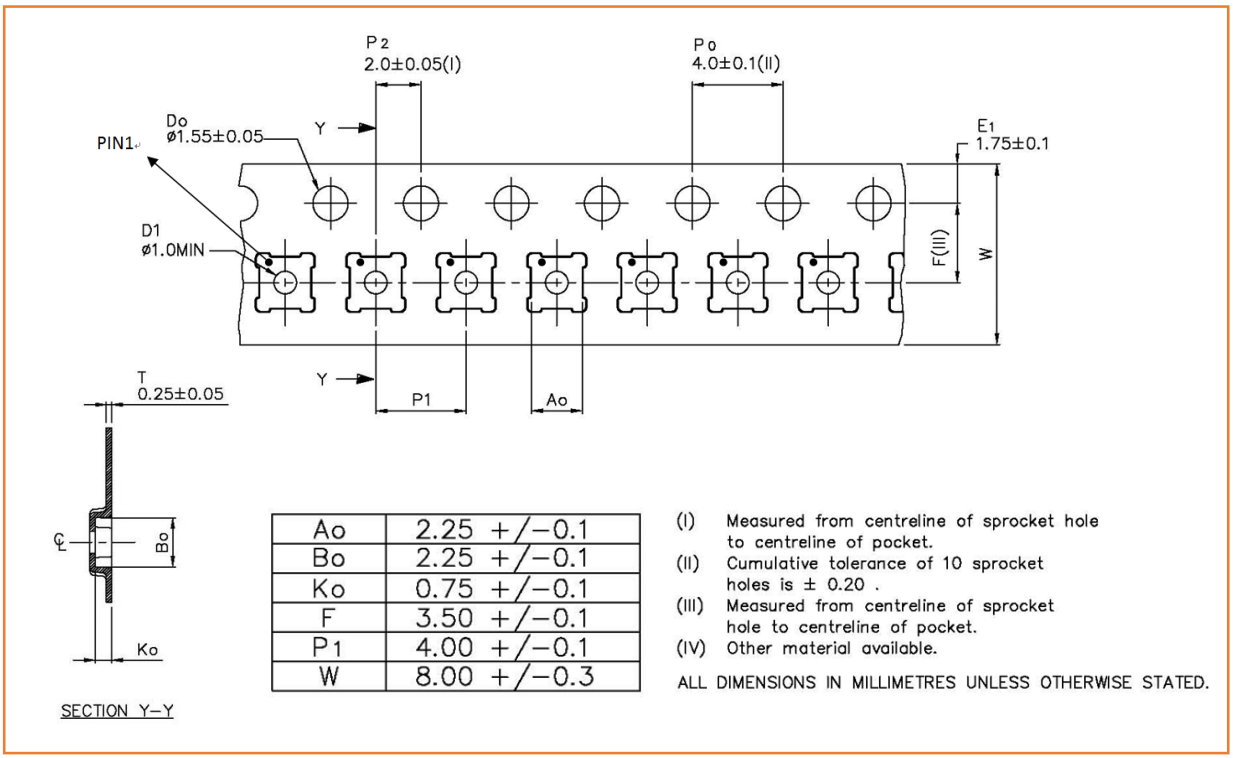


Figure 9 Tape and Reel Dimensions

Reflow Chart

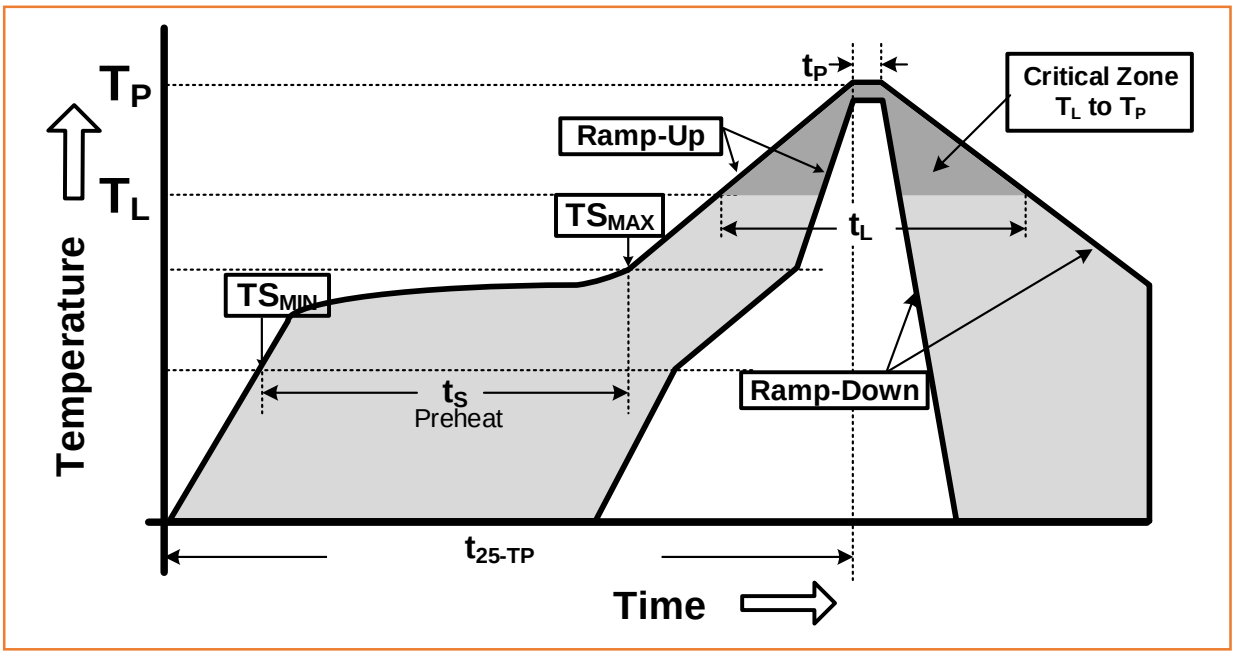


Figure 10 Recommended Lead-Free Reflow Profile

Table 9 Reflow Chart Parameters

Reflow Profile	Parameter
Preheat Temperature(TS_{MIN} to TS_{MAX})	150℃ to 200℃
Preheat Time(ts)	60 to 180 Seconds
Ramp-Up Rate(TS_{MAX} to T_P)	3℃/s MAX
Time Above T_L 217℃(t_L)	60 to 150 Seconds
Peak Temperature (T_P)	260℃
Time within 5℃ of Peak Temperature(t_P)	20 to 40 Seconds
Ramp-Down Rate(TS_{MAX} to T_P)	6℃/s MAX
Time for 25℃ to Peak Temperature($t_{25\text{-}TP}$)	8 Minutes MAX

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be applied when devices are operated.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.