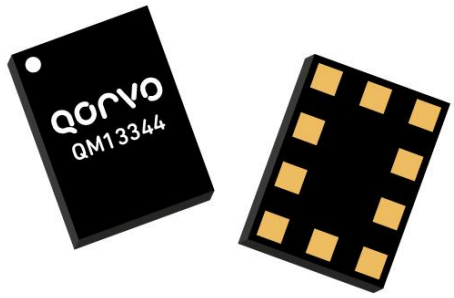
QM13344

4xSPST (Dual Single-Pole-Single-Throw Switch)

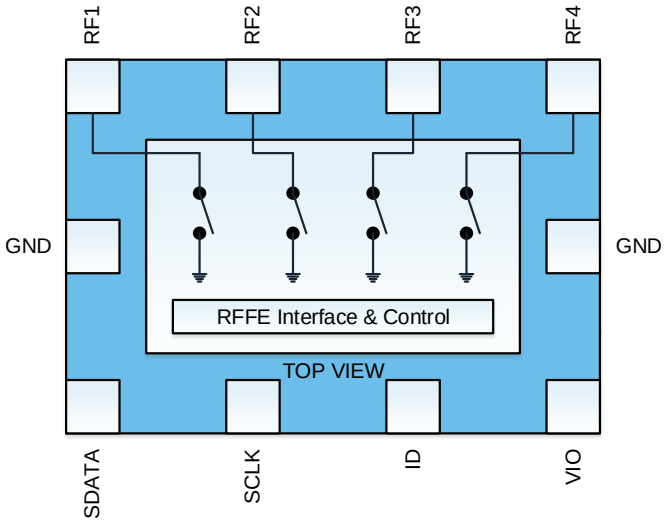
Product Overview

QM13344 is the smallest 4xSPST with VRF >80Vp and very low COFF. Excellent performance in a small solution size enables creation of antenna tuning solutions optimum for 5G applications.



10 Pin 1.1 x 1.5 x 0.4 mm Module Package

Functional Block Diagram



Key Features

- Very low COFF: <95fF
- Very high RF voltage handling capability: >80Vp
- 3 unique selectable USID using external pin, ID
- Small size 1.1mm x 1.5mm, module package
- > 2kV HBM ESD Protection on all pins
- RFFE 2.1 capable
- Suitable for all cellular applications including 5G with broadband performance up to 6GHz

Applications

- Antenna Tuning
- Band Switching
- Impedance Tuning

Ordering Information

Part Number	Description
QM13344SB	5-pc Sample Bag
QM13344SR	100-pc, 7” Reel
QM13344TR13	10000-pc, 13” Reel
QM13344DK	Design Kit with EVB and 5-pc Sample Bag

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-40 to 150 °C
Operating Temperature	-30 to 90 °C
V_{IO},SDATA, SCLK	2.5V
Max RF Voltage between RFC port and Ground (V_{RF}) V_{IO}=1.8V, Temp=25 °C	$80V_P$

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of the Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Recommended Operating Conditions

PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{IO} Supply Voltage	1.65	1.8	1.95	V
I_{VIO} Supply Current (Active Mode)		40		µA
V_{IO} Supply Current (Low Power Mode)		1		µA
SDATA, SCLK Logic High	0.8 x V_{IO}	V_{IO}	1.95	V
SDATA, SCLK Logic Low		0		V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{IO} = 1.8V, SDATA/SCLK = 1.8 V / 0 V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
R_{ON}	ON-State		1.95		Ω
C_{OFF}	OFF-State		95		fF
Second Harmonic	fo = 700MHz; Pin = 23dBm		-108		dBm
Third Harmonic			-117		dBm
Second Harmonic	fo = 915MHz; Pin = 35dBm		-90		dBm
Third Harmonic			-81		dBm
Second Harmonic	fo = 1910MHz; Pin = 33dBm		-84		dBm
Third Harmonic			-91		dBm
Second Harmonic	fo = 2570MHz; Pin = 23dBm		-76		dBm
Third Harmonic			-94		dBm
ON Switching Time	End of Register Write to 90% final RF Amplitude		10		µs
OFF Switching Time	End of Register Write to 10% final RF Amplitude		10		µs
IIP2	Refer to IIP2 conditions table		135		dBm
IIP3	Refer to IIP3 conditions table		78		dBm

IIP2 Test Conditions

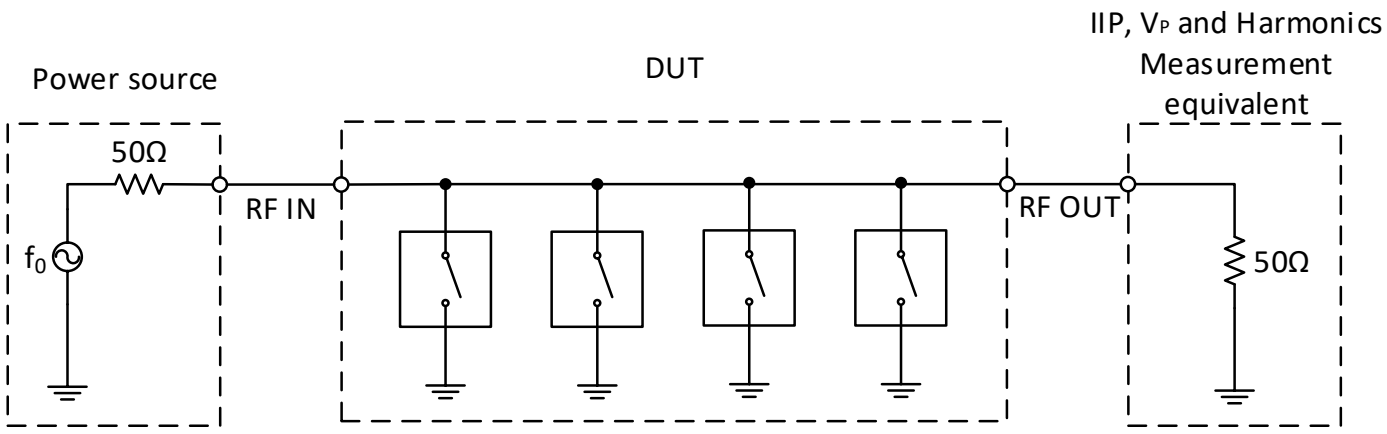
BAND	IN-BAND FREQ	CW TONE 1		CW TONE 2	
	[MHZ]	[MHZ]	[DBM]	[MHZ]	[DBM]
Band I Low	2140	1950	+20	190	-15
Band I High	2140	1950	+20	4090	-15
Band II Low	1960	1880	+20	80	-15
Band II High	1960	1880	+20	3840	-15
Band V Low	881.5	836.5	+20	45	-15
Band V High	881.5	836.5	+20	1718	-15
Band VII Low	942.5	897.5	+20	45	-15
Band VII High	942.5	897.5	+20	1840	-15

IIP3 Test Conditions

BAND	IN-BAND FREQ	CW TONE 1		CW TONE 2	
	[MHZ]	[MHZ]	[DBM]	[MHZ]	[DBM]
Band I	2140	1950	+20	1760	-15
Band V	881.5	836.5	+20	791.5	-15

Test Setup

IIP2, IIP3, V_P and Harmonic Measurement Setup



Power Modes and Triggering & USID_SEL Pin Connection

As per RFFE specification, register 28 is used for setting the power mode of the device and triggering functionality.

- Active Mode – Set register 28 bits D7:D6 to 00. REG_07<7:0>=00XXXXXX
- Low Power Mode – Set register 28 bits D7:D6 to 10. REG_07<7:0>=10XXXXXX

An external pin, ID, on the QM13344 provides the user with an option to set up to 3 of the USID. The ID pin can be used to set the USID to either 0110, 0111 or 1000. The ID pin can be connected to GND, VIO or float.

ID PIN CONNECTION	USID [S3:S0]
Connect to GND	0110
Connect to VIO	0111
float / NC	1000

RFFE MIPI Register Map

Register 0x0000 – ANT_CTRL0

Bit(s)	Field Name	Description		Reset	B/G	Trig	R/WM
7:4	SPARE	Reserved for future use		0x00	No	0 - 10	R/WM
3:0	SP4T[3:0]	Switch Selection		0x0	No	0 - 10	R/WM
		0000: ALL OFF	1000: RF4 ON				
		0001: RF1 ON	1001: RF4,1 ON				
		0010: RF2 ON	1010: RF4,2 ON				
		0011: RF2,1 ON	1011: RF4,2,1 ON				
		0100: RF3 ON	1100: RF4,3 ON				
		0101: RF3,1 ON	1101: RF4,3,1 ON				
		0110: RF3,2 ON	1110: RF4,3,2 ON				
		0111: RF3,2,1 ON	1111: RF4,3,2,1 ON				

Register 0x0001 – ANT_CTRL1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/WM
7:0	SPARE	Reserved for future use	0x00	No	0 - 10	R/WM

Register 0x001A – RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x001B – GSID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x001C – PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	PWR_MODE[1]	0: Normal Operation 1: Low Power - Antenna in isolation	1	B/G	No	R/W
6	PWR_MODE[0]	0: ACTIVE 1: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	0b000	B/G	No	W

Register 0x001D – PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x3A	No	No	R

Register 0x001E – MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0xC6	No	No	R

Register 0x001F – MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	MFG_ID[11:8]	Upper four bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0x3	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID The default value at reset is selected by tying pin SID. SID / USID: GND 0x6; VIO 0x7; float 0x8 *Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.*	0x4	No	No	R/W

Register 0x0020 – EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

Register 0x0021 – REVISION_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.				

Register 0x0022 – GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x0023 – UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	W
6:0	RESERVED		0x00	No	No	R

Register 0x0024 – ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x002B – BUS_LD

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	SPARE	Reserved for future use	0x0	No	No	R/W

Register 0x002C – TEST_PATT

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TEST_PATT[7:0]	Test Pattern	0xD2	No	No	R

Register 0x002D – EXT_TRIG_MASK

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TriggerMask[10:3]	Setting bit TriggerMask[N] disables Trigger[N] If using an Extended Write to update both TriggerMask and Trigger, than TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0x00	No	No	R/W

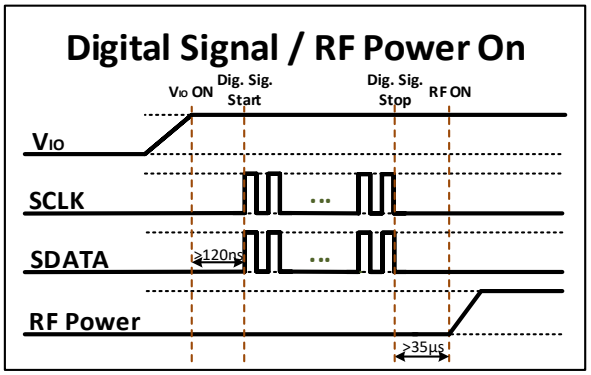
Register 0x002E – EXT_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	Trigger[10:3]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[10 - 3] will always read as 0.*	0x00	B/G	No	W

Power On and Off Sequence

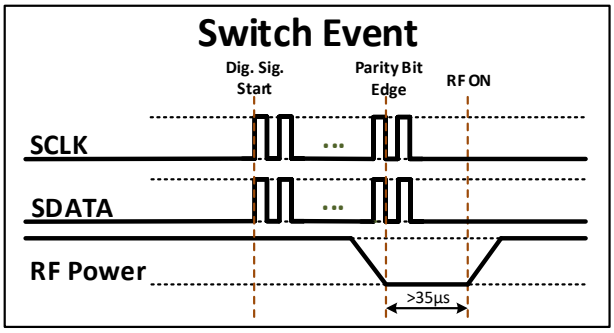
It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission.
2. Wait a minimum of 35 µs after RFFE bus is idle to apply an RF signal.



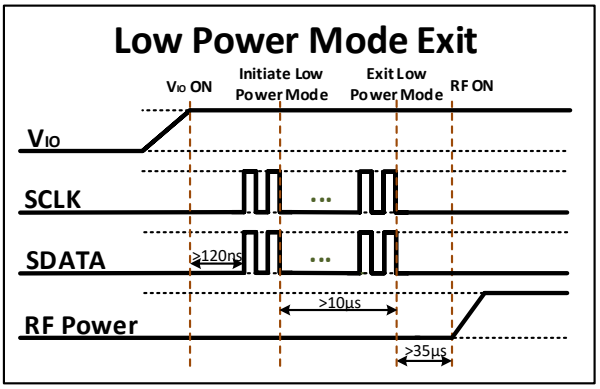
Digital Signal / RF Power-On Detail

3. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode.



Switch Event Timing

4. If “Low Power Mode” is utilized, there must be a delay of 35 µs before exiting “Low Power Mode”.



Low-Power Mode Exit Timing

PRELIMINARY

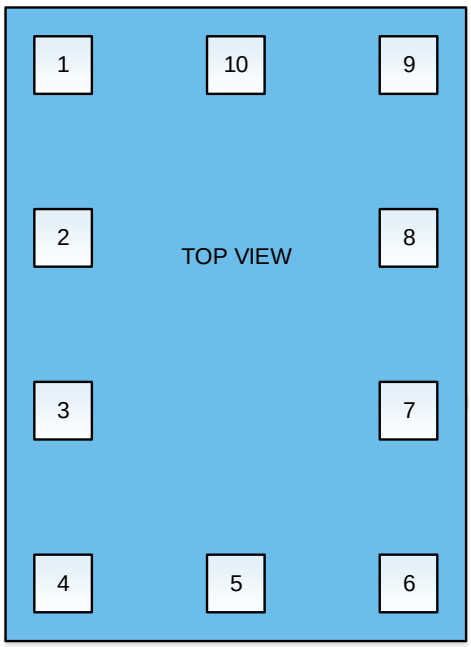
QM13344

4xSPST (Single-Pole-Single-Throw Switch)

Application Circuit Schematic

TBD

Pin Configuration



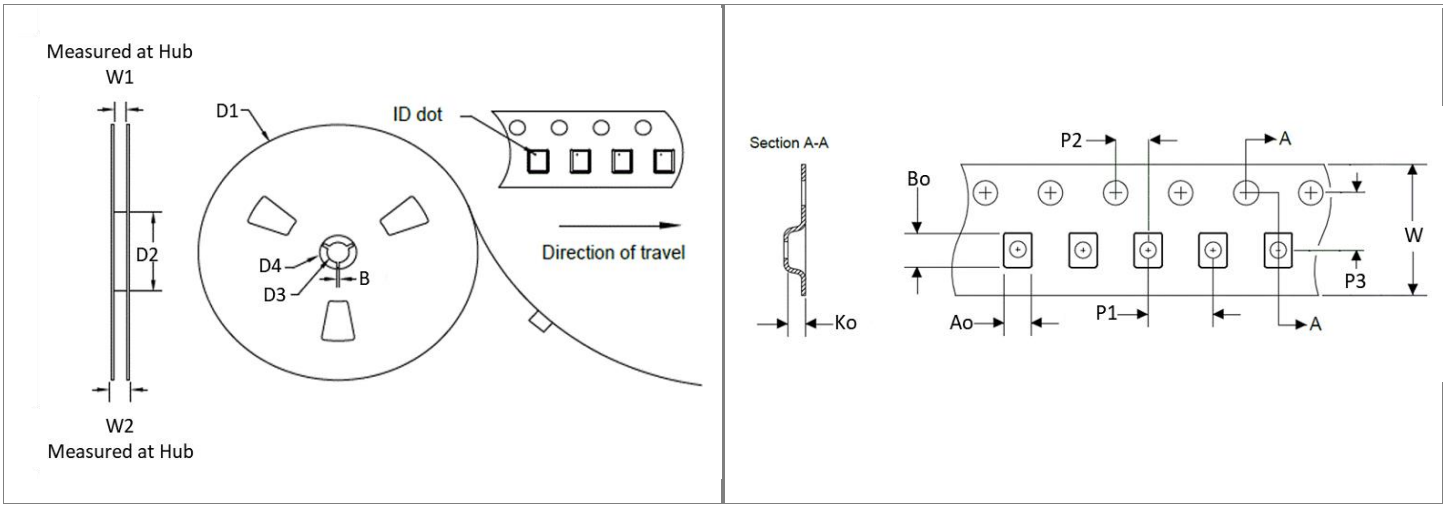
Pin Description

PIN	LABEL	DESCRIPTION
1	SDATA	RFFE DATA Line
2	SCLK	RFFE CLOCK Line
3	ID	USID Select
4	VIO	VIO Supply
5	GND	Ground
6	RF4	RF Port 4
7	RF3	RF Port 3
8	RF2	RF Port 2
9	RF1	RF Port 1
10	GND	Ground

QM13344

4xSPST (Single-Pole-Single-Throw Switch)

Tape and Reel Information



Feature	Measure	Symbol	Size (mm)	Feature	Measure	Symbol	Size (mm)
Flange	Diameter	D1	330.0	Cavity	Length	Ao	1.1
	Thickness	W2	14.2		Width	Bo	1.5
	Space Between Flange	W1	8.8		Depth	Ko	0.4
Hub	Outer Diameter	D2	102.0		Pitch	P1	4.0
	Arbor Hole Diameter	D3	13.0	Centerline Distance	Cavity to Perforation (Length)	P2	2.0
	Key Slit Width	B	2.0		Cavity to Perforation (Width)	P3	3.5
	Key Slit Diameter	D4	20.2	Carrier Tape	Width	W	8.0

(Unless otherwise specified, all dimension tolerances per EIA-481)

QM13344
4xSPST (Single-Pole-Single-Throw Switch)

Handling Precautions

Parameter	VALUE	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA/JEDEC JS-001

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

QM13344

4xSPST (Single-Pole-Single-Throw Switch)

REVISION HISTORY

REVISION	DESCRIPTION
REV A	Preliminary Data Sheet
REV B	Add RFFE MIPI Register Map and Tape and Reel Information

Contact Information