#### PI3WVR628

#### 2:1 MIPI 2-Data Lane Switch

#### **Features**

- → 3-lane, 2:1 switches that support D-PHY and C-PHY
- → Data rate support: up to 3.5Gsps C-PHY, up to 4.5Gb/s D-PHY.
- → Bandwidth: 6.0 GHz Typical
- → Low Crosstalk: -30 dB@2.25 GHz
- → Input Signals 0 to 1.3V
- → RON: 5.0Ω Typical LP & HS MIPI
- →  $\Delta$ R<sub>ON</sub>: 0.1Ω Typical LP & HS MIPI
- → R<sub>ON</sub>\_FLAT: 0.3Ω Typical LP & HS MIPI
- → I<sub>CCZ</sub>: 1µA Maximum
- → I<sub>CC</sub>: 15µA Typical
- → Skew of Opposite Transitions of the Same Output: 2ps Typical
- → V<sub>DD</sub> Operating Range: 1.5V to 3.6V
- → ESD Tolerance: 2kV HBM
- → Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- → Halogen and Antimony Free. "Green" Device (Note 3)
- → For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

#### **Description**

Diodes' PI3WVR628 is a two-data-lane MIPI switch. This 6 channel single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed (HS) or low-power (LP) MIPI signal. The PI3WVR628 is designed for the MIPI specification and allows connection to CSI/DSI, C-PHY/D-PHY module.

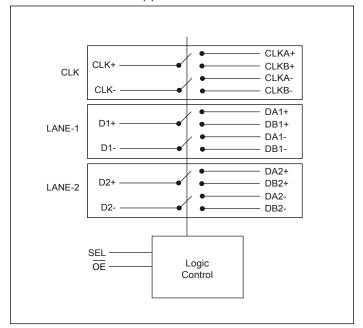
### **Applications**

- → Cellular Phones, Smart Phone
- **→** Tablets
- → Laptops
- → Displays

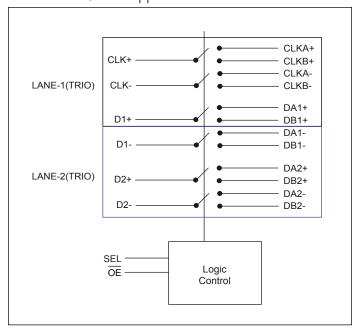
- 24-Pin, X1-LGA2417-24 (1.7mm x 2.4mm) (XB)

## **Block Diagram**

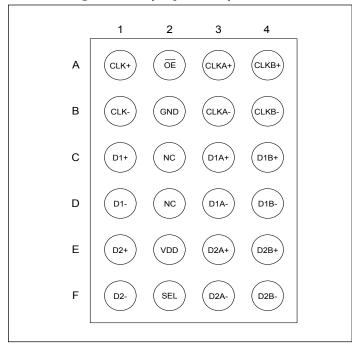
PI3WVR628 D-PHY Application



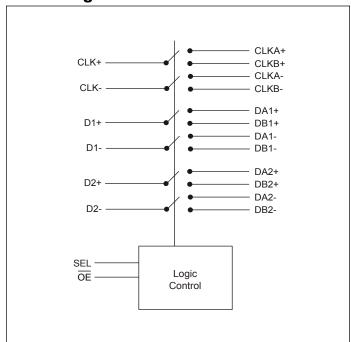
## PI3WVR628 C-PHY Application



## Pin Configuration(Top View)



## **Block Diagram**



## **Truth Table**

| SEL  | OE   Function |  |
|------|---------------|--|
| LOW  | LOW           | CLK+ = CLKA+, CLK- = CLKA-, Dn(+/-) = DAn(+/-) |
| HIGH | LOW           | CLK+ = CLKB+, CLK- = CLKB-, Dn(+/-) = DBn(+/-) |
| X    | HIGH          | Clock and Data Ports High Impedance            |

## PI3WVR628

## **Pin Description**

| Pin#   | Pin Name          | Signal Type | Description   |
|--------|-------------------|-------------|---|
| E2     | $V_{\mathrm{DD}}$ | Power       | 1.5V to 3.3V power supply   |
| B2     | GND               | Ground      | Ground  |
| A2     | ŌE                | I           | Output enable. if OE is low, IC is enabled. if OE is high, IC is power down and all I/Os are Hi-Z |
| F2     | SEL               | I           | Switch logic control  |
| C2, D2 | NC                | -           | Not Connect   |
| F4     | D2B-              | I/O         | Negative differential signal 2 for port B   |
| E4     | D2B+              | I/O         | Positive differential signal 2 for port B   |
| F3     | D2A-              | I/O         | Negative differential signal 2 for port A   |
| E3     | D2A+              | I/O         | Positive differential signal 2 for port A   |
| F1     | D2-               | I/O         | Negative differential signal 2 for COM port   |
| E1     | D2+               | I/O         | Positive differential signal 2 for COM port   |
| D4     | D1B-              | I/O         | Negative differential signal 1 for port B   |
| C4     | D1B+              | I/O         | Positive differential signal 1 for port B   |
| D3     | D1A-              | I/O         | Negative differential signal 1 for port A   |
| C3     | D1A+              | I/O         | Positive differential signal 1 for port A   |
| D1     | D1-               | I/O         | Negative differential signal 1 for COM port   |
| C1     | D1+               | I/O         | Positive differential signal 1 for COM port   |
| B4     | CLKB-             | I/O         | Clock negative differential signal for port B   |
| A4     | CLKB+             | I/O         | Clock positive differential signal for port B   |
| В3     | CLKA-             | I/O         | Clock negative differential signal for port A   |
| A3     | CLKA+             | I/O         | Clock positive differential signal for port A   |
| B1     | CLK-              | I/O         | Clock negative differential signal for COM port   |
| A1     | CLK+              | I/O         | Clock positive differential signal for COM port   |

#### PI3WVR628

### **Absolute Maximum Ratings**

(Above which useful life may be impaired. For user guidelines, not tested.)

| <u> </u>   |                         |
|--|-------------------------|
| V <sub>CC</sub> , Supply Voltage,                              | 0.5V to 4.6V            |
| V <sub>CNTRL</sub> , DC Input Voltage (OE, SEL) <sup>(1)</sup> | 0.5V to V <sub>CC</sub> |
| V <sub>SW</sub> , DC Switch I/O Voltage <sup>(1,2)</sup>       | 0.3V to 2.5V            |
| I <sub>IK</sub> , DC Input Diodes Current                      | 50mA                    |
| I <sub>OUT</sub> , DC Output Current                           | 25mA                    |
| T <sub>STG</sub> , Storage Temperature                         | 65°C to +150°C          |
| Tj, Junction Temperature                                       | 125°C                   |
| ESD:   |                         |
| Human Body Model, JEDEC: JESD22-A114, All F                    | Pins 2.0kV              |
| Charged Device Model, JEDEC: JESD22-C101                       | 1.0kV                   |
|  |                         |

#### Note:

Stresses greater than those listed under MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

#### Note:

- 1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
- 2. V<sub>SW</sub> refers to analog data switch paths.

### **Recommended Operating Conditions**

The Recommended operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

| Symbol   | Description  | <b>Test Conditions</b> | Min. | Max.            | Units |
|--|--|------------------------|------|-----------------|-------|
| V <sub>CC</sub>  | Supply Voltage   |                        | 1.5  | 3.6             | V     |
| V <sub>CNTRL</sub>   | Control Input Voltage (SEL, $\overline{OE}$ ) <sup>(1)</sup> |                        | 0    | V <sub>CC</sub> | V     |
| 17.  | Switch I/O Walters (CLV D. CLVA CLVD DA. DD.)                | HS Mode                | 0    | 0.5             | V     |
| V <sub>SW</sub> Switch I/O Voltage (CLK-, D-, CLKA-, CLKB-, DA-, DB- |  | LP Mode                | 0    | 1.3             | V     |
| T <sub>A</sub>   | Operating Temperature  |                        | -40  | +85             | °C    |

#### Note:

### **DC and Transient Characteristics**

All typical values are at  $T_A = 25$ °C unless otherwise specified.

|                                |   |   |             | $T_A = -40^{\circ} \text{C to } +85^{\circ} \text{C}$ |      | +85°C |       |
|--------------------------------|---|---|-------------|---|------|-------|-------|
| Symbol                         | Description   | <b>Test Conditions</b>                    | $V_{CC}(V)$ | Min.  | Тур. | Max.  | Units |
| V <sub>IK</sub>                | Clamp Diode Voltage (OE, SEL)                         | $I_{IN} = -18 \text{mA}$                  | 1.5         | -1.2  |      | -0.6  | V     |
| V <sub>IH</sub>                | Input Voltage High                                    | SEL, OE                                   | 1.5 to 3.3  | 1.0   |      |       | V     |
| V <sub>IL</sub>                | Input Voltage Low                                     | SEL, OE                                   | 1.5 to 3.3  |   |      | 0.5   | V     |
| I <sub>IN</sub>                | Control Input Leakage (OE, SEL)                       | V <sub>CNTRL</sub> = 0 to V <sub>CC</sub> | 3.3         | -0.5  |      | 0.5   | μΑ    |
| $I_{NO(OFF)}$<br>$I_{NC(OFF)}$ | Off Leakage Current of Port CLKA-, DA-, CLKB- and DB- | $V_{SW} = 0.0 \le DATA \le 1.3V$          | 3.3         | -0.5  |      | 0.5   | μΑ    |
| I <sub>A(ON)</sub>             | On Leakage Current of Common<br>Ports (CLK-, D-)      | $V_{SW} = 0.0 \le DATA \le 1.3V$          | 3.3         | -0.5  |      | 0.5   | μА    |

<sup>1.</sup> The control inputs must be held HIGH or LOW; they must not float.

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## DC and Transient Characteristics Cont.

|                           | Description   |  |                     | $T_A = -40^{\circ} \text{C to } +85^{\circ} \text{C}$ |      |      |       |
|---------------------------|---|--|---------------------|---|------|------|-------|
| Symbol                    |   | <b>Test Conditions</b>   | V <sub>CC</sub> (V) | Min.  | Тур. | Max. | Units |
| I <sub>OFF</sub>          | Power-Off Leakage Current (All I/O Ports)   | $V_{SW} = 0.0 \text{ or } 1.3 \text{V}$  | 0                   | -0.5  |      | 0.5  | μА    |
| $I_{OZ}$                  | Off-State Leakage   | $\frac{V_{SW} = 0.0 \le DATA \le 1.3V,}{OE = High}$  | 3.3                 | -0.5  |      | 0.5  | μА    |
|                           |   | $I_{ON} = -8 \text{mA}, \overline{OE} = 0 \text{V},$   | 1.5                 |   |      |      |       |
| R <sub>ON_MIPI_HS</sub>   | Switch On Resistance for HS MIPI  | $SEL = V_{CC} \text{ or } 0V, CLKA,$   | 2.5                 |   | 5    |      | Ω     |
|                           |   | CLKB, DB- or DA- = $0.2V$  | 3.3                 |   |      |      |       |
|                           |   | $I_{ON} = -8mA$ , $\overline{OE} = 0V$ ,   | 1.5                 |   |      |      |       |
| R <sub>ON_MIPI_LP</sub>   | Switch On Resistance for LP MIPI  | SEL = $V_{CC}$ or $0V$ , CLKA,   | 2.5                 |   | 5    |      | Ω     |
|                           |   | CLKB, DB- or DA- = 1.2V  | 3.3                 |   |      |      |       |
|                           | On Resistance Matching Between<br>HS MIPI Channels <sup>(1)</sup>   | $I_{ON} = -8mA$ , $\overline{OE} = 0V$ ,<br>$SEL = V_{CC}$ or $0V$ , $CLKA$ ,<br>CLKB, $DB$ - or $DA$ - $= 0.2V$ | 1.5                 |   |      |      | _     |
| $\Delta R_{ON\_MIPI\_HS}$ |   |  | 2.5                 |   | 0.1  |      | Ω     |
|                           |   |  | 3.3                 |   |      |      |       |
| A.D.                      | On Resistance Matching Between  | $I_{ON} = -8mA$ , $\overline{OE} = 0V$ ,<br>$SEL = V_{CC}$ or $0V$ , $CLKA$ ,<br>CLKB, $DB$ - or $DA$ - = 1.2V   | 1.5                 |   | 0.1  |      |       |
| ΔR <sub>ON_MIPI_LP</sub>  | LP MIPI Channels <sup>(1)</sup>   |  | 3.3                 |   | 0.1  |      | Ω     |
|                           |   | $I_{ON} = -8 \text{mA}, \overline{OE} = 0 \text{V},$   | 1.5                 |   |      |      |       |
| R <sub>ON_FLAT_</sub>     | On Resistance Flatness for HS MIPI  | SEL = V <sub>CC</sub> or 0V, CLKA,<br>CLKB, DB- or DA- = 0 to<br>0.5V  | 2.5                 |   | 0.3  |      |       |
| MIPI_HS                   | On Resistance Flatness for HS WIFF  |  | 3.3                 |   | 0.3  |      | Ω     |
|                           |   | $I_{ON} = -8mA, \overline{OE} = 0V,$   | 1.5                 |   |      |      |       |
| R <sub>ON_FLAT_</sub>     | On Resistance Flatness for LP MIPI  | $SEL = V_{CC}$ or $0V$ , $CLKA$ ,  | 2.5                 |   | 0.3  |      | Ω     |
| MIPI_LP                   | On Resistance Flatness for LP MIPI  | CLKB, DB- or DA- = 0 to 1.3V   | 3.3                 |   | 0.5  |      | 32    |
| $I_{CC}$                  | Quiescent Supply Current  | $\frac{V_{SEL} = 0 \text{ or } V_{CC}, I_{OUT} = 0,}{OE = 0V}$   | 3.6                 |   | 11   | 20   | μΑ    |
| I <sub>CCZ</sub>          | Quiescent Supply Current (High<br>Impedance)  | $\frac{V_{SEL} = 0 \text{ or } V_{CC}, I_{OUT} = 0,}{OE = 0V}$   | 3.6                 |   |      | 1    | μА    |
| I <sub>CCT</sub>          | $\begin{array}{c} \text{Increase in $I_{CC}$ Current Per Control} \\ \text{Voltage and $V_{CC}$} \end{array}$ | $V_{SEL} = 0$ or $V_{CC}$ , $\overline{OE} = 1.5V$   | 3.6                 |   | 1    |      | μА    |

**PI3WVR628** 

## **AC Electrical Characteristics**

All typical values are for  $V_{CC}=3.3 V$  and  $T_A=25 ^{\circ} C$  unless otherwise specified.

|                   |  |  |             | T <sub>A</sub> = | 40°C to | +85°C |       |  |
|-------------------|--|--|-------------|------------------|---------|-------|-------|--|
| Symbol            | Description  | <b>Test Conditions</b>   | $V_{CC}(V)$ | Min.             | Тур.    | Max.  | Units |  |
| t <sub>INIT</sub> | Initialization Time $V_{CC}$ to $Output^{(1)}$     | $R_{L} = 50\Omega, C_{L} = 0 pF, V_{SW}$<br>= 0.6V                               | 1.5 to 3.6  |                  | 60      |       | μs    |  |
| t <sub>EN</sub>   | Enable Time OE to Output                           | $R_L = 50\Omega, C_L = 0pF, V_{SW}$<br>= 0.6V                                    | 1.5 to 3.6  |                  | 60      | 150   | μs    |  |
| $t_{ m DIS}$      | Disable Time OE to Output                          | $R_L = 50\Omega, C_L = 0pF, V_{SW}$<br>= 0.6V                                    | 1.5 to 3.6  |                  | 35      | 250   | ns    |  |
| t <sub>ON</sub>   | Turn-On Time SEL to Output                         | $R_L = 50\Omega, C_L = 0pF, V_{SW}$ $= 0.6V$                                     | 1.5 to 3.6  |                  | 350     | 1100  | ns    |  |
| t <sub>OFF</sub>  | Turn-Off Time SEL to Output                        | $R_L = 50\Omega, C_L = 0pF, V_{SW}$ $= 0.6V$                                     | 1.5 to 3.6  |                  | 125     | 800   | ns    |  |
| t <sub>BBM</sub>  | Break-Before-Make Time                             | $R_L = 50\Omega, C_L = 0pF, V_{SW}$ $= 0.6V$                                     | 1.5 to 3.6  |                  |         | 450   | ns    |  |
| t <sub>PD</sub>   | Propagation Delay <sup>(1)</sup>                   | $C_L = 0$ pF, $R_L = 50$ $\Omega$  | 1.5 to 3.6  |                  |         | 0.25  | ns    |  |
| O <sub>IRR</sub>  | Differential Off Isolation for MIPI <sup>(1)</sup> | $\frac{R_L}{OE} = 50\Omega, f = 1250MHz,$ $\frac{R_L}{OE} = HIGH, V_{SW} = 0.5V$ | 1.5 to 3.6  |                  | -26     |       | dB    |  |
| V                 | Differential Crosstalk for MIPI(1)                 | $R_L = 50\Omega$ , $f = 1250MHz$ ,<br>$SEL = HIGH$ , $V_{SW} = 0.5V$             | 1.5 to 3.6  |                  |         | -35   | lp.   |  |
| $X_{TALK}$        | Differential Crosstalk for MIPT                    | $R_L = 50\Omega, f = 2250 MHz, \\ SEL = LOW, V_{SW} = 0.5V$                      | 1.5 10 5.6  |                  |         | -30   | dB    |  |
|                   |  | $R_L = 50\Omega, C_L = 0pF,$<br>$f = 2250MHz, V_{SW} = 0.5V$                     | 1.5 to 3.6  |                  | -1.1    |       | 1D    |  |
| $I_{LOSS}$        | Differential Insertion Loss <sup>(1)</sup>         | $R_L = 50\Omega, C_L = 0pF,$<br>$f = 1250MHz, V_{SW} = 0.5V$                     | 1.5 to 3.6  |                  | -0.8    |       | dB    |  |
| BW                | Differential -3db Bandwidth <sup>(1)</sup>         | $R_L = 50\Omega, C_L = 0pF, V_{SW}$<br>= 0.5V                                    | 1.5 to 3.6  | 5                | 6       |       | GHz   |  |

#### Note:

 $<sup>1. \</sup> Guaranteed \ by \ characterization.$ 

**PI3WVR628** 

# **High-Speed-Related AC Electrical Characteristics**

|                    |  |  |             | $T_A = -4$ | 40°C to | +85°C |       |
|--------------------|--|--|-------------|------------|---------|-------|-------|
| Symbol             | Description  | <b>Test Conditions</b>                         | $V_{CC}(V)$ | Min.       | Тур.    | Max.  | Units |
|                    | D-PHY HS Mode Skew of Opposite Transitions of the Same Output <sup>(1)</sup> | $R_L = 50\Omega, C_L = 0$ pF, $V_{SW} = 0.3$ V | 1.5 to 3.6  |            | 4       |       |       |
| t <sub>SK(P)</sub> | C-PHY HS Mode Skew of 3 channels in same lane                                | $R_L = 50\Omega, C_L = 0pF, V_{SW} = 0.5V$     | 1.5 to 3.6  |            | 4       |       | ps    |
|                    | D-PHY HS Mode Skew of all group A or group B channels <sup>(1)</sup>         | $R_L = 50\Omega, C_L = 0pF, V_{SW} = 0.3V$     | 1.5 to 3.6  |            | 8       |       |       |

Note:

## **Capacitance**

|                  |                                  |   | $T_A = -4$ | 40°C to | +85°C |       |
|------------------|----------------------------------|---|------------|---------|-------|-------|
| Symbol           | Description                      | <b>Test Conditions</b>  | Min.       | Тур.    | Max.  | Units |
| C <sub>IN</sub>  | Control Pin Input Capacitance(1) | $V_{CC} = 0V, f = 1MHz$   |            | 2.1     |       | pF    |
| C <sub>ON</sub>  | On Capacitance <sup>(1)</sup>    | $V_{CC} = 3.3V$ , $\overline{OE} = 0V$ , $f = 1250MHz$ (In HS common value)     |            | 1.3     |       | pF    |
| C <sub>OFF</sub> | Off Capacitance <sup>(1)</sup>   | $V_{CC}$ or $\overline{OE}$ = 3.3V, f = 1250MHz (Both sides in HS common value) |            | 0.8     |       | pF    |

Note:

 $<sup>1. \</sup> Guaranteed \ by \ characterization.$ 

 $<sup>1. \</sup> Guaranteed \ by \ characterization.$ 

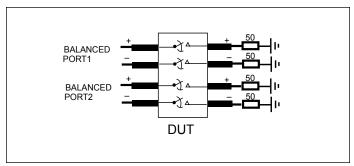


Fig 1. Crosstalk Setup

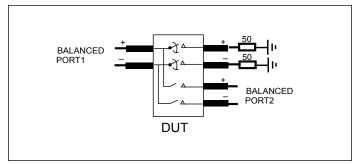


Fig 2. Off-Isolation Setup

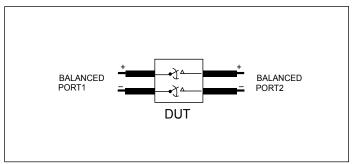
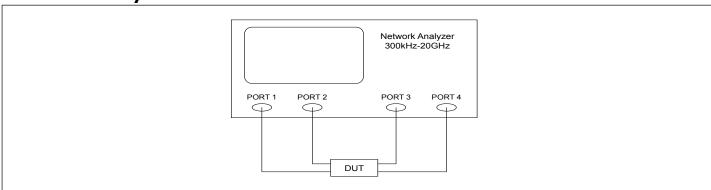
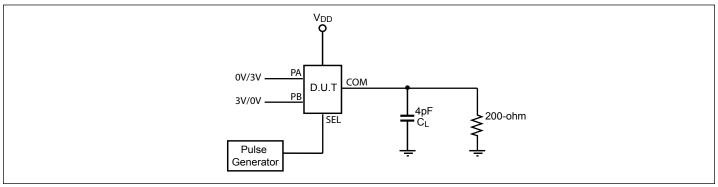


Fig 3. Differential Insertion Loss

## **Test Circuit for Dynamic Electrical Characteristics**



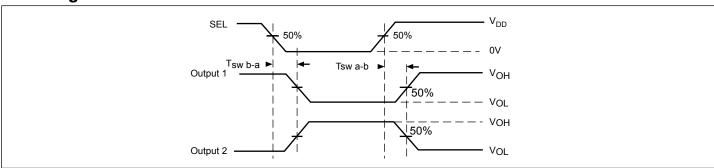
#### Test Circuit for Electrical Characteristics(1-4)



#### Notes:

- 1.  $C_L$  = Load capacitance: includes jig and probe capacitance.
- 2.  $R_T$  = Termination resistance: should be equal to  $Z_{OUT}$  of the Pulse Generator
- 3. All input impulses are supplied by generators having the following characteristics:  $PRR \leq MHz, Z_O = 50\Omega, t_R \leq 2.5ns, t_F \leq 2.5ns$
- 4. The outputs are measured one at a time with one transition per measurement.

## **Switching Waveforms**



**Voltage Waveforms for Select Timing** 

#### **Test Condition**

| Output 1 Test Condition | Output 2 Test Condition |
|-------------------------|-------------------------|
| PA = Low                | PA = High               |
| PB = High               | PB = Low                |

### **Part Marking**

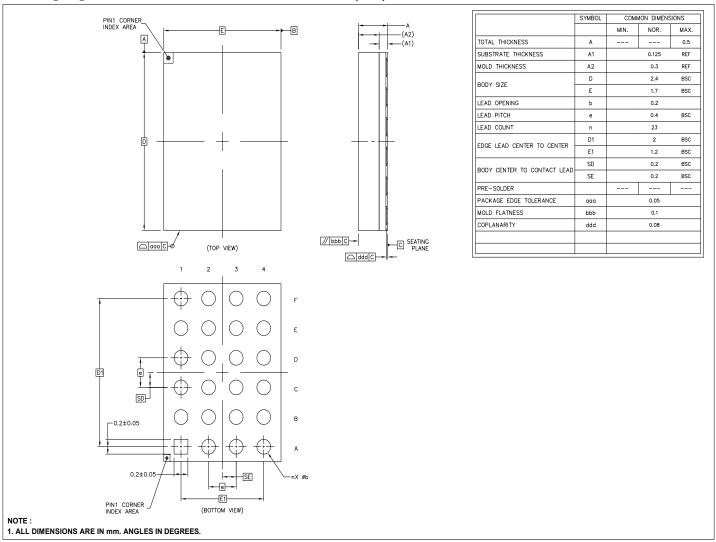


Y: Shortened Date Code (Year)

W: Shortened Date Code (Workweek)

1st X: Assembly Code 2nd X: Fab Code

## Packaging Mechanical: 24-X1-LGA2417-24 (XB)



#### For latest package info.

 $please\ check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-mechanicals-and-thermal-characteristics/pericom-packaging-pericom-$ 

## **Ordering Information**

| Ordering Code | Package Code | Package Description       |
|---------------|--------------|---------------------------|
| PI3WVR628XBEX | XB           | 24-contact, X1-LGA2417-24 |

#### Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. E = Pb-free and Green
- 5. X suffix = Tape/Reel

#### PI3WVR628

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#### LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

- A. Life support devices or systems are devices or systems which:
  - 1. are intended to implant into the body, or
- 2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.
- B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the