SGM8252A
2.8MHz, High Voltage, High Precision, Low Noise Rail-to-Rail Output Operational Amplifier

GENERAL DESCRIPTION

The dual SGM8252A is a rail-to-rail output, low noise and high precision operational amplifier which has low input offset voltage and bias current. It is guaranteed to operate from 4.5V to 36V single supply.

The rail-to-rail output swing provided by the SGM8252A makes both high-side and low-side sensing easy. The combination of these characteristics makes the SGM8252A good choice for temperature, position and pressure sensors, medical equipment and strain gauge amplifiers, or any other 4.5V to 36V application requiring precision and long term stability.

The dual SGM8252A is available in Green SOIC-8 and MSOP-8 packages. It is rated over the -40℃ to +125℃ temperature range.

FEATURES

- **Low Offset Voltage: 5μV (TYP)**
- **Rail-to-Rail Output Swing**
- **4.5V to 36V Single Supply Operation**
- **Open-Loop Voltage Gain: 150dB (TYP)**
- **PSRR: 150dB (TYP)**
- **CMRR: 135dB (TYP)**
- **0.1Hz to 10Hz Noise: 0.4μV_{P-P}**
- **Input Voltage Noise Density: 20nV/$\sqrt{Hz}$ at 1kHz**
- **Gain-Bandwidth Product: 2.8MHz**
- **Overload Recovery Time: 3μs**
- **Low Supply Current: 460μA/Amplifier (TYP)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-8 and MSOP-8 Packages**

APPLICATIONS

Temperature Measurements
Pressure Sensors
Precision Current Sensing
Electronic Scales
Strain Gauge Amplifiers
Medical Instrumentation
Thermocouple Amplifiers
Handheld Test Equipment

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8252A	SOIC-8	-40℃ to +125℃	SGM8252AXS8G/TR	SGM 8252AXS8 XXXXX	Tape and Reel, 4000
	MSOP-8	-40℃ to +125℃	SGM8252AXMS8G/TR	SGM8252A XMS8 XXXXX	Tape and Reel, 4000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

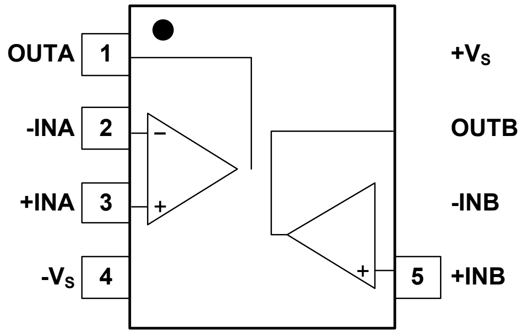
Supply Voltage....................40V
Input Voltage Range .... $(-V_S) - 0.3V$ to $(+V_S) + 0.3V$
Differential Input Voltage Range .... -15V to +15V
Junction Temperature ....+150℃
Storage Temperature Range ....-65℃ to +150℃
Lead Temperature (Soldering, 10s) ....+260℃
ESD Susceptibility
HBM....................6000V
MM....................300V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ....4.5V to 36V
Operating Temperature Range ....-40℃ to +125℃

PIN CONFIGURATIONS

SGM8252A (TOP VIEW)



SOIC-8/MSOP-8

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

ELECTRICAL CHARACTERISTICS

(At T_A = +25℃, V_S = ±2.5V to V_S = ±18V, V_{CM} = 0V and R_L = 10kΩ connected to 0V, Full = -40℃ to +125℃, unless otherwise noted.)

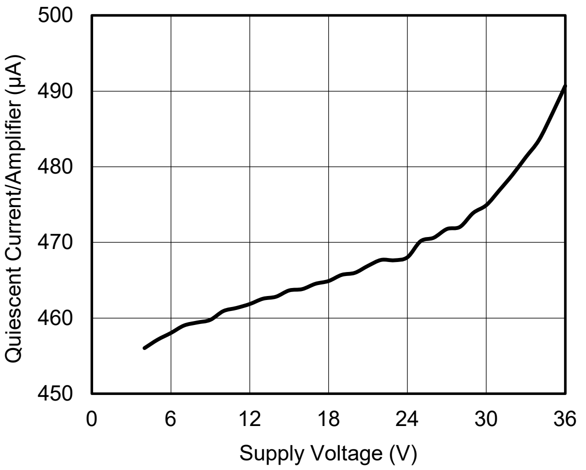
PARAMETER	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (V_{OS})		+25℃		5		μV
Input Offset Voltage Drift ($\Delta V_{OS}/\Delta T$)		Full		20		nV/℃
Input Bias Current (I_B)		+25℃		±100		pA
Input Offset Current (I_{OS})		+25℃		±200		pA
Input Common Mode Voltage Range (V_{CM})		Full	($-V_S$) - 0.05		($+V_S$) -1.5	V
Common Mode Rejection Ratio [1] (CMRR)	V_{CM} = ($-V_S$) - 0.05V to ($+V_S$) - 1.5V	+25℃		135		dB
Open-Loop Voltage Gain (A_{OL})	V_S = ±2.5V, V_{OUT} = ±2.0V	+25℃		140		dB
	V_S = ±18V, V_{OUT} = ±17.5V	+25℃		150		
OUTPUT CHARACTERISTICS						
Output Voltage Swing from Rail	V_S = ±2.5V	+25℃		13		mV
	V_S = ±18V	+25℃		95		
Output Short-Circuit Current (I_{SC})	V_S = ±2.5V	+25℃		±32		mA
	V_S = ±18V	+25℃		±48		
POWER SUPPLY						
Operating Voltage Range (V_S)		Full	4.5		36	V
Quiescent Current/Amplifier (I_Q)	I_{OUT} = 0	+25℃		460		μA
Power Supply Rejection Ratio [1] (PSRR)	V_S = 4.5V to 36V	+25℃		150		dB
DYNAMIC PERFORMANCE						
Gain-Bandwidth Product (GBP)	V_{OUT} = 100mV_{P-P}, C_L = 10pF	+25℃		2.8		MHz
Slew Rate (SR)		+25℃		1.2		V/μs
Settling Time to 0.1% (t_S)	V_{IN} = 1V Step, A_V = +1	+25℃		0.8		μs
Overload Recovery Time	$V_{IN} \times A_V > V_S$	+25℃		3		μs
Total Harmonic Distortion + Noise (THD+N)	V_{IN} = 2V_{P-P}, A_V = +1, f = 1kHz	+25℃		0.0005		%
NOISE						
Input Voltage Noise	f = 0.1Hz to 10Hz	+25℃		0.4		μV_{P-P}
Input Voltage Noise Density (e_n)	f = 0.1kHz	+25℃		20		nV/√Hz
	f = 1kHz	+25℃		20		
	f = 10kHz	+25℃		23		

NOTE: 1. PSRR and CMRR are affected by the matching between external gain-setting resistor ratios.

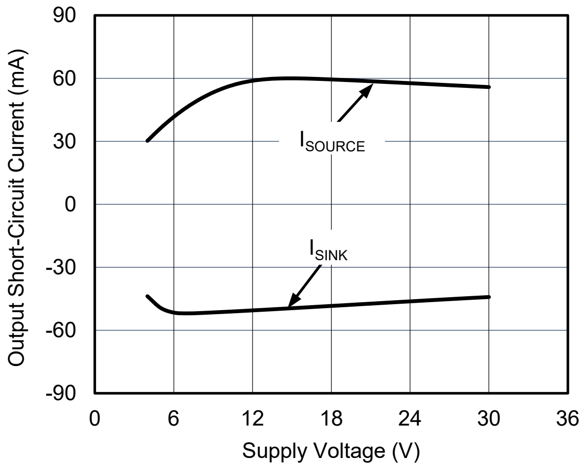
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = ±15V, C_L = 10pF and R_L = 10kΩ, unless otherwise noted.

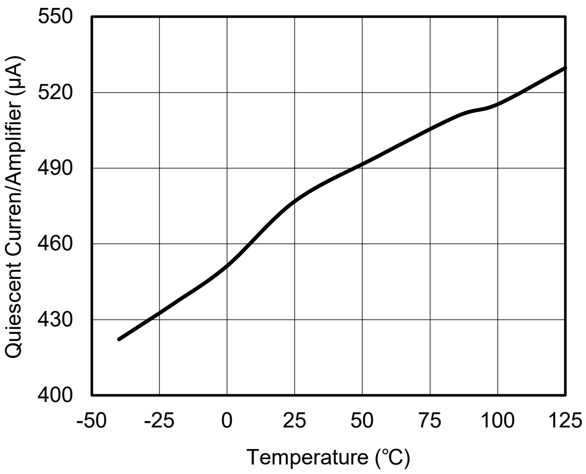
Quiescent Current vs. Supply Voltage



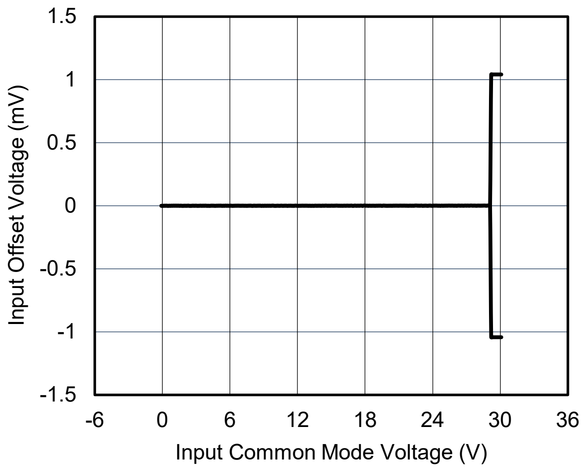
Output Short-Circuit Current vs. Supply Voltage



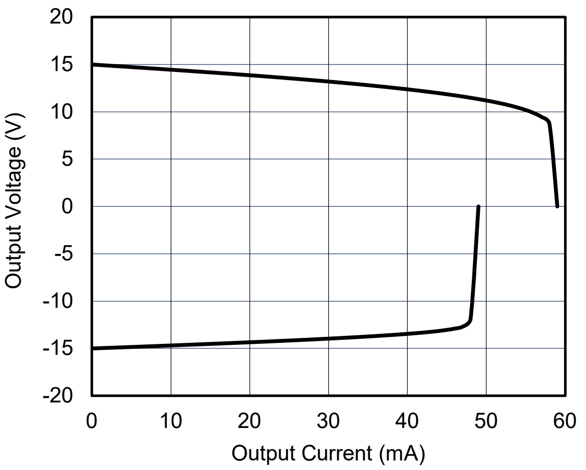
Quiescent Current vs. Temperature



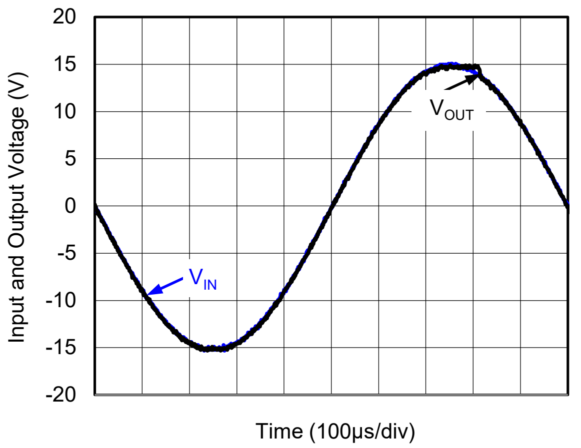
Input Offset Voltage vs. Input Common Mode Voltage



Output Voltage vs. Output Current



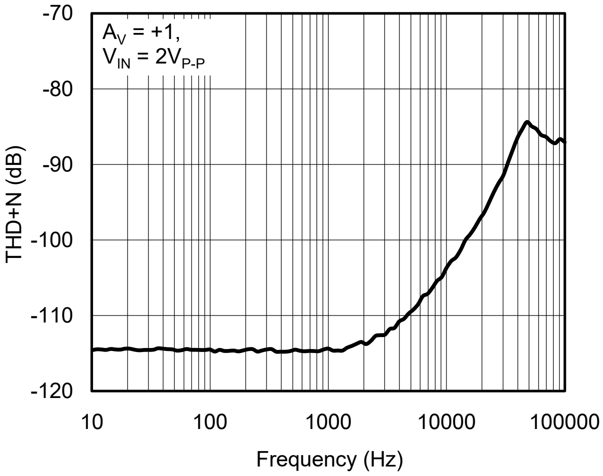
No Phase Reversal



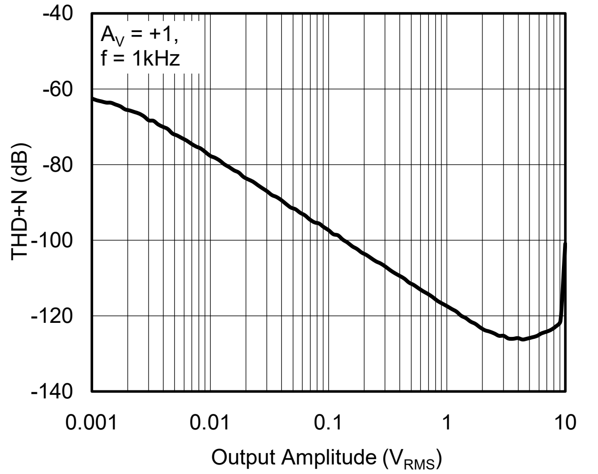
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V, C_L = 10pF and R_L = 10kΩ, unless otherwise noted.

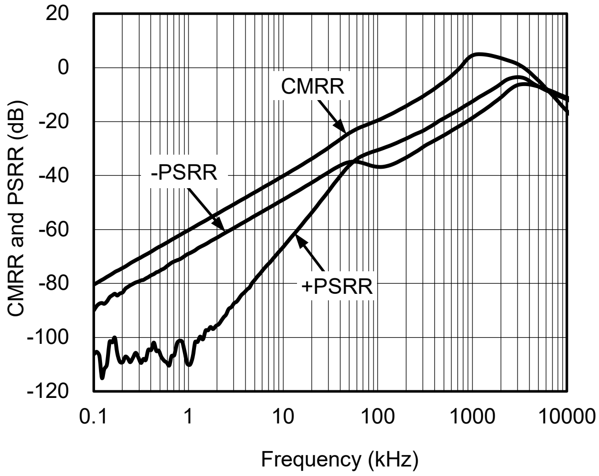
THD+N vs. Frequency



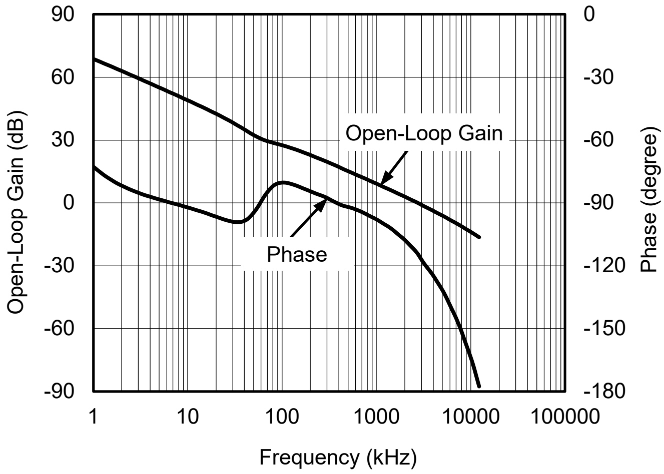
THD+N vs. Output Amplitude



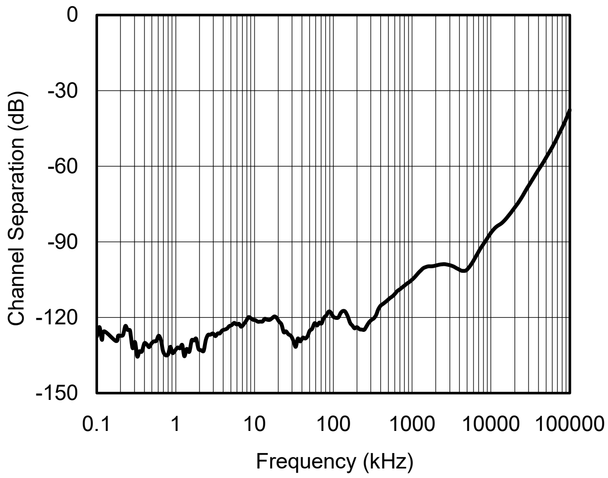
CMRR and PSRR vs. Frequency



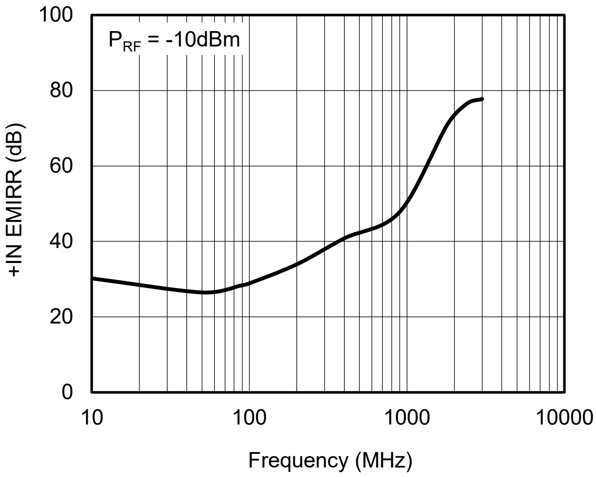
Open-Loop Gain and Phase vs. Frequency



Channel Separation vs. Frequency



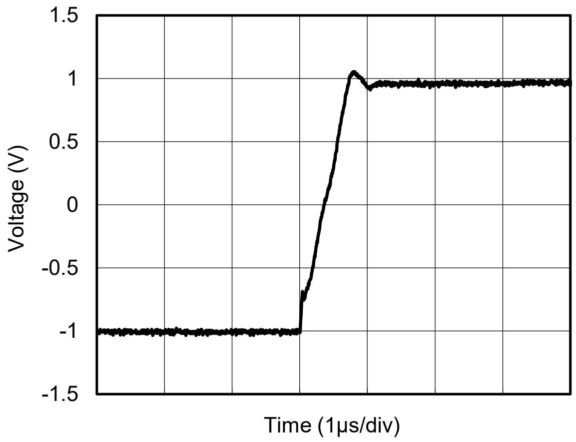
+IN EMIRR vs. Frequency



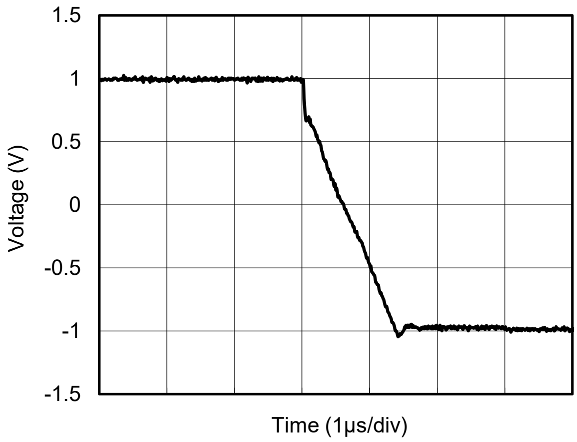
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V, C_L = 10pF and R_L = 10kΩ, unless otherwise noted.

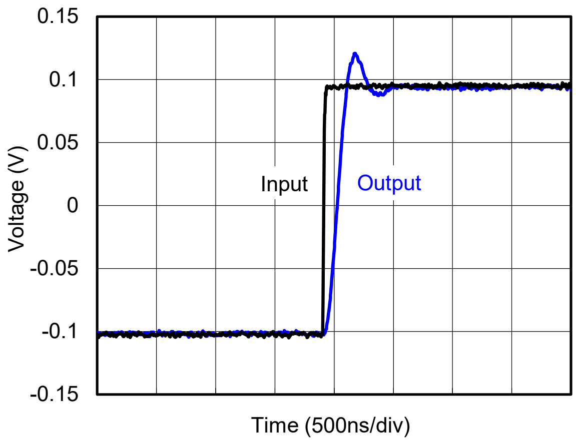
Slew Rate (up)



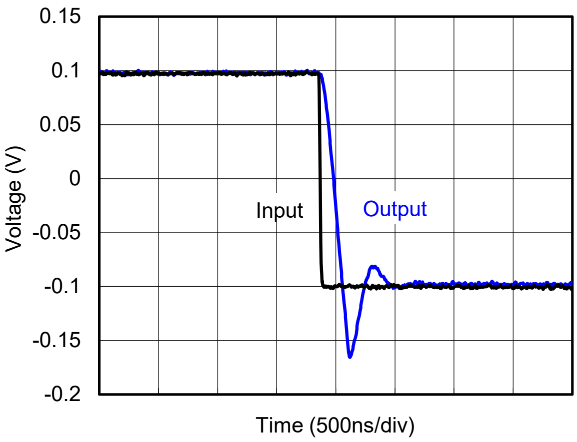
Slew Rate (down)



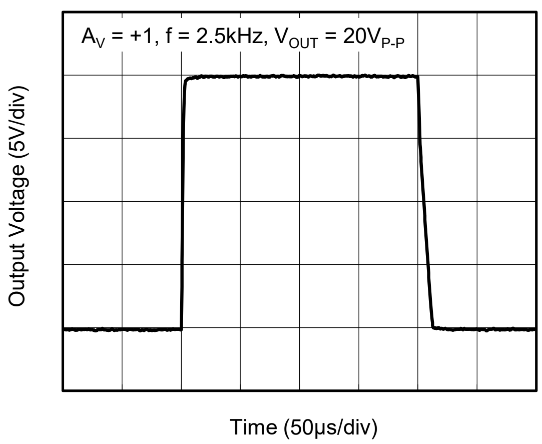
Positive Settling Time



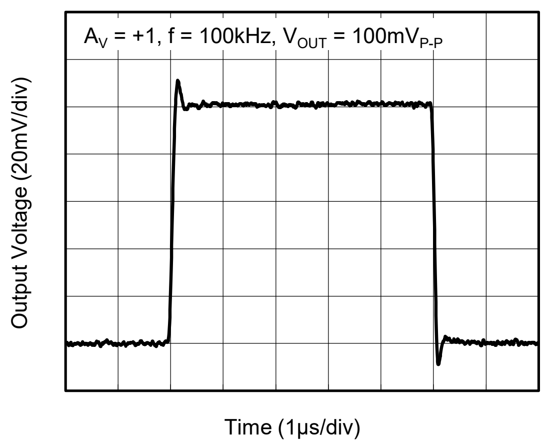
Negative Settling Time



Large-Signal Step Response



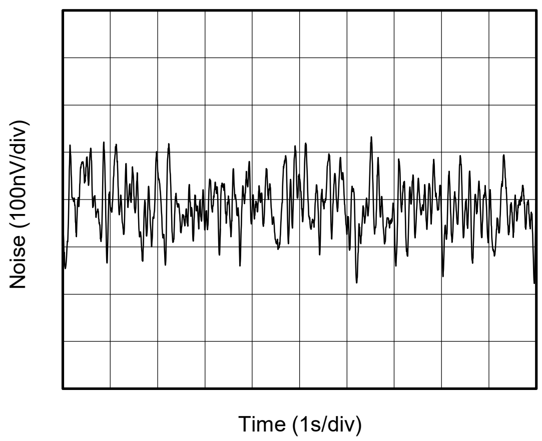
Small-Signal Step Response



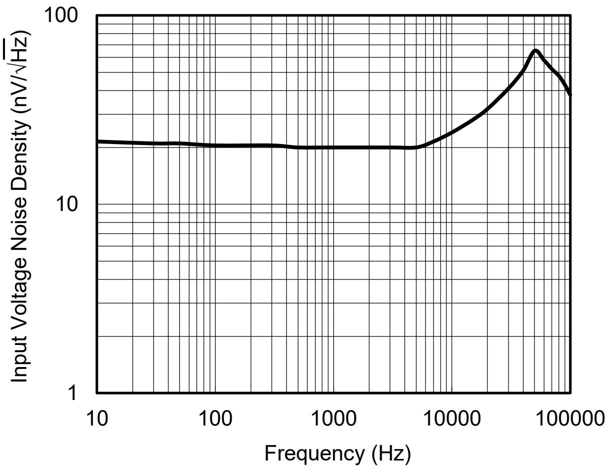
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V, C_L = 10pF and R_L = 10kΩ, unless otherwise noted.

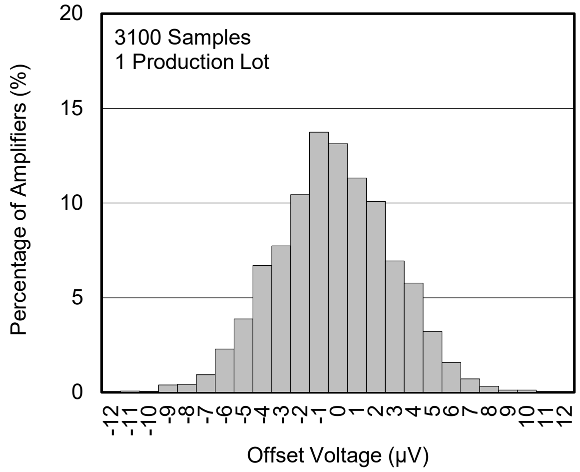
0.1Hz to 10Hz Input Voltage Noise



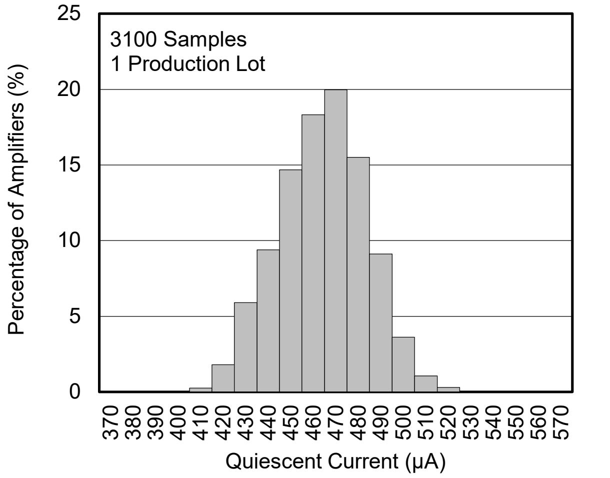
Input Voltage Noise Density vs. Frequency



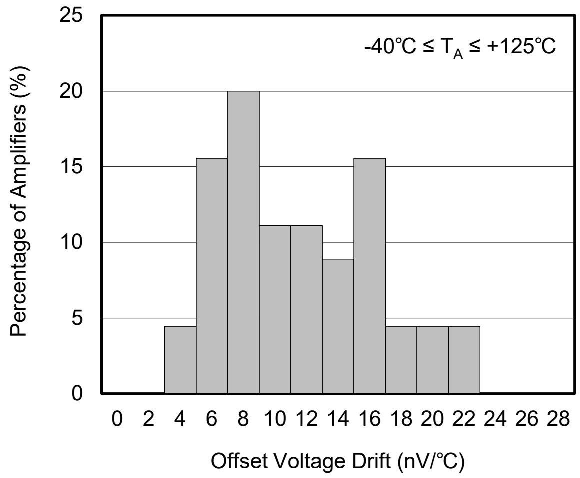
Offset Voltage Production Distribution



Quiescent Current Production Distribution



Offset Voltage Drift Distribution



APPLICATION NOTES

Driving Capacitive Loads

The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation. Applications that require greater capacitive driving capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 1. The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD}.

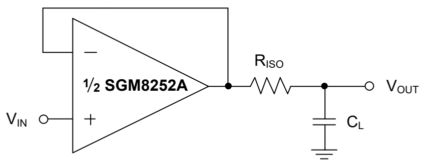


Figure 1. Indirectly Driving Heavy Capacitive Load

An improved circuit is shown in Figure 2. It provides DC accuracy as well as AC stability. R_F provides the DC accuracy by connecting the inverting input with the output. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

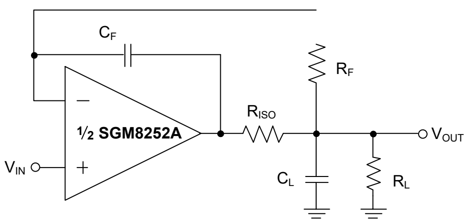


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

For non-buffer configuration, there are two other ways to increase the phase margin: (a) by increasing the amplifier's closed-loop gain or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

Power-Supply Bypassing and Layout

The SGM8252A operates from either a single 4.5V to 36V supply or dual ±2.25V to ±18V supplies. For single-supply operation, bypass the power supply $+V_S$ with a 0.1μF ceramic capacitor which should be placed close to the $+V_S$ pin. For dual-supply operation, both the $+V_S$ and the $-V_S$ supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. 2.2μF tantalum capacitor can be added for better performance.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible.

For the operational amplifier, soldering the part to the board directly is strongly recommended. Try to keep the high frequency current loop area small to minimize the EMI (electromagnetic interference).

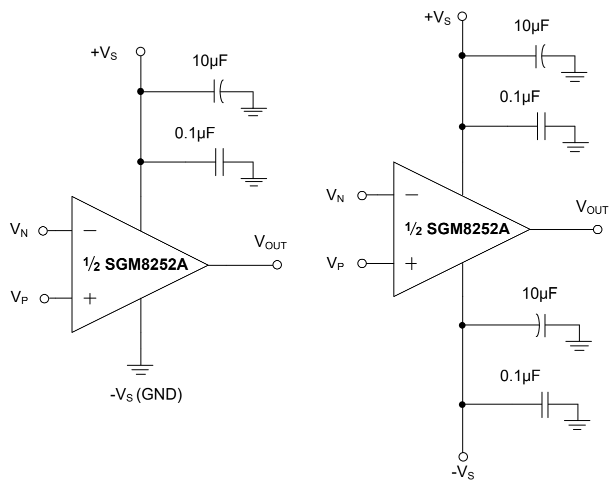


Figure 3. Amplifier with Bypass Capacitors

Grounding

A ground plane layer is important for SGM8252A circuit design. The length of the current path in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be in parallel. This helps reduce unwanted positive feedback.

TYPICAL APPLICATION CIRCUITS

Differential Amplifier

The circuit shown in Figure 4 performs the difference function. If the resistor ratios are equal ($R_4/R_3 = R_2/R_1$), then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

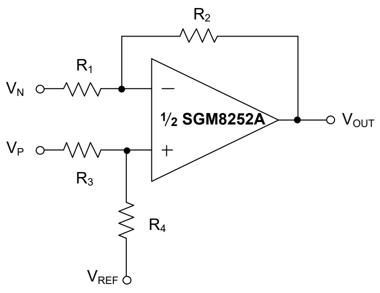


Figure 4. Differential Amplifier

Instrumentation Amplifier

The circuit in Figure 5 performs the same function as that in Figure 4 but with a high input impedance.

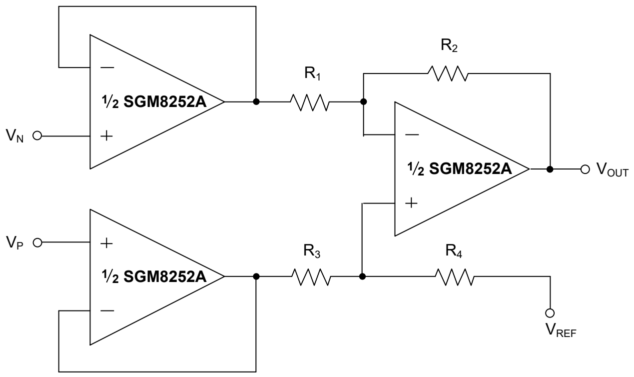


Figure 5. Instrumentation Amplifier

Active Low-Pass Filter

The low-pass filter shown in Figure 6 has a DC gain of ($-R_2/R_1$) and the -3dB corner frequency is $1/2\pi R_2C$. Make sure the filter bandwidth is within the bandwidth of the amplifier. Feedback resistors with large values can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistor values as low as possible and consistent with output loading consideration.

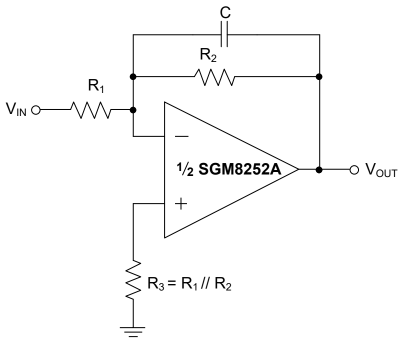
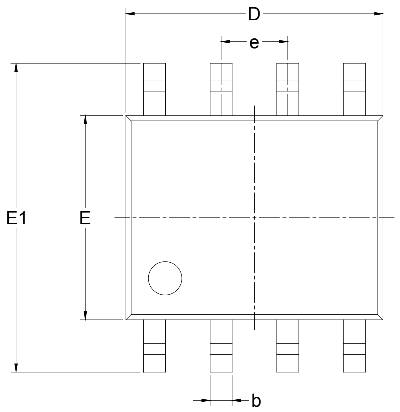
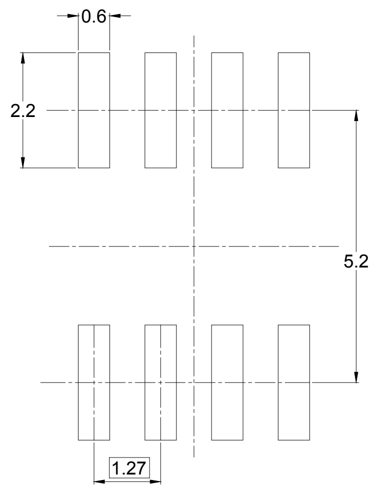


Figure 6. Active Low-Pass Filter

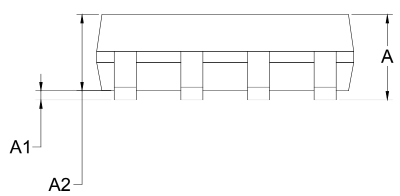
PACKAGE OUTLINE DIMENSIONS

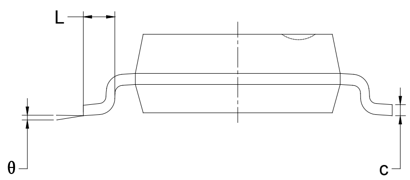
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

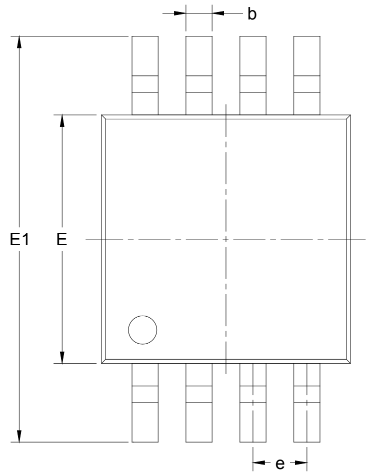


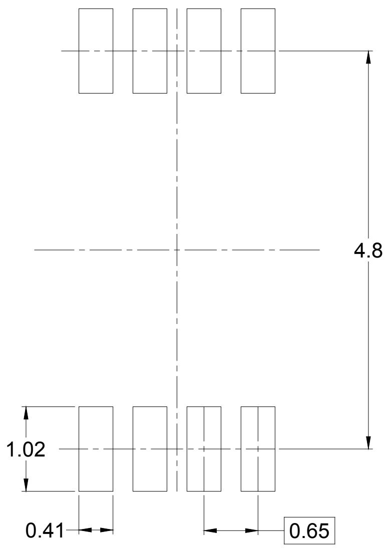


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	**MAX**	**MIN**	**MAX**
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

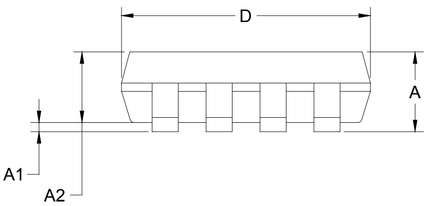
PACKAGE OUTLINE DIMENSIONS

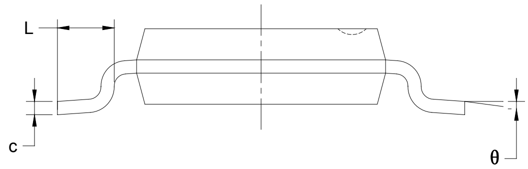
MSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)

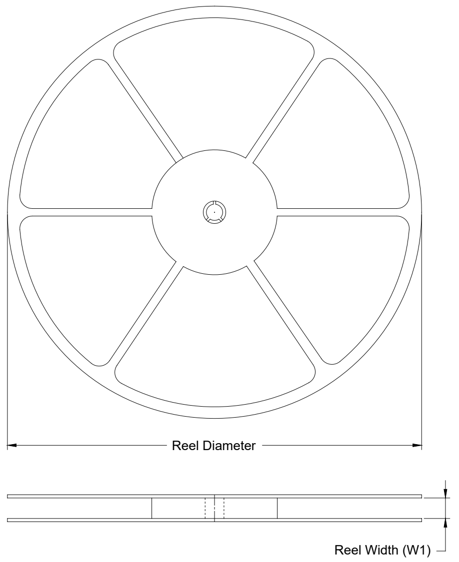




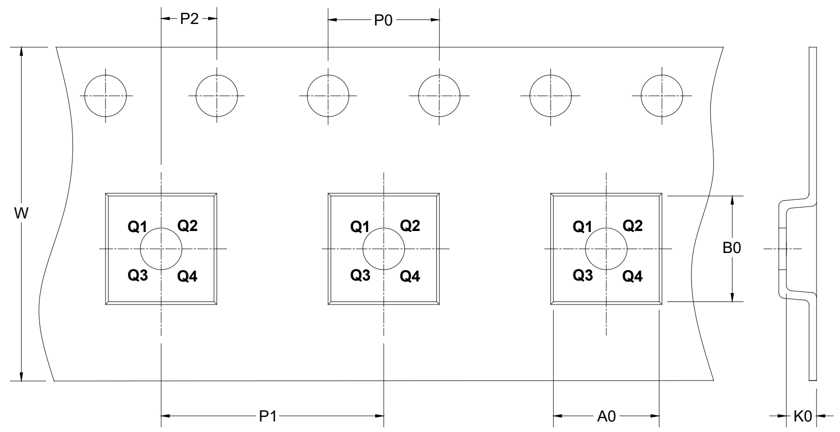
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

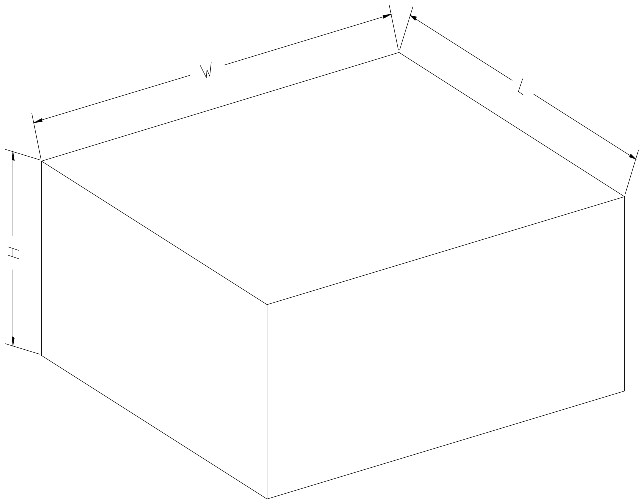
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002