SGM836
Low Quiescent Current, Programmable Delay Supervisory Circuit

GENERAL DESCRIPTION

The SGM836 family can monitor system voltages from 0.4V to 5V. When the detection voltage drops below a preset threshold (V_{IT}) or the manual reset (nMR) pin is driven low, the open-drain nRESET output is asserted. After the detection voltage and nMR voltage return above their respective thresholds, the nRESET output remains low within the user-adjustable delay time.

The SGM836 uses a precision reference to achieve 1% threshold accuracy. The reset timeout period can be set to 20ms by leaving the C_T pin open, and can be set to 300ms by connecting the C_T pin to V_{DD} by using a resistor or can be programmed from 1.25ms to 10s by connecting the SRT pin to an external capacitor. Low quiescent current makes the SGM836 very suitable for battery-powered applications.

The SGM836 is available in Green SOT-23-6 and TDFN-2×2-6AL packages. It is fully specified over a temperature range of -40℃ to +125℃.

FEATURES

- **Adjustable Reset Timeout Period: 1.25ms to 10s**
- **Low Quiescent Current: 0.6μA (TYP)**
- **High Threshold Accuracy: 1% (TYP)**
- **Factory-Set Detection Voltages from 0.9V to 5V and Adjustable Detection Voltage Down to 0.4V**
- **Manual Reset (nMR) Input**
- **Open-Drain nRESET Output**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOT-23-6 and TDFN-2×2-6AL Packages**

APPLICATIONS

Portable and Battery-Powered Products
FPGA and ASIC Applications
DSP or Microcontroller Applications
Notebook and Desktop Computers

TYPICAL APPLICATION

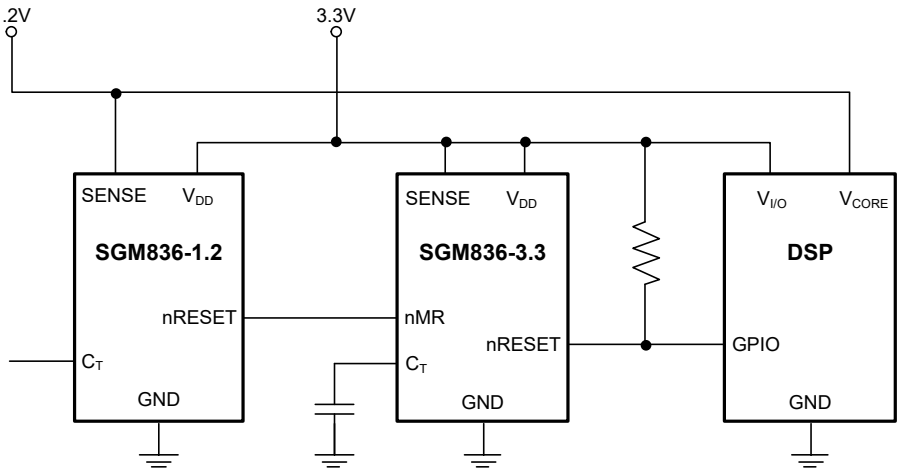


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	THRESHOLD VOLTAGE (V_{IT}) (V)	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM836-0.9	0.84	SOT-23-6	-40℃ to +125℃	SGM836-0.9XN6G/TR	R6AXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-0.9XTDI6G/TR	R18 XXXX	Tape and Reel, 3000
SGM836-1.2	1.12	SOT-23-6	-40℃ to +125℃	SGM836-1.2XN6G/TR	R6BXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.2XTDI6G/TR	R19 XXXX	Tape and Reel, 3000
SGM836-1.25	1.16	SOT-23-6	-40℃ to +125℃	SGM836-1.25XN6G/TR	R6CXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.25XTDI6G/TR	R1A XXXX	Tape and Reel, 3000
SGM836-1.5	1.40	SOT-23-6	-40℃ to +125℃	SGM836-1.5XN6G/TR	R6EXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.5XTDI6G/TR	R1B XXXX	Tape and Reel, 3000
SGM836-1.8	1.67	SOT-23-6	-40℃ to +125℃	SGM836-1.8XN6G/TR	R71XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.8XTDI6G/TR	R1C XXXX	Tape and Reel, 3000
SGM836-1.9	1.77	SOT-23-6	-40℃ to +125℃	SGM836-1.9XN6G/TR	R73XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-1.9XTDI6G/TR	R1D XXXX	Tape and Reel, 3000
SGM836-2.5	2.33	SOT-23-6	-40℃ to +125℃	SGM836-2.5XN6G/TR	R76XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-2.5XTDI6G/TR	R1E XXXX	Tape and Reel, 3000
SGM836-2.7	2.52	SOT-23-6	-40℃ to +125℃	SGM836-2.7XN6G/TR	R78XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-2.7XTDI6G/TR	R1F XXXX	Tape and Reel, 3000
SGM836-2.9	2.7	SOT-23-6	-40℃ to +125℃	SGM836-2.9XN6G/TR	R7AXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-2.9XTDI6G/TR	R20 XXXX	Tape and Reel, 3000
SGM836-3.0	2.79	SOT-23-6	-40℃ to +125℃	SGM836-3.0XN6G/TR	R3DXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-3.0XTDI6G/TR	R21 XXXX	Tape and Reel, 3000
SGM836-3.3	3.07	SOT-23-6	-40℃ to +125℃	SGM836-3.3XN6G/TR	R7CXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-3.3XTDI6G/TR	R22 XXXX	Tape and Reel, 3000
SGM836-3.7	3.45	SOT-23-6	-40℃ to +125℃	SGM836-3.7XN6G/TR	R7EXX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-3.7XTDI6G/TR	R23 XXXX	Tape and Reel, 3000
SGM836-4.0	3.73	SOT-23-6	-40℃ to +125℃	SGM836-4.0XN6G/TR	R80XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-4.0XTDI6G/TR	R24 XXXX	Tape and Reel, 3000

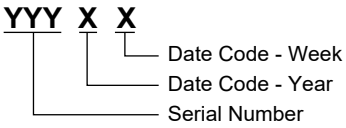
PACKAGE/ORDERING INFORMATION (continued)

MODEL	THRESHOLD VOLTAGE (V_{IT}) (V)	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM836-4.5	4.2	SOT-23-6	-40℃ to +125℃	SGM836-4.5XN6G/TR	R82XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-4.5XTDI6G/TR	R25 XXXX	Tape and Reel, 3000
SGM836-5.0	4.65	SOT-23-6	-40℃ to +125℃	SGM836-5.0XN6G/TR	R84XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-5.0XTDI6G/TR	R26 XXXX	Tape and Reel, 3000
SGM836-ADJ	0.405	SOT-23-6	-40℃ to +125℃	SGM836-ADJXN6G/TR	R85XX	Tape and Reel, 3000
		TDFN-2×2-6AL	-40℃ to +125℃	SGM836-ADJXTDI6G/TR	R27 XXXX	Tape and Reel, 3000

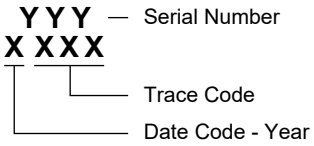
MARKING INFORMATION

NOTE: XX = Date Code. XXXX = Date Code and Trace Code.

SOT-23-6



TDFN-2×2-6AL



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to 7V
C_T to GND ..... -0.3V to V_{DD} + 0.3V
nRESET, nMR, SENSE to GND ..... -0.3V to 7V
nRESET Pin Current ..... ±5mA
Package Thermal Resistance
SOT-23-6, θ_{JA} ..... 243℃/W
TDFN-2×2-6AL, θ_{JA} ..... 124℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range, V_{DD} ..... 1.65V to 6.5V
SENSE Pin Voltage, V_{SENSE} ..... 0V to 6.5V
C_T Pin Voltage, V_{CT} ..... V_{DD} (MAX)
nMR Pin Voltage, V_{nMR} ..... 0V to 6.5V
nRESET Pin Voltage, V_{nRESET} ..... 0V to 6.5V
nRESET Pin Current, I_{nRESET} ..... 0.0003mA to 5mA
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

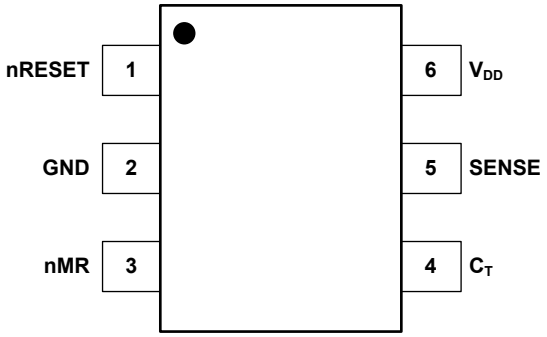
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

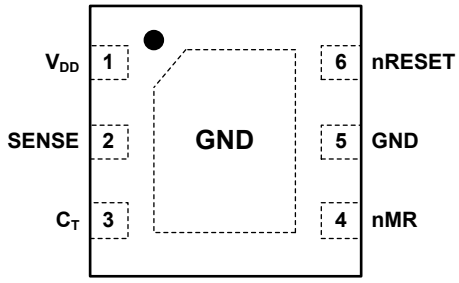
PIN CONFIGURATIONS

(TOP VIEW)



SOT-23-6

(TOP VIEW)



TDFN-2×2-6AL

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
SOT-23-6	TDFN-2×2-6AL			
1	6	nRESET	O	Active-Low Reset Output. When the SENSE input is lower than V_{IT} or the nMR pin is set to logic low, nRESET is asserted and driven to a low-impedance state. nRESET remains low (asserted) for the reset timeout period after both V_{SENSE} exceeds V_{IT} and nMR pin is driven high. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin and allows the reset pin to attain voltages higher than V_{DD}.
2	5	GND	—	Ground.
3	4	nMR	I	Manual Reset Input Pin. Pulling this pin (nMR) low will assert nRESET. nMR is internally pulled up to V_{DD} by a 100kΩ resistor.
4	3	C_T	I	Reset Timeout Delay Programming Pin. Connecting this pin to V_{DD} through a 40kΩ to 200kΩ resistor or leaving it open results in fixed delay times. Connecting this pin to a ground referenced capacitor ≥ 100pF gives a user-programmable delay time.
5	2	SENSE	I	The Dedicated Voltage Monitor Pin. If the voltage at this terminal drops below the threshold voltage V_{IT}, then nRESET is asserted.
6	1	V_{DD}	I	Supply Voltage.
—	Exposed Pad	GND	—	Exposed Pad. Connect to ground.

NOTE: I: input, O: output.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.65V to 6.5V, R_{LRESET} = 100kΩ (1), T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V_{DD}		1.65		6.5	V
Supply Current (Current into V_{DD} Pin)	I_{DD}	V_{DD} = 3.3V, nRESET not asserted, nMR, nRESET, C_T open		0.6	1.5	μA
		V_{DD} = 6.5V, nRESET not asserted, nMR, nRESET, C_T open		0.9	2	
Low-Level Output Voltage	V_{OL}	1.3V ≤ V_{DD} < 1.8V, I_{OL} = 0.4mA			0.2	V
		1.8V ≤ V_{DD} ≤ 6.5V, I_{OL} = 1mA			0.3	
Power-Up Reset Voltage (2)	V_{POR}	V_{OL} (MAX) = 0.2V, I_{nRESET} = 15μA			0.8	V
Negative-Going Input Threshold Accuracy	V_{IT}	All versions, T_J = +25℃	-1.0		1.0	%
		V_{IT} ≤ 3.3V	-1.5		1.5	
		3.3V < V_{IT} ≤ 5.0V	-1.8		1.8	
		V_{IT} ≤ 3.3V, T_J = -40℃ to +85℃	-1.25		1.25	
		3.3V < V_{IT} ≤ 5.0V, T_J = -40℃ to +85℃	-1.3		1.3	
Hysteresis On V_{IT}	V_{HYS}	All versions			3.5	%
nMR Internal Pull-Up Resistance	R_{nMR}		50	100		kΩ
Input Current at SENSE Pin	I_{SENSE}	SGM836-ADJ, V_{SENSE} = V_{IT}	-25		25	nA
		Fixed versions, V_{SENSE} = 6.5V		235		
nRESET Leakage Current	I_{OH}	V_{nRESET} = 6.5V, nRESET not asserted			1	μA
Input Capacitance, any Pin	C_{IN}	C_T pin, V_{IN} = 0V to V_{DD}		5		pF
		Other pins, V_{IN} = 0V to 6.5V		5		
nMR Input	V_{IL}	Logic Low	0		0.3 × V_{DD}	V
	V_{IH}	Logic High	0.7 × V_{DD}		V_{DD}	
Input Pulse Width to nRESET	t_{SENSE}	V_{IH} = 1.05 × V_{IT}, V_{IL} = 0.95 × V_{IT}		25		μs
	t_{nMR}	V_{IH} = 0.7 × V_{DD}, V_{IL} = 0.3 × V_{DD}		100		ns
C_T Source Threshold Voltage	$V_{TH-RAMP}$			1.206		V
nRESET Delay Time	t_D	C_T = Open	12	20	28	ms
		C_T = V_{DD}	180	300	420	
		C_T = 100pF	0.8	1.3	1.8	
Propagation Delay	t_{MR}	nMR to nRESET		250		ns
High-to-Low Level nRESET Delay	t_{RP0}	SENSE to nRESET		100		μs

NOTE:

1. R_{LRESET} is the resistor connected to the nRESET pin.

TIMING DIAGRAM

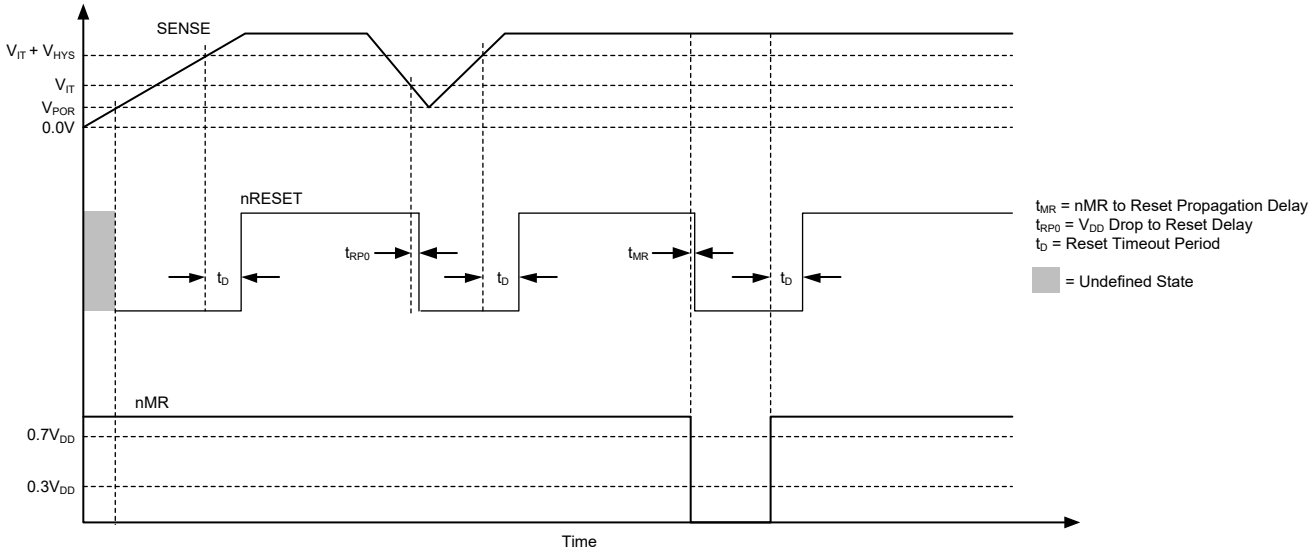
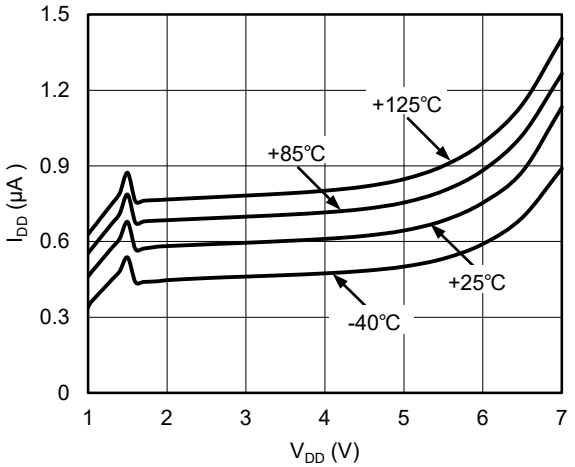


Figure 2. SGM836 Timing Diagram Showing nMR and SENSE Reset Timing

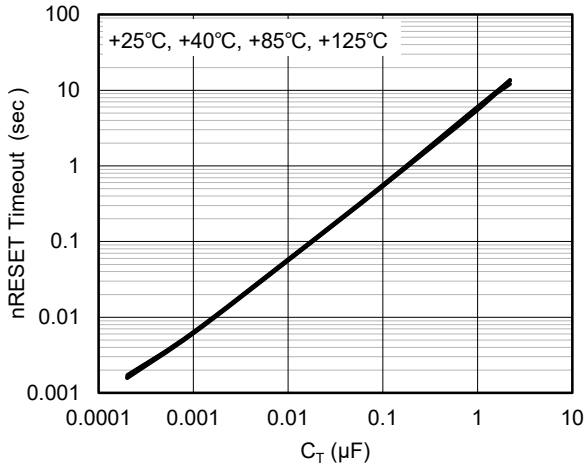
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, V_{DD} = 3.3V and R_{LRESET} = 100kΩ, unless otherwise noted.

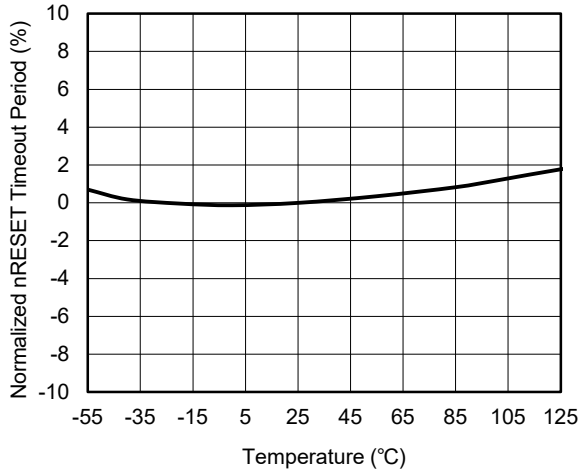
Supply Current vs. Supply Voltage



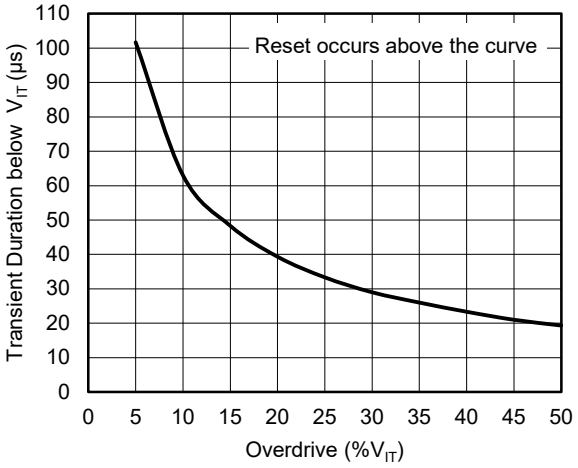
nRESET Timeout Period vs. C_T



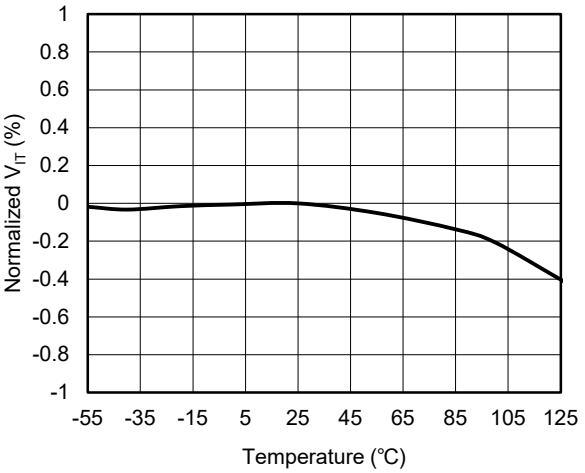
Normalized nRESET Delay Time vs. Temperature
(C_T = Open, C_T = V_{DD}, C_T = Any)



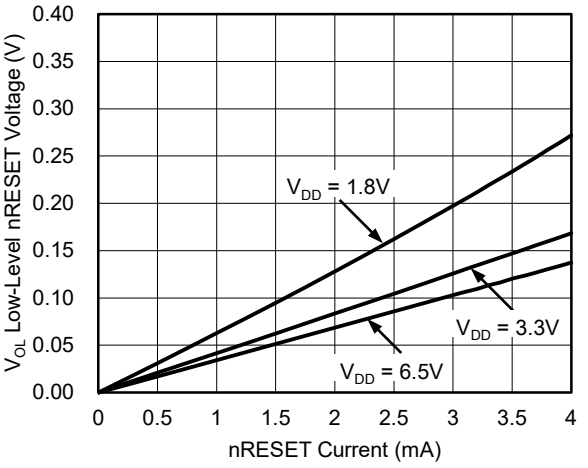
Maximum Transient Duration at SENSE vs. SENSE Threshold Overdrive Voltage



Normalized SENSE Threshold Voltage (V_{IT}) vs. Temperature



Low-Level nRESET Voltage vs. nRESET Current



FUNCTIONAL BLOCK DIAGRAM

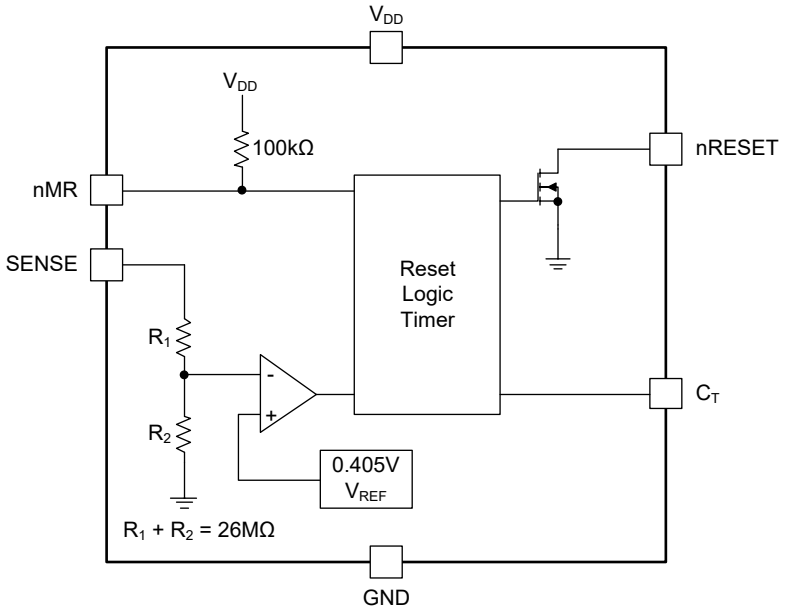


Figure 3. Fixed Voltage Version Block Diagram

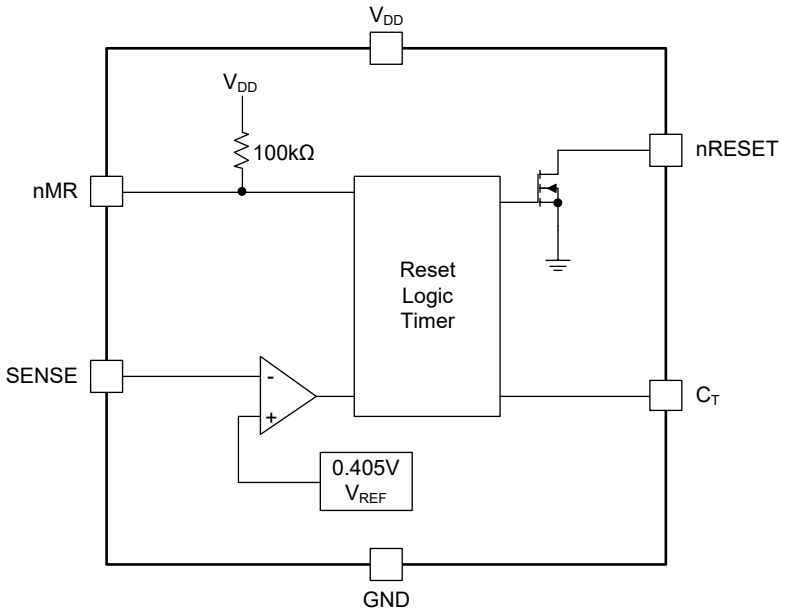


Figure 4. Adjustable Voltage Version Block Diagram

DETAILED DESCRIPTION

When the SENSE voltage drops below V_{IT} or the nMR pin is driven low, the open-drain nRESET output is asserted. After the SENSE voltage and nMR voltage return above their respective thresholds, the nRESET output remains low within the user-adjustable delay time.

Feature Description

The SGM836 device has a reset delay time adjustment function and a wide range of detection thresholds, so it can be widely used in various applications. The detection threshold voltages are factory-set from 0.9V to 5V, while the SGM836-ADJ can be set to any voltage above 0.405V with an external resistance divider. Two preset reset timeout delays are pin configurable: connecting the C_T pin to V_{DD} results in a 300ms reset timeout delay; leaving the C_T pin floating provides a 20ms reset timeout delay. In addition, connecting a capacitor between C_T pin and ground allows a programmable reset timeout period from 1.25ms to 10s.

SENSE Input

The SENSE pin is dedicated for voltage monitor. If the voltage on this pin drops below V_{IT}, nRESET is asserted. The comparator with built-in hysteresis ensures smooth nRESET and deassetion. It is recommended to connect a bypass capacitor from 1nF to 10nF at the SENSE pin to reduce the sensitivity to voltage transient and PCB layout parasitics.

The SGM836 immunes to short negative transients on the SENSE pin. Sensitivity to transients is dependent on the voltage overdrive on this pin.

The SGM836-ADJ can be used to monitor any voltage rail down to 0.405V using the circuit shown in Figure 5.

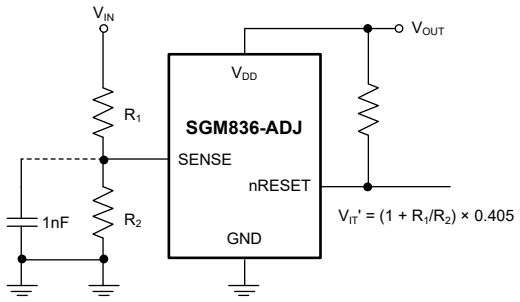


Figure 5. Using the SGM836-ADJ to Monitor a User-Defined Threshold Voltage

Selecting the Reset Delay Time

The SGM836 provides three methods to set the reset timeout delay as shown in Figure 6. Figure 6 (a) shows the configuration for a fixed 300ms typical delay time by connecting the C_T pin to V_{DD}; a resistor from 40kΩ to 200kΩ must be used. The resistor value will not affect the supply current. Figure 6 (b) shows a fixed 20ms delay time by leaving the C_T pin open. Figure 6 (c) shows a user-defined programmable time between 1.25ms and 10s by connecting a capacitor between the C_T pin and the ground.

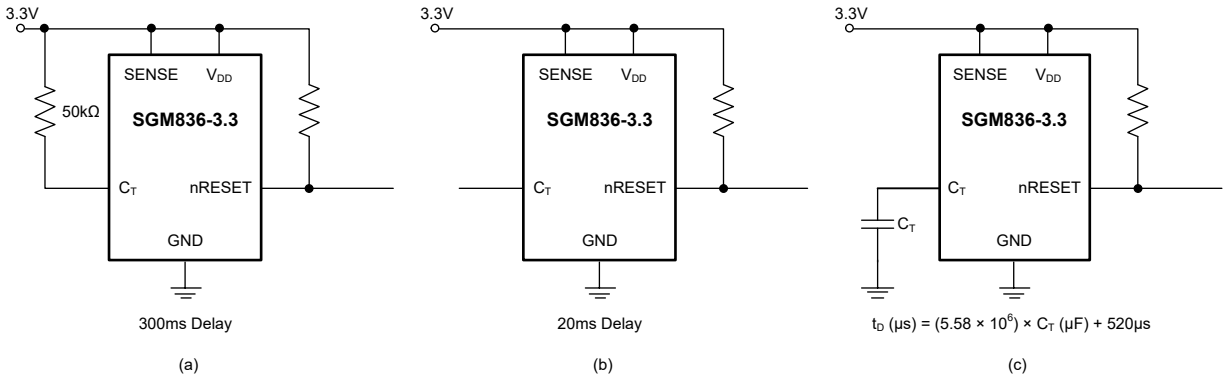


Figure 6. Configuration Used to Set the nRESET Delay Time

DETAILED DESCRIPTION (continued)

The capacitor C_T should be at least 100pF nominal value so that the SGM836 can identify the presence of the capacitor. The reset timeout delay can be calculated using Equation 1.

$$t_D\ (\mu s) = (5.58 \times 10^6) \times C_T\ (\mu F) + 520\mu s \qquad (1)$$

The reset timeout delay is determined by the time required to charge the external capacitor to 1.206V with the on-chip precise 216nA current source.

When nRESET is asserted, the capacitor is discharged. After clearing the nRESET condition, the internal current source will be enabled and the external capacitor will be charged. When the voltage on the capacitor reaches 1.206V, nRESET is set to invalid. Please note that low leakage capacitors such as ceramics should be used, and the stray capacitance around the pins may cause errors in the reset delay time.

Manual RESET (nMR) Input

The nMR input allows a processor or other logic circuits to initiate a reset. When nMR is set to logic low (0.3 × V_{DD}), the nRESET is asserted. After nMR returns to logic high and SENSE exceeds its reset threshold, nRESET is deasserted after the user-defined reset delay expires. Note that nMR is internally connected to V_{DD} through a 100kΩ resistor, so if nMR is not used, this pin can be left open.

Figure 7 shows how to use nMR to monitor multiple system voltages. Note that if the logic signal does not drive nMR fully to V_{DD}, there will be some extra current drawn into V_{DD} due to an internal pull-up resistor on nMR. To minimize current draw, an external FET can be used as shown in Figure 8.

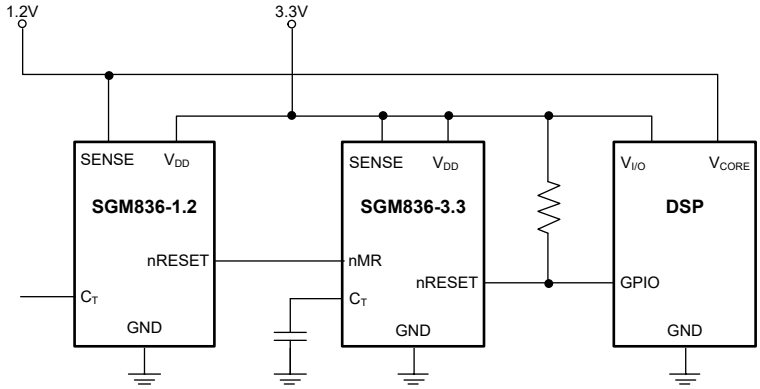


Figure 7. Using nMR to Monitor Multiple System Voltages

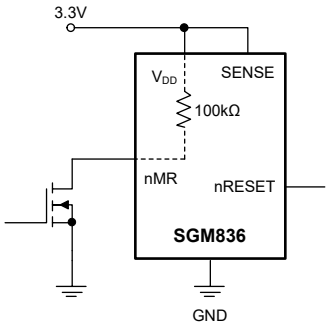


Figure 8. Using an External MOSFET to Minimize I_{DD} When nMR Signal Does not Go to V_{DD}

DETAILED DESCRIPTION (continued)

nRESET Output

As long as SENSE voltage exceeds V_{IT} and the nMR is logic high, nRESET remains high (deasserted). If either V_{SENSE} is lower than V_{IT} or nMR is driven low, nRESET is asserted, driving the nRESET pin to a low-impedance state.

Once the nMR is logic high again and SENSE voltage exceeds V_{IT} + V_{HYS}, a delay circuit is enabled, keeping nRESET low for a specified reset delay period. Once the reset delay has expired, the nRESET pin enters a high-impedance state. The pull-up resistor from the nRESET pin to the power supply can be used to reset the microprocessor signal to have a voltage above V_{DD} voltage. The pull-up resistor should be no smaller than 10kΩ due to the limited nRESET pull-down ability.

Device Functional Modes

Table 1. Truth Table

nMR	SENSE > V_{IT}	nRESET
L	0	L
L	1	L
H	0	L
H	1	H

Normal Operation (V_{DD} > V_{DD_MIN})

When the V_{DD} voltage is higher than V_{DD_MIN}, the logic state of nRESET is determined by V_{SENSE} and the logic state of nMR.

• nMR high: When V_{DD} voltage is higher than 1.65V for a selected time (t_D), the nRESET logic state corresponds to V_{SENSE} relative to V_{IT}.

• nMR low: In this mode, nRESET is held low regardless of V_{SENSE}.

Above Power-On Reset but Lower than V_{DD_MIN} (V_{POR} < V_{DD} < V_{DD_MIN})

When the V_{DD} voltage is lower than V_{DD_MIN} and higher than the power-on reset voltage (V_{POR}), the nRESET is asserted and driven to a low-impedance state.

Below Power-On Reset (V_{DD} < V_{POR})

When the V_{DD} voltage is lower than the required voltage (V_{POR}), the nRESET voltage is undefined. In the case of nRESET pulling up to V_{DD} through a 100kΩ resistor, nRESET voltage is equal to or lower than V_{DD} voltage.

APPLICATION INFORMATION

Figure 9 shows a typical application of the SGM836-2.5 used with a 2.5V processor. The nRESET output is typically connected to the nRESET input of a microprocessor. A pull-up resistor is necessary to keep the nRESET logic high when nRESET is not asserted.

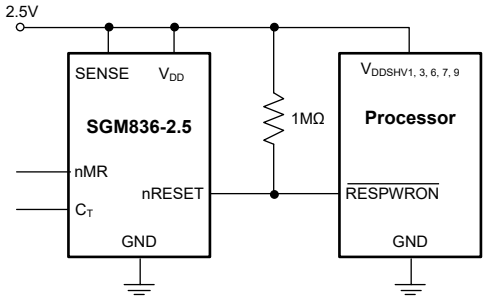


Figure 9. Typical Application of the SGM836 with a Processor

Design Requirements

The SGM836 is intended to drive the nRESET input of a microprocessor. The nRESET pin is pulled high with a 1MΩ resistor and the reset delay time is controlled by C_T depending on the reset requirement time of the microprocessor. In this case, C_T is left open for a typical reset delay time of 20ms.

Detailed Design Procedure

The primary constraint for this application is the reset timeout period. In this case, because C_T is open, the reset timeout period is set to 20ms. A 0.1μF decoupling capacitor is connected to the V_{DD} pin and a 1MΩ resistor is used to pull the nRESET pin high.

Immunity to SENSE Pin Voltage Transients

The SGM836 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients depends on threshold overdrive. Threshold overdrive is defined by how much the V_{SENSE} exceeds the specified threshold and is important to know because the smaller the overdrive is, the slower the nRESET responses. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 2:

$$\text{Overdrive} = | (V_{SENSE} / V_{IT} - 1) \times 100\% | \quad (2)$$

where:

V_{IT} is the threshold voltage.

Power Supply Recommendations

The device is designed to operate from an input supply with a voltage range from 1.65V to 6.5V.

Layout Guidelines

It is recommended to place a 0.1μF ceramic capacitor near the V_{DD} pin. If there is no capacitor connected to the C_T pin, parasitic capacitance on this pin should be minimized so the nRESET delay time is not significantly affected.

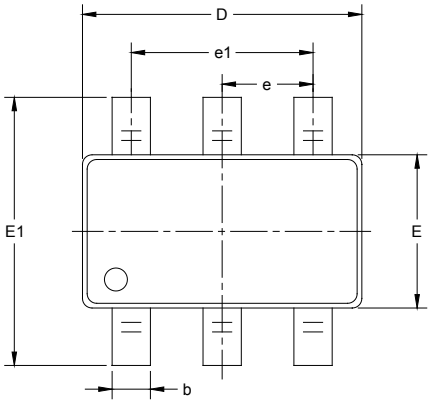
REVISION HISTORY

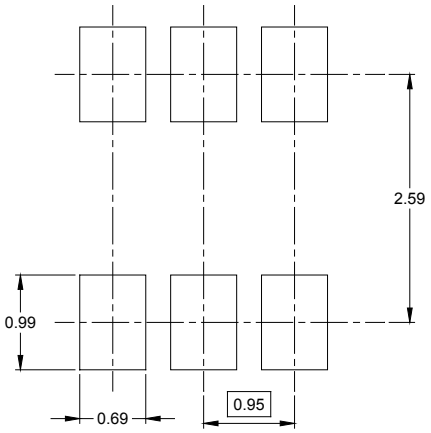
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (JANUARY 2021) to REV.A	Page
Changed from product preview to production data	All

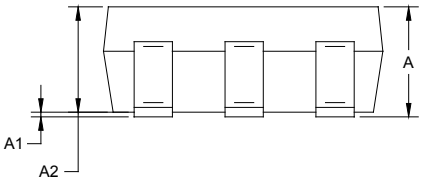
PACKAGE OUTLINE DIMENSIONS

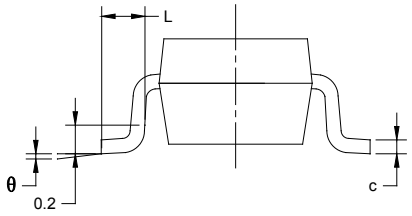
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)

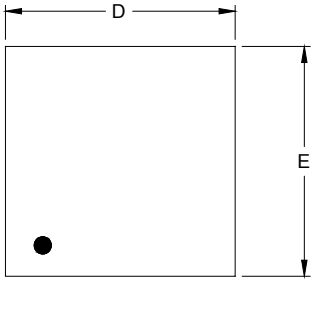




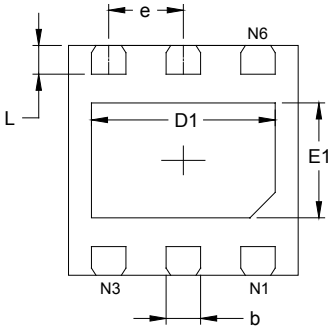
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

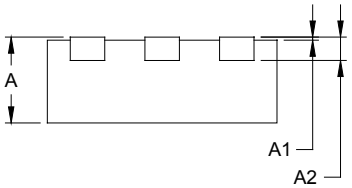
TDFN-2×2-6AL



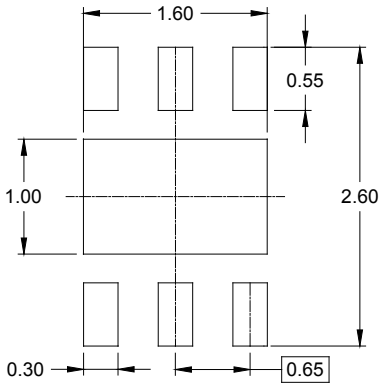
TOP VIEW



BOTTOM VIEW



SIDE VIEW

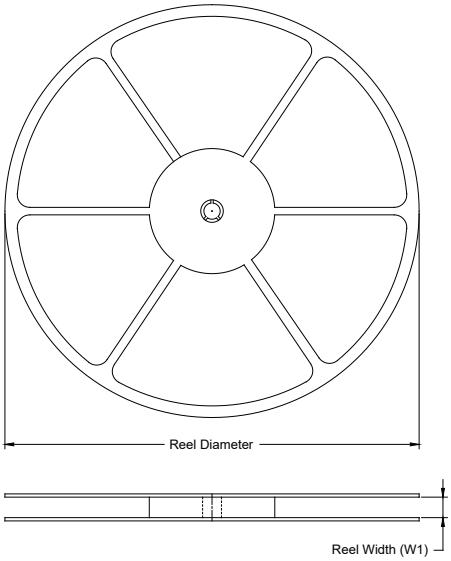


RECOMMENDED LAND PATTERN (Unit: mm)

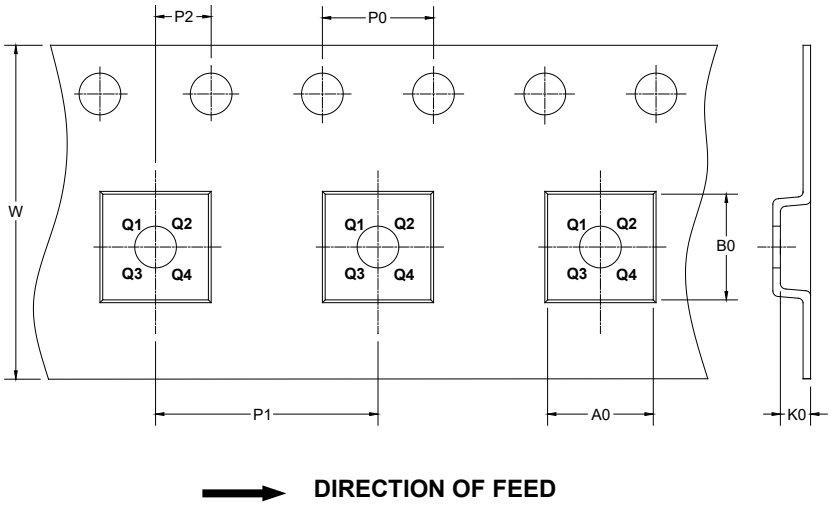
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	**MAX**	**MIN**	**MAX**
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.500	1.700	0.059	0.067
E	1.900	2.100	0.075	0.083
E1	0.900	1.100	0.035	0.043
b	0.250	0.350	0.010	0.014
e	0.650 BSC		0.026 BSC	
L	0.174	0.326	0.007	0.013

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



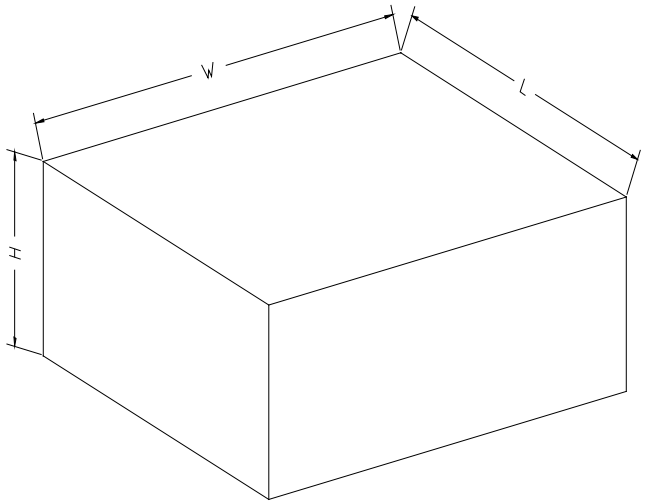
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7″	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3
TDFN-2×2-6AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002