SGM895/SGM896/SGM897/SGM898/SGM899
Ultra-Small, Supervisory Circuits with Adjustable Sequencing

GENERAL DESCRIPTION

The SGM895/SGM896/SGM897/SGM898/SGM899 are ultra-small, low-power and high-accuracy micro-processor supervisory circuits with adjustable sequencing capability. Since the high-impedance detection input pin (IN) with a 0.5V threshold voltage is separated from the power supply, these devices offer tremendous flexibility with an adjustable threshold using an external resistive divider. Moreover, the delay time can be adjusted by an external capacitor connected to the CDELAY pin. These devices are ideal for power-supply sequencing, reset sequencing and power-switching applications.

When the input voltage at IN (V_{IN}) exceeds the V_{TH} threshold voltage (0.5V, TYP) and the enable input is asserted (ENABLE = high or nENABLE = low), the output asserts (OUT = high or nOUT = low). When V_{IN} falls below V_{TH} - V_{HYST} (0.495V, TYP) or when the enable input is deasserted (ENABLE = low or nENABLE = high), the output deasserts (OUT = low or nOUT = high). All devices provide a capacitor-adjustable input delay time (t_{DELAY}) from when V_{IN} exceeds V_{TH} to when the output asserts. The SGM89_A provide the same capacitor-adjustable delay time from when the enable is asserted to when the output asserts, whereas the SGM89_P provide a 350ns (TYP) propagation delay time from when the enable is asserted to when the output asserts.

The SGM895 provides an active-high enable input and an active-high push-pull output. The SGM896 provides an active-low enable input and an active-low push-pull output. The SGM897 provides an active-high enable input and an active-high open-drain output. The SGM898 provides an active-low enable input and an active-low open-drain output. Finally, the SGM899 provides an active-low enable with an active-high push-pull output.

All devices are available in ultra-small Green UTDFN-1.45×1-6AL and TSOT-23-6 packages.

FEATURES

- **High Voltage Threshold Accuracy:**
  - **+25℃: ±1%**
  - **-40℃ to +125℃: ±1.6%**
- **Low Power Consumption: 2.1μA (TYP)**
- **Operating Supply Voltage Range: 1.6V to 5.5V**
- **Capacitor-Adjustable Delay**
- **Active-High/Active-Low Enable Input Options**
- **Active-High/Active-Low Output Options**
- **Open-Drain (28V Tolerant)/Push-Pull Output Options**
- **Available in Ultra-Small Green UTDFN-1.45×1-6AL and TSOT-23-6 Packages**

APPLICATIONS

Portable Equipment
Computers/Servers
Critical μP Monitoring
Automotive
Medical Equipment
Intelligent Instruments

TYPICAL APPLICATION

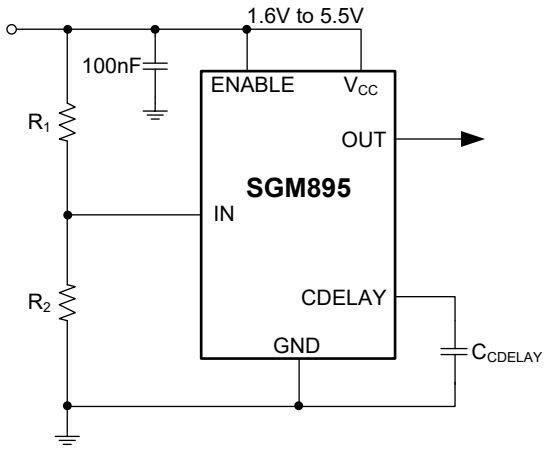


Figure 1. Typical Application Circuit

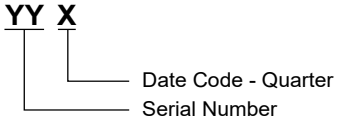
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM895A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM895AXUDL6G/TR	J9X	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM895AXTN6G/TR	CICXX	Tape and Reel, 3000
SGM895P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM895PXUDL6G/TR	IAX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM895PXTN6G/TR	CKFXX	Tape and Reel, 3000
SGM896A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM896AXUDL6G/TR	L6X	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM896AXTN6G/TR	CL0XX	Tape and Reel, 3000
SGM896P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM896PXUDL6G/TR	L7X	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM896PXTN6G/TR	CL1XX	Tape and Reel, 3000
SGM897A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM897AXUDL6G/TR	I8X	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM897AXTN6G/TR	CIDXX	Tape and Reel, 3000
SGM897P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM897PXUDL6G/TR	IBX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM897PXTN6G/TR	CL2XX	Tape and Reel, 3000
SGM898A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM898AXUDL6G/TR	L9X	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM898AXTN6G/TR	CL3XX	Tape and Reel, 3000
SGM898P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM898PXUDL6G/TR	LAX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM898PXTN6G/TR	CL4XX	Tape and Reel, 3000
SGM899A	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM899AXUDL6G/TR	I9X	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM899AXTN6G/TR	CIEXX	Tape and Reel, 3000
SGM899P	UTDFN-1.45×1-6AL	-40°C to +125°C	SGM899PXUDL6G/TR	ICX	Tape and Reel, 5000
	TSOT-23-6	-40°C to +125°C	SGM899PXTN6G/TR	CL5XX	Tape and Reel, 3000

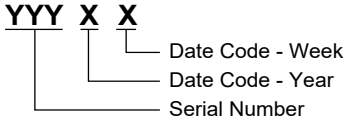
MARKING INFORMATION

NOTE: X = Date Code. XX = Date Code

UTDFN-1.45×1-6AL



TSOT-23-6



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{CC}, ENABLE, nENABLE, IN ..... -0.3V to 6V
OUT, nOUT (Push-Pull) .....-0.3V to V_{CC} + 0.3V
OUT, nOUT (Open-Drain) ..... -0.3V to 30V
CDELAY.....-0.3V to V_{CC} + 0.3V
Output Current (All Pins).....±20mA
Package Thermal Resistance
UTDFN-1.45×1-6AL, θ_{JA} ..... 294℃/W
TSOT-23-6, θ_{JA} ..... 230℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Junction Temperature Range .....-40℃ to +125℃
Operating Ambient Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

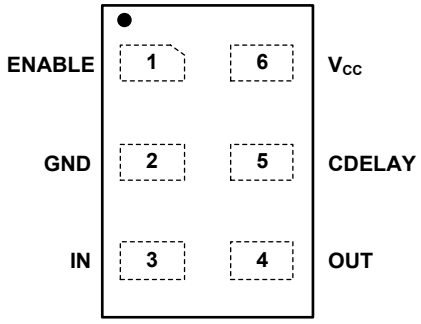
SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

SELECTOR GUIDE

DEVICE	ENABLE INPUT	OUTPUT	INPUT DELAY TIME	ENABLE DELAY TIME
SGM895A	Active-High	Active-High, Push-Pull	Capacitor-Adjustable	Capacitor-Adjustable
SGM895P	Active-High	Active-High, Push-Pull	Capacitor-Adjustable	350ns Delay
SGM896A	Active-Low	Active-Low, Push-Pull	Capacitor-Adjustable	Capacitor-Adjustable
SGM896P	Active-Low	Active-Low, Push-Pull	Capacitor-Adjustable	350ns Delay
SGM897A	Active-High	Active-High, Open-Drain	Capacitor-Adjustable	Capacitor-Adjustable
SGM897P	Active-High	Active-High, Open-Drain	Capacitor-Adjustable	350ns Delay
SGM898A	Active-Low	Active-Low, Open-Drain	Capacitor-Adjustable	Capacitor-Adjustable
SGM898P	Active-Low	Active-Low, Open-Drain	Capacitor-Adjustable	350ns Delay
SGM899A	Active-Low	Active-High, Push-Pull	Capacitor-Adjustable	Capacitor-Adjustable
SGM899P	Active-Low	Active-High, Push-Pull	Capacitor-Adjustable	350ns Delay

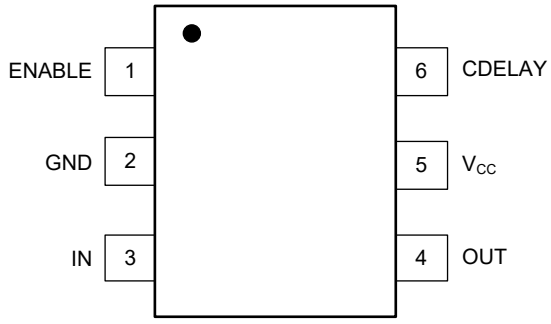
PIN CONFIGURATIONS

SGM895/SGM897 (TOP VIEW)



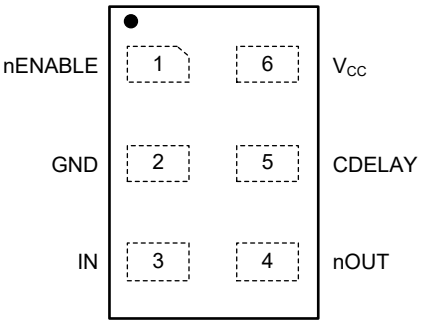
UTDFN-1.45×1-6AL

SGM895/SGM897 (TOP VIEW)



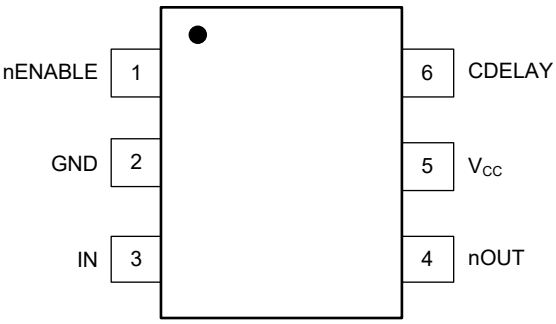
TSOT-23-6

SGM896/SGM898 (TOP VIEW)



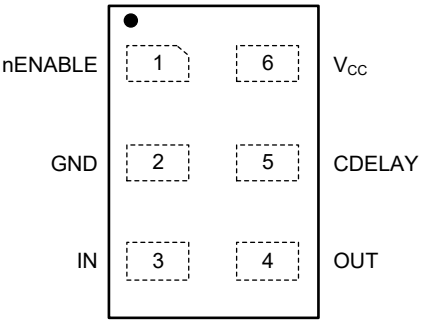
UTDFN-1.45×1-6AL

SGM896/SGM898 (TOP VIEW)



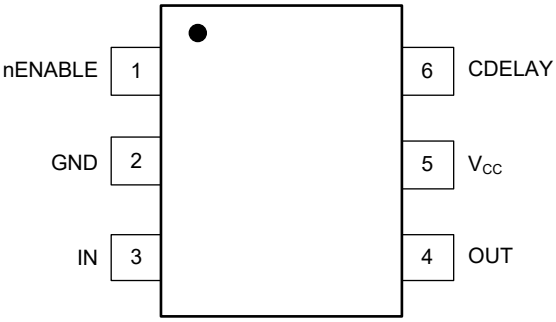
TSOT-23-6

SGM899 (TOP VIEW)



UTDFN-1.45×1-6AL

SGM899 (TOP VIEW)



TSOT-23-6

PIN DESCRIPTION

PIN						NAME	FUNCTION
SGM895/SGM897		SGM896/SGM898		SGM899			
UTDFN-1.45×1-6AL	TSOT-23-6	UTDFN-1.45×1-6AL	TSOT-23-6	UTDFN-1.45×1-6AL	TSOT-23-6		
1	1	—	—	—	—	ENABLE	Active-High Enable Input. Set ENABLE low immediately to deassert the output to its false state (OUT = low) independent of V_{IN}. With V_{IN} above V_{TH}, set ENABLE high to assert the output to its true state (OUT = high) after the CDELAY adjustable delay period (SGM89_A) or a 350ns propagation delay (SGM89_P).
—	—	1	1	1	1	nENABLE	Active-Low Enable Input. Set nENABLE high immediately to deassert the output to its false state (OUT = low or nOUT = high) independent of V_{IN}. With V_{IN} above V_{TH}, set nENABLE low to assert the output to its true state (OUT = high or nOUT = low) after the CDELAY adjustable delay period (SGM89_A) or a 350ns propagation delay (SGM89_P).
2	2	2	2	2	2	GND	Ground.
3	3	3	3	3	3	IN	High-Impedance Detection Input. Connect the IN pin to an external resistive divider to set the desired detection threshold. The output state changes when V_{IN} exceeds V_{TH} (0.5V, TYP) or when V_{IN} drops below V_{TH} - V_{HYST} (0.495V, TYP).
4	4	—	—	4	4	OUT	Active-High Output, Push-Pull (SGM895/SGM899) or Open-Drain (SGM897). When V_{IN} exceeds V_{TH} and the enable input is asserted (ENABLE = high or nENABLE = low), the output asserts (OUT = high) after the CDELAY adjustable delay period. The output deasserts (OUT = low) immediately after V_{IN} drops below V_{TH} - V_{HYST} or the enable input is deasserted (ENABLE = low or nENABLE = high). The open-drain version requires an external pull-up resistor.
—	—	4	4	—	—	nOUT	Active-Low Output, Push-Pull (SGM896) or Open-Drain (SGM898). When V_{IN} exceeds V_{TH} and the enable input is asserted (nENABLE = low), the output asserts (nOUT = low) after the CDELAY adjustable delay period. The output deasserts (nOUT = high) immediately after V_{IN} drops below V_{TH} - V_{HYST} or the enable input is deasserted (nENABLE = high). The open-drain version requires an external pull-up resistor.
5	6	5	6	5	6	CDELAY	Capacitor-Adjustable Delay. Connect an external capacitor (C_{CDELAY}) between CDELAY and GND to set the delay period. t_{DELAY} (ms) = 3.95 × C_{CDELAY} (nF) + 0.048ms There is a 50μs (TYP) fixed delay for the output deasserting when V_{IN} falls below V_{TH} - V_{HYST}.
6	5	6	5	6	5	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.6V to 5.5V, Full = -40℃ to +125℃, typical values are at V_{CC} = 3.3V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Supply							
Operating Voltage Range	V_{CC}		Full	1.6		5.5	V
Under-Voltage Lockout (1)	V_{UVLO}	V_{CC} falling	Full	1.31		1.49	V
V_{CC} Supply Current	I_{CC}		Full		2.1	7.8	μA
IN							
Threshold Voltage	V_{TH}	V_{IN} rising, 1.6V < V_{CC} < 5.5V	+25℃	0.495	0.500	0.505	V
			Full	0.492	0.500	0.508	
Hysteresis	V_{HYST}	V_{IN} falling	Full		5		mV
Input Current	I_{IN}	V_{IN} = 0V or V_{CC}	Full	-20		20	nA
CDELAY							
Delay Charge Current	I_{CD}		Full	210	253	290	nA
Delay Threshold	V_{TCD}	CDELAY rising	Full	0.96	1.00	1.04	V
CDELAY Pull-Down Resistance	R_{CDELAY}		Full		120	350	Ω
ENABLE/nENABLE							
Input Low Voltage	V_{IL}		Full			0.4	V
Input High Voltage	V_{IH}		Full	1.4			V
Input Leakage Current	I_{LEAK}	ENABLE, nENABLE = V_{CC} or GND	Full	-50		50	nA
OUT/nOUT							
Output Low Voltage (Open-Drain or Push-Pull)	V_{OL}	V_{CC} ≥ 1.2V, I_{SINK} = 90μA, SGM895/SGM897/SGM899 only	Full			0.3	V
		V_{CC} ≥ 2.25V, I_{SINK} = 0.5mA	Full			0.3	
		V_{CC} ≥ 4.5V, I_{SINK} = 1mA	Full			0.4	
Output High Voltage (Push-Pull)	V_{OH}	V_{CC} ≥ 2.25V, I_{SOURCE} = 500μA	Full	0.8 × V_{CC}			V
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800μA	Full	0.8 × V_{CC}			
Output Open-Drain Leakage Current	I_{LKG}	Output high impedance, V_{OUT} = 28V	Full			1	μA
Timing							
IN to OUT/nOUT Propagation Delay	t_{DELAY}	V_{IN} rising, C_{CDELAY} = 0nF	Full		48		μs
		V_{IN} rising, C_{CDELAY} = 47nF	Full		185		ms
	t_{DL}	V_{IN} falling	Full		50		μs
ENABLE/nENABLE Minimum Input Pulse Width	t_{PW}		Full	1.1			μs
ENABLE/nENABLE Glitch Rejection			Full		210		ns
ENABLE/nENABLE to OUT/nOUT Delay	t_{OFF}	From device enabled to device disabled	Full		350		ns
ENABLE/nENABLE to OUT/nOUT Delay	t_{PROPP}	From device disabled to device enabled (SGM89_P)	Full		350		ns
	t_{PROPA}	From device disabled to device enabled (SGM89_A), C_{CDELAY} = 0nF	Full		30		μs
		From device disabled to device enabled (SGM89_A), C_{CDELAY} = 47nF	Full		185		ms

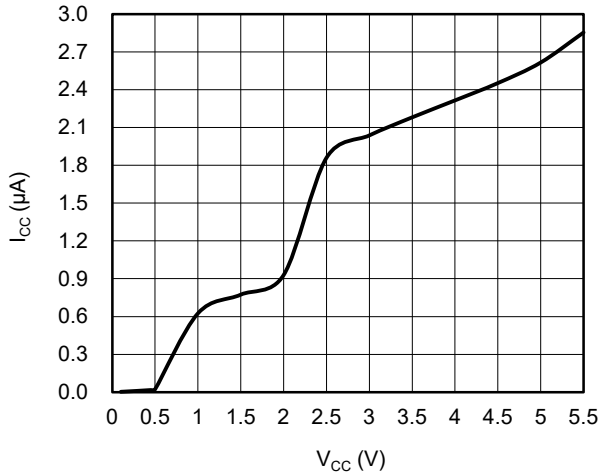
NOTES:

1. When V_{CC} falls below the UVLO threshold, the outputs will deassert (OUT goes low or nOUT goes high).
2. The output state is not guaranteed when V_{CC} falls below 1.2V.
3. During the initial power-up, V_{CC} must exceed 1.6V for at least 2ms before the output is guaranteed to be in the correct state.

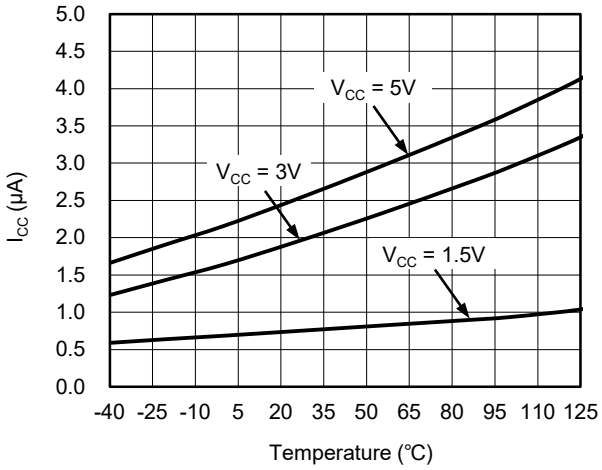
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V and T_J = +25℃, unless otherwise noted.

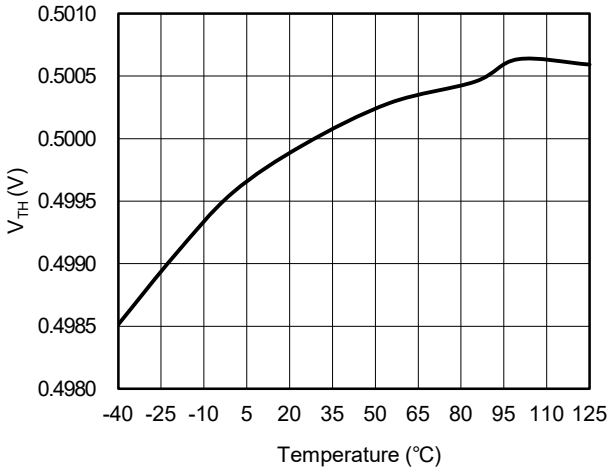
Supply Current vs. Supply Voltage



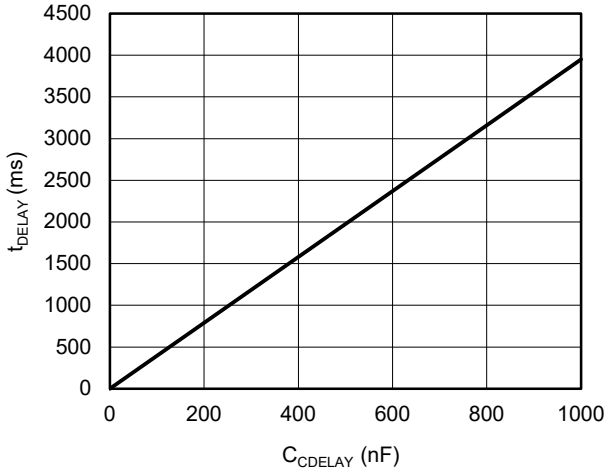
Supply Current vs. Temperature



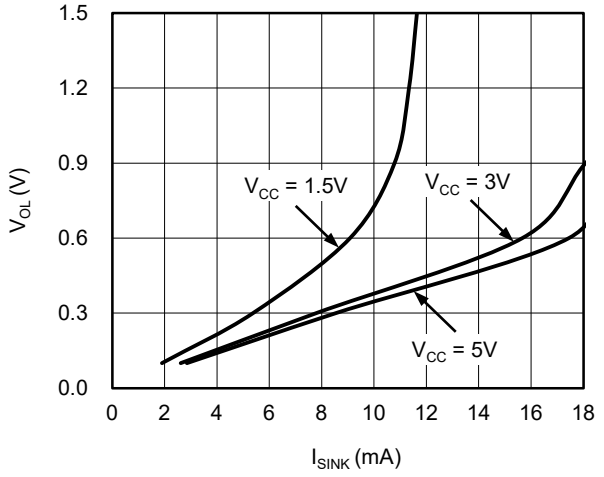
IN Threshold vs. Temperature



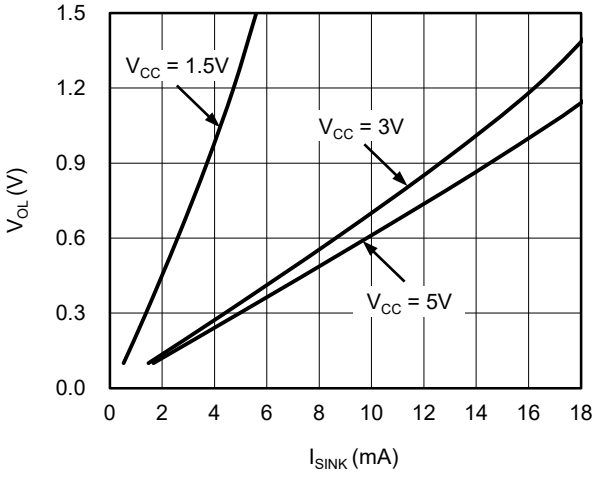
OUT Delay vs. C_{CDELAY}



Output Low Voltage vs. Sink Current
(SGM895/SGM896/SGM899)



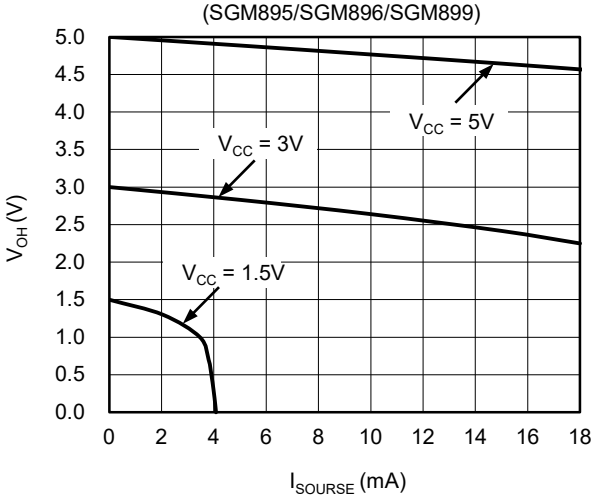
Output Low Voltage vs. Sink Current
(SGM897/SGM898)



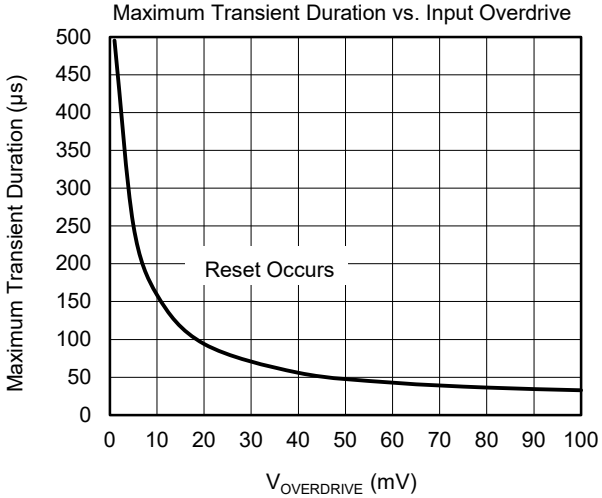
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{CC} = 3.3V and T_J = +25℃, unless otherwise noted.

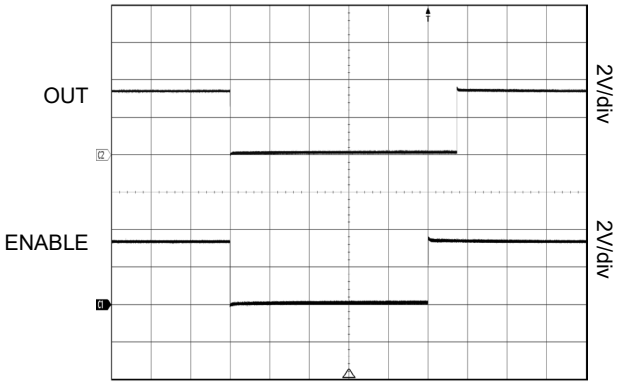
Output High Voltage vs. Source Current
(SGM895/SGM896/SGM899)



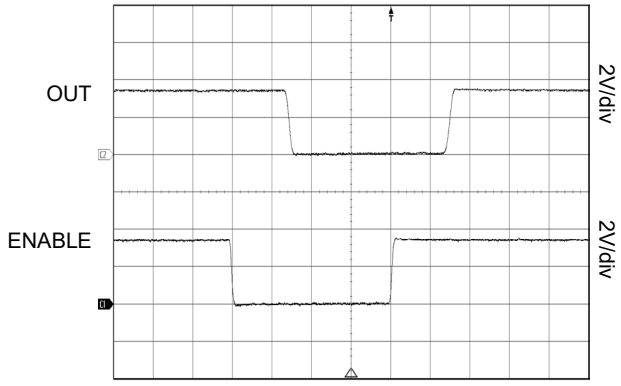
Maximum Transient Duration vs. Input Overdrive



Enable Turn-On/Off Delay (SGM895A)



Enable Turn-On/Off Delay (SGM895P)



FUNCTIONAL BLOCK DIAGRAM

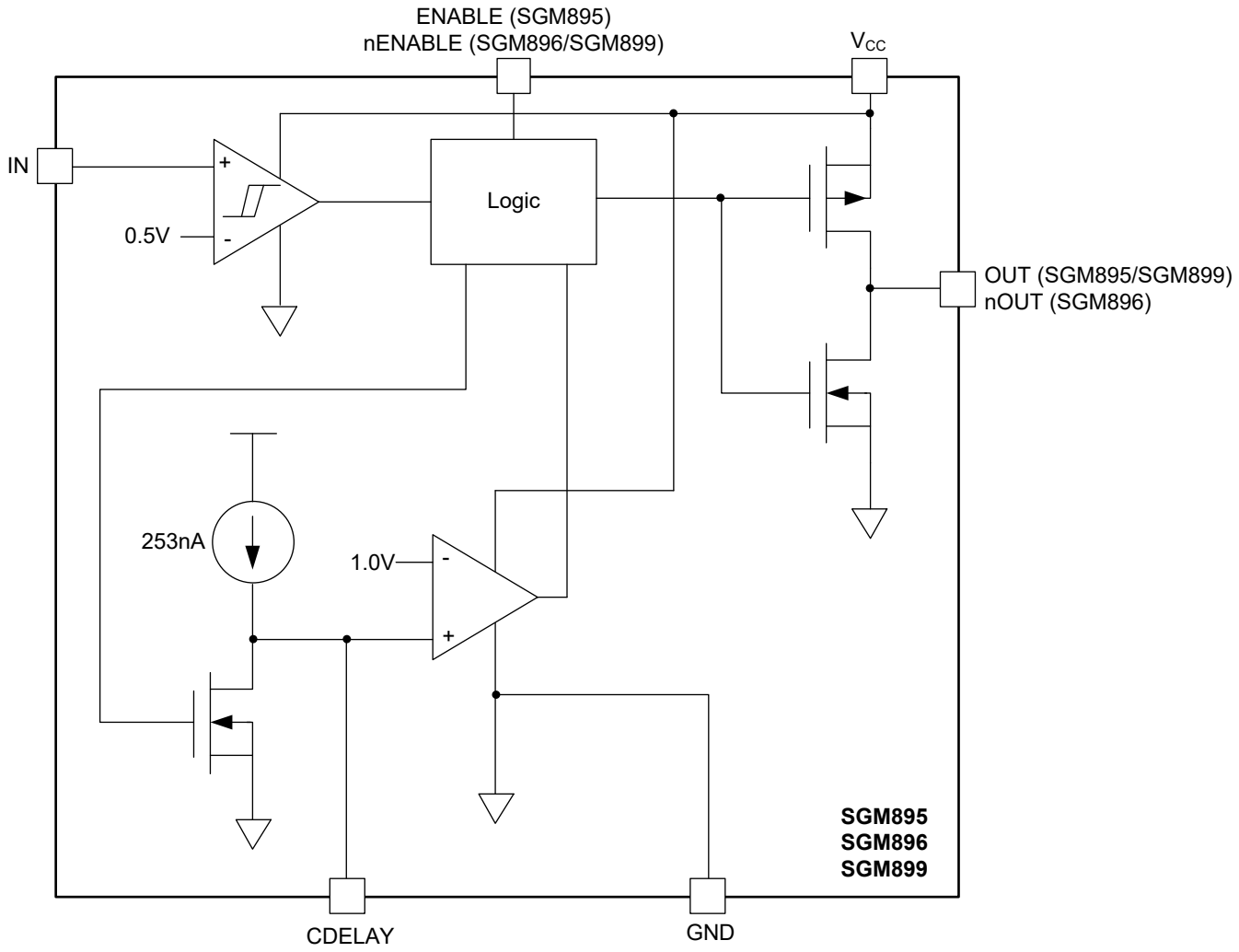


Figure 2. SGM895/SGM896/SGM899 Block Diagram

DETAILED DESCRIPTION

The SGM895/SGM896/SGM897/SGM898/SGM899 are low-power and high-accuracy microprocessor supervisory circuits with adjustable sequencing capability.

When V_{IN} exceeds V_{TH}, the enable input can be used to set the output asserted or deasserted. After the enable input is asserted, the output asserts with the CDELAY adjusted delay period (SGM89_A) or with a 350ns fixed propagation delay (SGM89_P). Table 1, 2, and 3 show the details of the output state depending on the various input and enable conditions.

Table 1. SGM895/SGM897 Output

IN Pin	ENABLE Pin	OUT Pin
$V_{IN} < V_{TH}$	Low	Low
$V_{IN} < V_{TH}$	High	Low
$V_{IN} > V_{TH}$	Low	Low
$V_{IN} > V_{TH}$	High	OUT = V_{CC} (SGM895)
		OUT = high-impedance (SGM897)

Table 2. SGM896/SGM898 Output

IN Pin	nENABLE Pin	nOUT Pin
$V_{IN} < V_{TH}$	Low	nOUT = V_{CC} (SGM896)
		nOUT = high-impedance (SGM898)
$V_{IN} < V_{TH}$	High	nOUT = V_{CC} (SGM896)
		nOUT = high-impedance (SGM898)
$V_{IN} > V_{TH}$	Low	Low
$V_{IN} > V_{TH}$	High	nOUT = V_{CC} (SGM896)
		nOUT = high-impedance (SGM898)

Table 3. SGM899 Output

IN Pin	nENABLE Pin	OUT Pin
$V_{IN} < V_{TH}$	Low	Low
$V_{IN} < V_{TH}$	High	Low
$V_{IN} > V_{TH}$	Low	High
$V_{IN} > V_{TH}$	High	Low

Supply Voltage Input (V_{CC})

The device operates with a supply voltage range of 1.6V to 5.5V. When V_{CC} falls below the UVLO threshold voltage, the output deasserts. However, the output state is not guaranteed when V_{CC} falls below 1.2V. For noisy systems, it is recommended to place a 100nF bypass capacitor close to the V_{CC} pin. For the active-high push-pull output device, connecting a 100kΩ external pull-down resistor to ground ensures the correct logic state for V_{CC} down to 0.

Detection Input (IN)

Connect a resistive divider to IN pin to monitor external voltages (see R_1 and R_2 of the Typical Application Circuit). IN has a rising threshold of V_{TH} = 0.5V and a falling threshold of 0.495V (5mV hysteresis). When V_{IN} exceeds V_{TH} and the enable input is asserted (ENABLE = high or nENABLE = low), OUT goes high (nOUT goes low) after a t_{DELAY} period. When V_{IN} falls below 0.495V, OUT goes low (nOUT goes high) after a 50μs delay. IN has a maximum ±20nA input leakage current, so it is permitted to use larger-value resistors without adding significant error to the resistive divider.

Adjustable Delay (CDELAY)

When V_{IN} > V_{TH} and the enable pin is asserted (ENABLE = high or nENABLE = low), the internal 253nA (TYP) current source begins to charge an external capacitor connected between CDELAY and GND. When the voltage at CDELAY reaches 1V, the output asserts (OUT goes high or nOUT goes low). When the output asserts, C_{CDELAY} is immediately discharged. Adjust the delay time according to the equation:

$$t_{DELAY}\,(ms) = 3.95 \times C_{CDELAY}\,(nF) + 0.048ms \quad (1)$$

where C_{CDELAY} is the external capacitor from CDELAY to GND.

Under the condition of V_{IN} > V_{TH}, the output state depends on the state of ENABLE (nENABLE). For adjustable delay devices (SGM89_A), when ENABLE goes from low to high (nENABLE goes from high to low) the output asserts after a t_{DELAY} period. For propagation delay devices (SGM89_P), there is a 350ns fixed propagation delay from when the enable input is asserted to when the output asserts. Figure 3 through 8 show the timing diagrams of the adjustable and fixed delay devices, respectively.

DETAILED DESCRIPTION (continued)

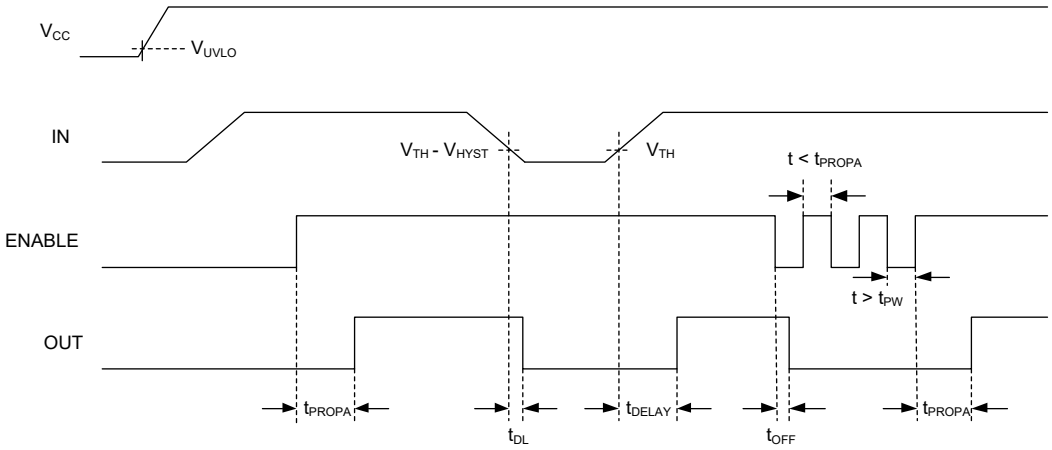


Figure 3. SGM895A/SGM897A Timing Diagram

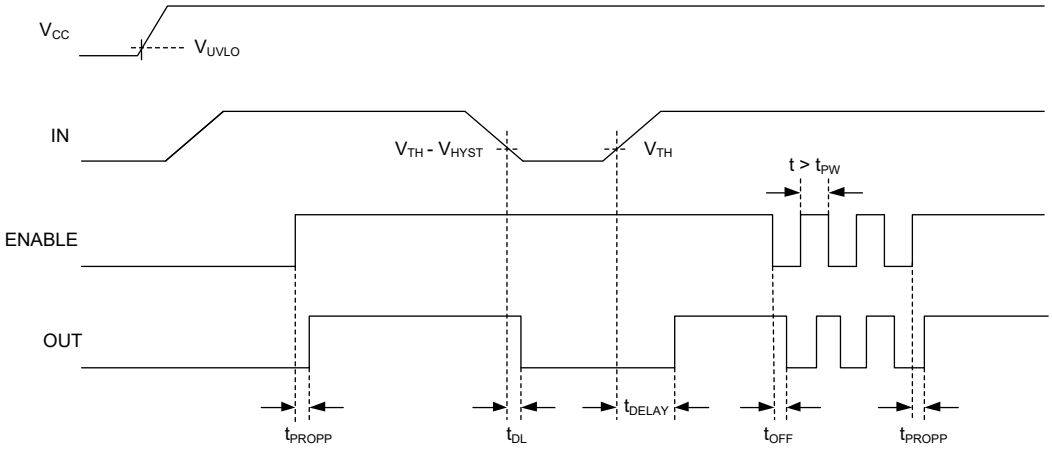


Figure 4. SGM895P/SGM897P Timing Diagram

DETAILED DESCRIPTION (continued)

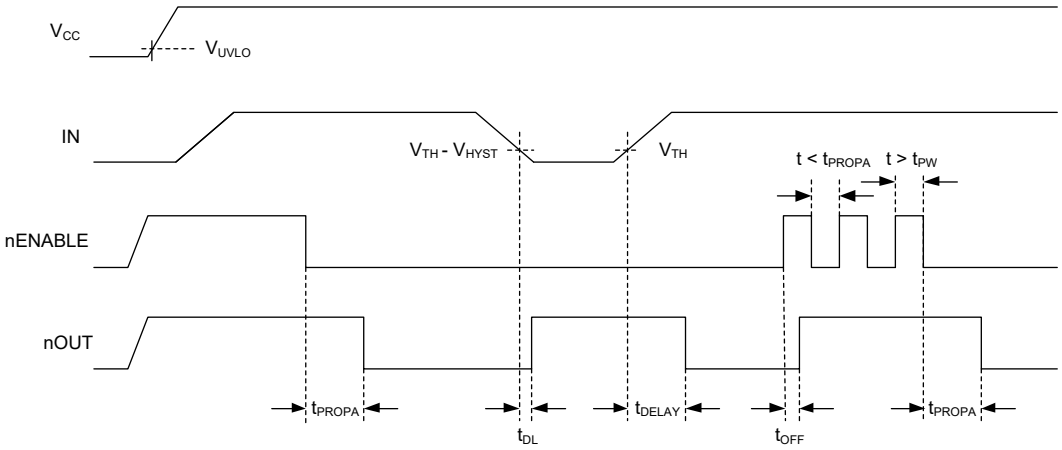


Figure 5. SGM896A/SGM898A Timing Diagram

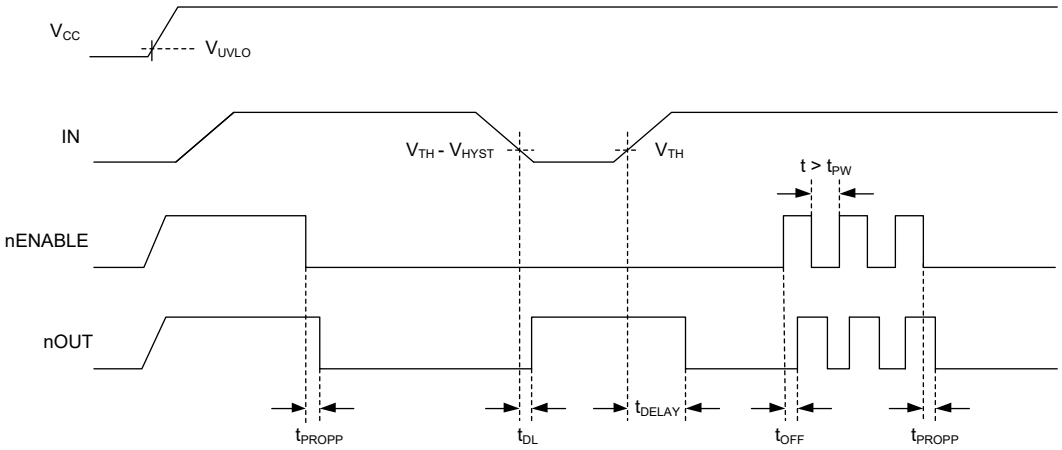


Figure 6. SGM896P/SGM898P Timing Diagram

DETAILED DESCRIPTION (continued)

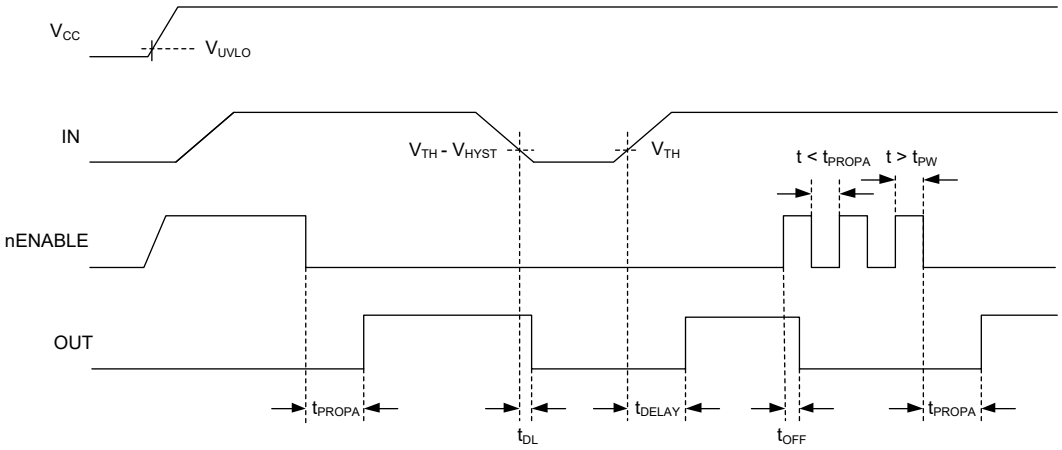


Figure 7. SGM899A Timing Diagram

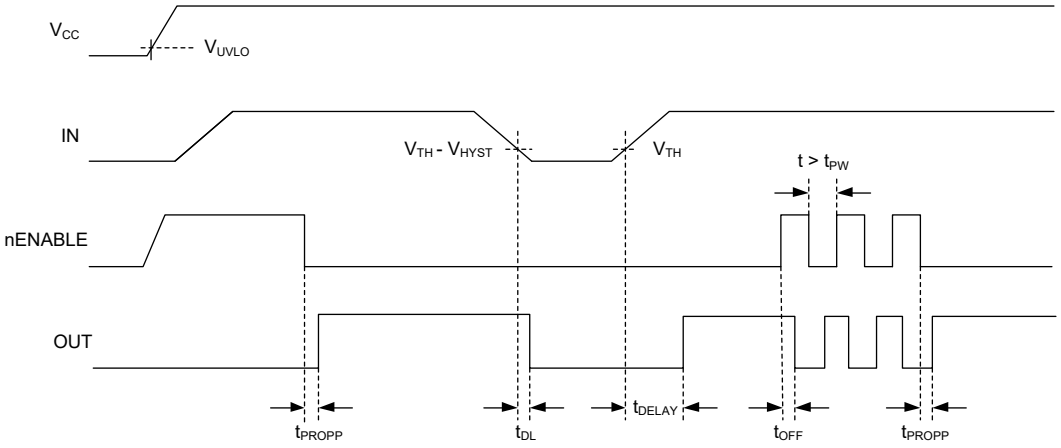


Figure 8. SGM899P Timing Diagram

Enable Input (ENABLE or nENABLE)

The SGM895/SGM897 provide an active-high enable input (ENABLE), while the SGM896/SGM898/SGM899 provide an active-low enable input (nENABLE). When V_{IN} > V_{TH}, SGM89_A provide an adjustable delay period from when ENABLE is asserted to when the output asserts, while SGM89_P provide a fixed propagation delay time.

The enable input offers logic-high threshold of 1.4V and logic-low threshold of 0.4V. When V_{IN} > 0.5V, set ENABLE low (nENABLE high) to force OUT low (nOUT high) within t_{PROPP}.

Output (OUT or nOUT)

The SGM895/SGM899 offer an active-high push-pull output (OUT), while the SGM896 offers an active-low push-pull output (nOUT). The SGM897 offers an active-high open-drain output (OUT), while the SGM898 offers an active-low open-drain output (nOUT).

The push-pull output devices are referenced to V_{CC}. The open-drain outputs can be pulled up to 28V.

APPLICATION INFORMATION

Input Threshold

The SGM895/SGM896/SGM897/SGM898/SGM899 detect the voltage on IN through an external resistive divider (see R_1 and R_2 in the Typical Application Circuit). Connect R_1 and R_2 as close to IN as possible to avoid the environment noise. The resistor values of R_1 and R_2 can be very high to minimize current consumption due to low IN leakage current. For example, set R_2 to 1MΩ and calculate R_1 based on the desired detection voltage by the following equation:

$$R_1 = R_2 \times \left[\frac{V_{MONITOR}}{V_{TH}} - 1 \right] \quad (2)$$

where $V_{MONITOR}$ is the desired detection voltage and V_{TH} is the detector input threshold (0.5V).

Pull-Up Resistor Values (SGM897/SGM898)

The exact pull-up resistor values for the open-drain outputs are not critical, however, proper logic levels should be ensured. For example, if V_{CC} = 2.25V and the pull-up voltage is 28V, users should keep the sink current less than 0.5mA as shown in the Electrical Characteristics Table. As a result, the pull-up resistor should be greater than 56kΩ. For a 12V pull-up, the resistor should be larger than 24kΩ. Note that the ability to sink current is dependent on the V_{CC} supply voltage.

Typical Application Circuits

Figure 9, 10 and 11 show typical applications for the SGM895/SGM896/SGM897/SGM898/SGM899. Figure 9 shows that the SGM897 is used as an over-voltage protection circuit by a P-channel MOSFET. Figure 10 shows that the SGM895 is used as a low-voltage sequencing circuit by an N-channel MOSFET. Finally, Figure 11 shows that the SGM895 is used in a multiple-output sequencing application.

Using an N-Channel Device for Sequencing

In higher power applications, the power loss of N-channel MOSFET can be reduced due to its lower on-resistance. However, it requires a sufficient positive V_{GS} voltage to fully turn on. The application in Figure 10 shows the SGM895 in a switch sequencing application using an N-channel MOSFET.

Similarly, if a higher voltage is present in the system, the open-drain version can be used in the same manner.

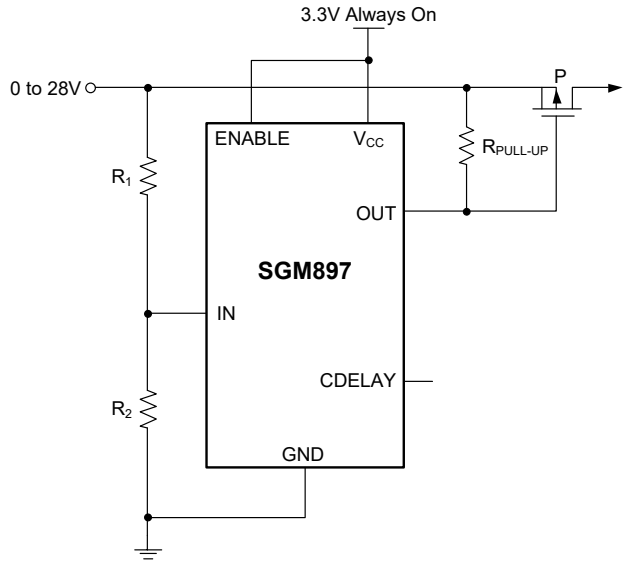


Figure 9. Over-Voltage Protection

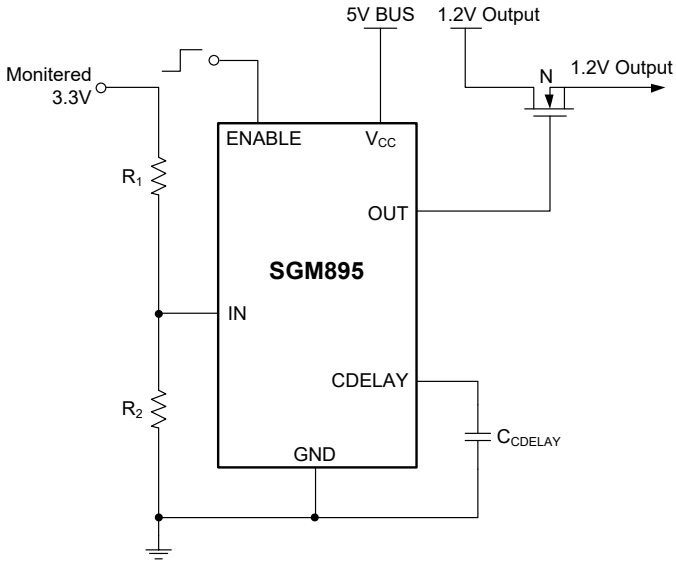


Figure 10. Low-Voltage Sequencing Using an N-Channel MOSFET

APPLICATION INFORMATION (continued)

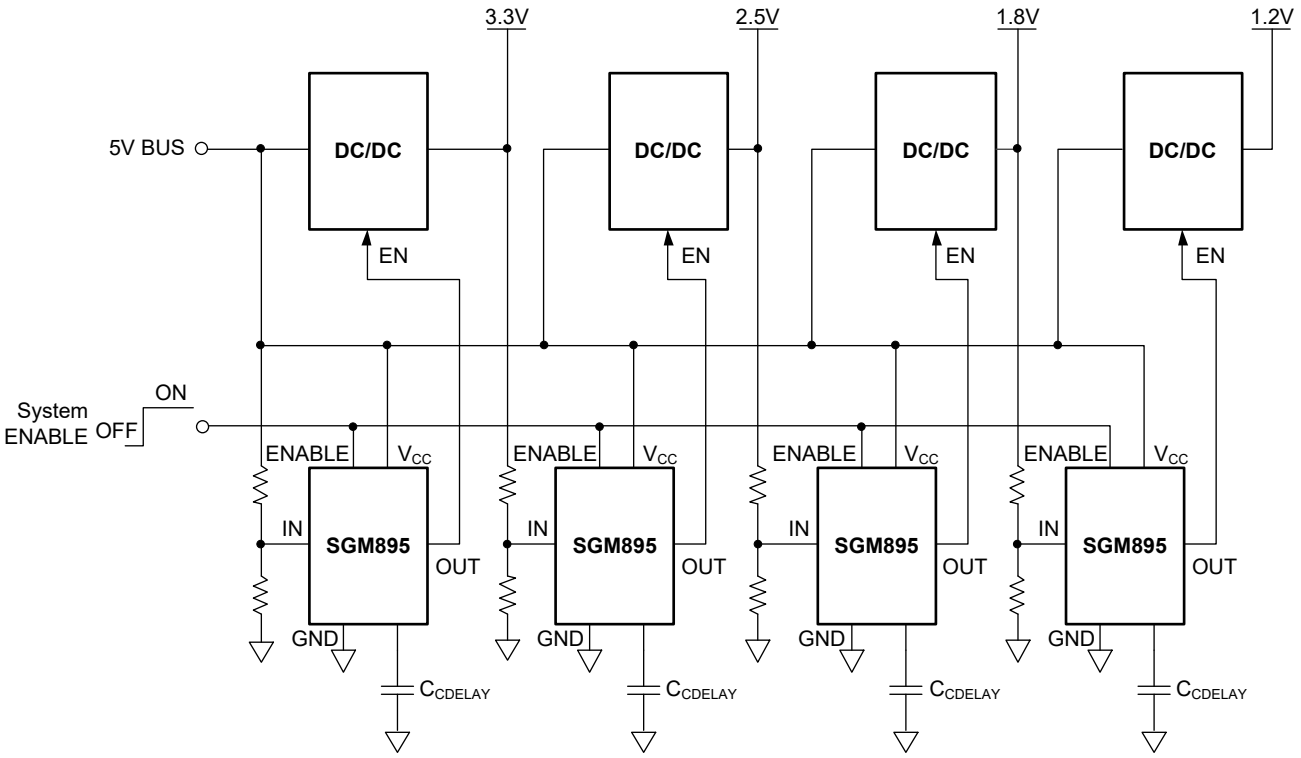
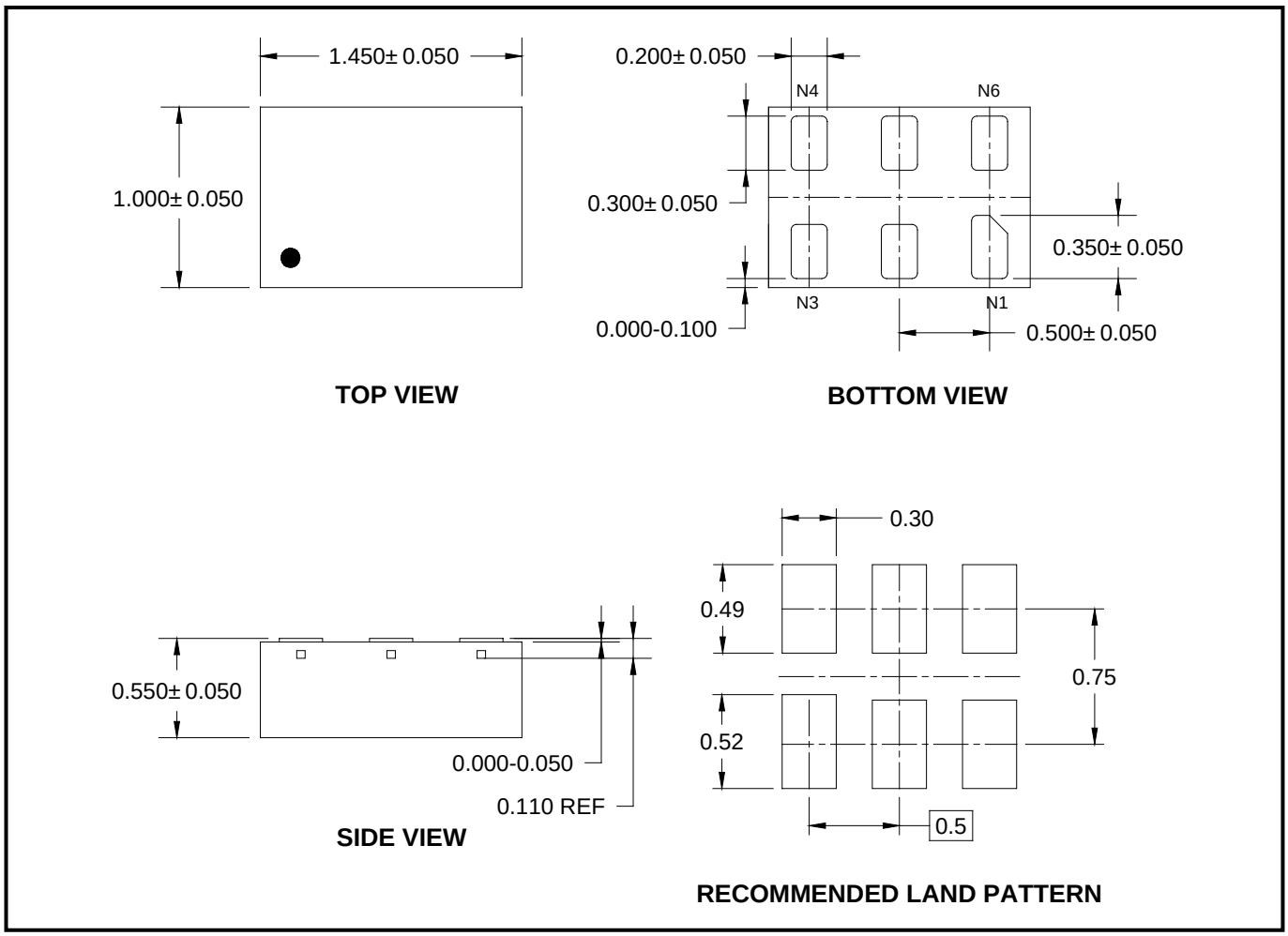


Figure 11. Multiple-Output Sequencing

PACKAGE OUTLINE DIMENSIONS

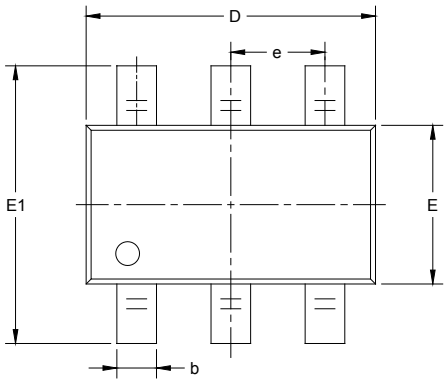
UTDFN-1.45×1-6AL

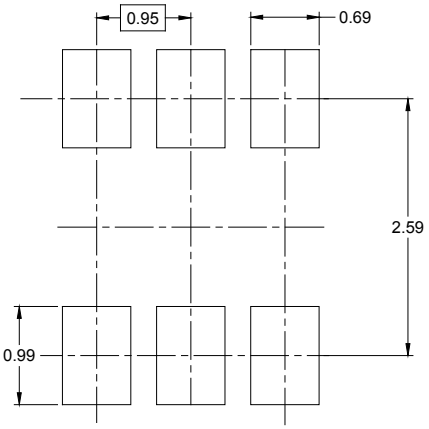


NOTE: All linear dimensions are in millimeters.

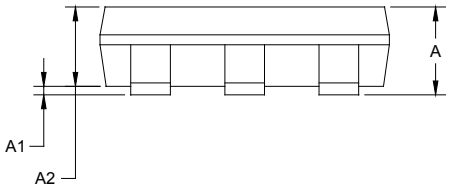
PACKAGE OUTLINE DIMENSIONS

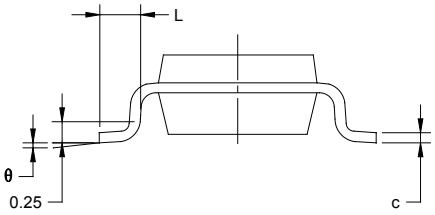
TSOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)

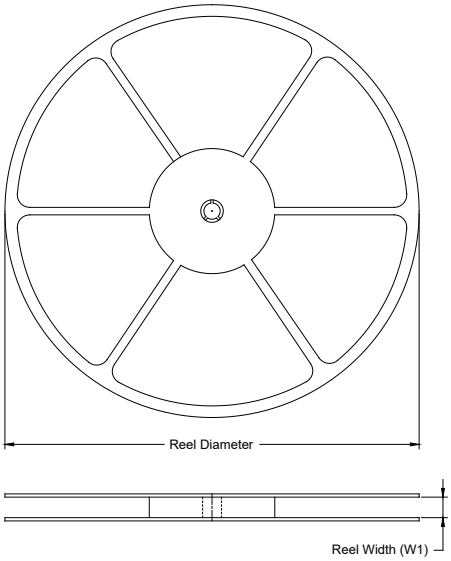




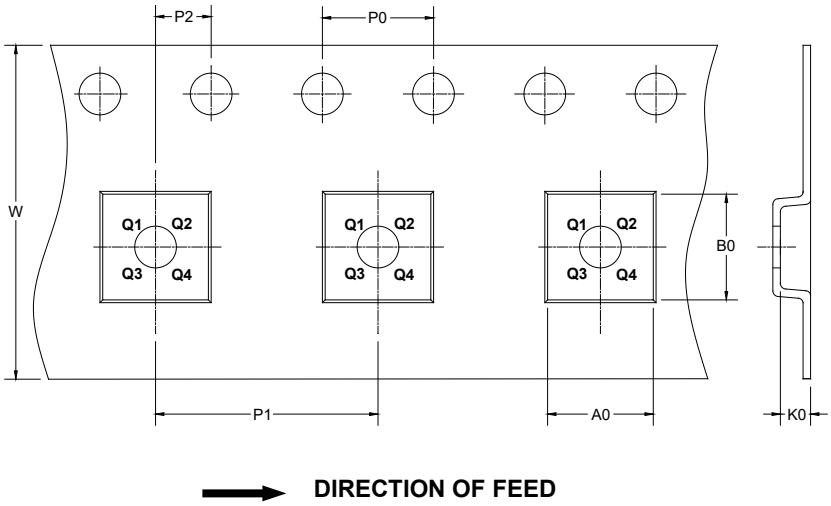
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.000		0.043
A1	0.000	0.100	0.000	0.004
A2	0.700	0.900	0.028	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.200	0.003	0.008
D	2.850	2.950	0.112	0.116
E	1.550	1.650	0.061	0.065
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

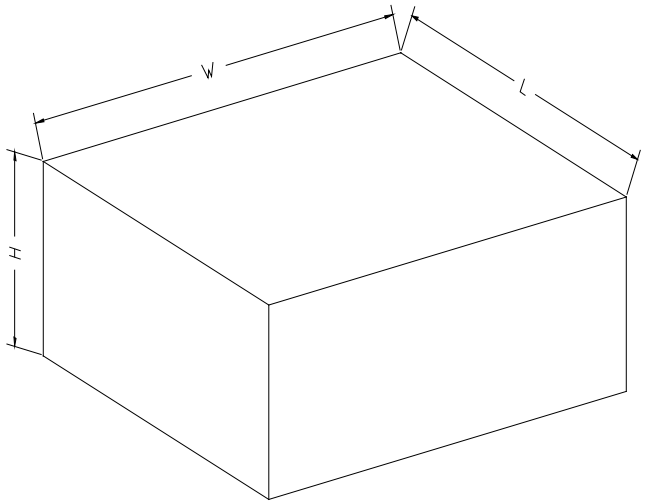
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.45×1-6AL	7″	9.5	1.15	1.60	0.75	4.0	4.0	2.0	8.0	Q1
TSOT-23-6	7″	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002