Dual Ultra-Low On-Resistance Load Switch with Controlled Turn-On

Features

- **Integrated Dual Channel Load Switch**
- **Input Voltage Range: 0.8V to 5.5V**
- **Dual Ultra-low ON-Resistance (16mΩ)**
  - **$R_{DS(on)}$ = 17mΩ at V_{IN} = 5V (V_{BIAS} = 5V)**
  - **$R_{DS(on)}$ = 16mΩ at V_{IN} = 3.6V (V_{BIAS} = 5V)**
  - **$R_{DS(on)}$ = 16mΩ at V_{IN} = 1.8V (V_{BIAS} = 5V)**
  - **$R_{DS(on)}$ = 15mΩ at V_{IN} = 0.8V (V_{BIAS} = 5V)**
- **6A Continuous Switch Current per channel**
- **Low Quiescent Current**
  - **65μA (Both Channel)**
  - **55μA (Single Channel)**
- **Low Threshold Control Inputs**
- **Adjustable Slew-rate Control**
- **Quick Output Discharge Transistor**
- **14 Pin TDFN Package with Thermal Pad**

General Description

The G2898 is dual N-channel MOSFET power switch designed for high-side load-switching application. The device has a typical $R_{DS(ON)}$ of 16mΩ and the output current is limited to 6A. Each channel is controlled by an on/off input (EN1, EN2) independently, which is suitable for interfacing directly with low-voltage I/O ports.

In the G2898, a 220Ω on-chip load resistor is added for quick output discharge (QOD) when the switch is turned off. Moreover, the controlled rise time can be adjusted by using a ceramic capacitor on the CTx pins in order to prevent in-rush current at start-up time.

The G2898 is available in 14 pin TDFN package.

Applications

- **Notebooks / Netbooks**
- **Tablet PCs**
- **Consumer Electronics**
- **Set-Top-Boxes**
- **Industrial Systems**
- **Telecom Systems**

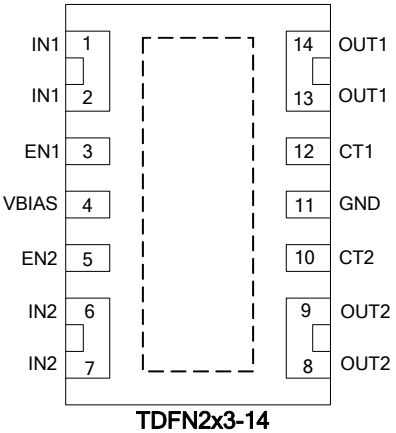
Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2898KD1U	2898	-40°C to 85°C	TDFN2X3-14

Note: KD: TDFN2X3-14
1: Bonding Code
U: Tape & Reel
Green : Lead Free / Halogen Free.

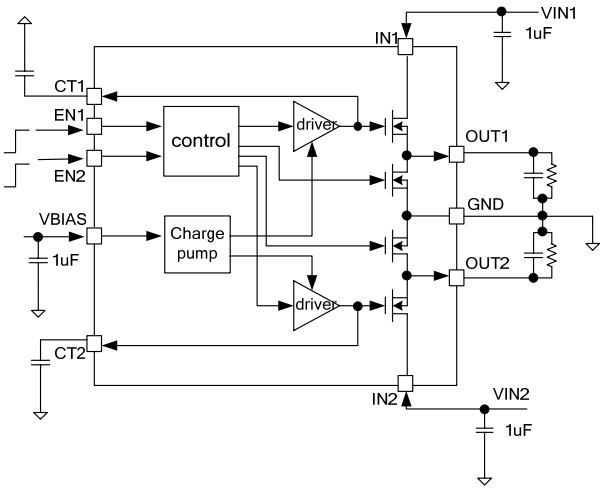
G2898

Pin Configuration



TDFN2x3-14

Typical Application Circuit



Absolute Maximum Ratings

V_{IN1} ,$V_{IN2}$to GND . . . . . -0.3V to +6V
EN1,EN2 to GND . . . . . .-0.3V to +6V
V_{OUT1} , $V_{OUT1}$to GND . . . . . -0.3V to +6V
CT1,CT2 to GND . . . . . .-0.3V to +12V
V_{BIAS} to GND . . . . . -0.3V to +6V
Continuous Switch Current (I_{MAX}). 6A
Junction Temperature . . . . . .150°C
Thermal Resistance Junction to Ambient, (θ_{JA})*
TDFN2X3-14 . . . . . .68.9°C/W

Continuous Power Dissipation (T_A = +25°C)*
TDFN2X3-14 . . . . . .1.9W
Thermal Resistance Junction to Case, (θ_{JC})
TDFN2X3-14 . . . . . .45°C/W
Operating Temperature Range . . . . . -40°C to 85°C
Storage Temperature Range . . . . . .-65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . .260°C
ESD(HBM) . . . . . .2KV(1)
ESD(MM) 200V

*Please refer to Minimum Footprint PCB Layout Section
Note 1：Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS
VIN1,2 Input voltage range	0.8	V_{BIAS}	V
VBIAS Bias voltage range	2.5	5.6	V
EN1,2 ON voltage range	0	5.5	V
VOUT1,2 Output voltage range	---	VIN1,2	V
VIH High-level input voltage, EN1, EN2	1.2	5.5	V
VIL Low-level input voltage, EN1, EN2		0.5	V
CIN1,2 Input Capacitor	1*	---	µF

*Note: 1-uF input capacitor is sufficient in most application cases. If the distance of power trace on PCB is longer than general design, larger input capacitor is highly recommended for normal operation.

Electrical Characteristics

(V_{IN1} = 0.8V to 5.5V, V_{IN2} = 0.8V to 5.5V, V_{BIAS}= 5V, T_A = –40ºC to 85ºC (unless otherwise noted)

PARAMETER	SYMBOL	Conditions		T_A	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}				0.8	---	V_{BIAS}	V
Bias Voltage Range	V_{BIAS}				2.5	---	5.6	V
Bias Current	I_{BIAS}	IOUT1 = IOUT2 = 0, VIN1 = VIN2 =5V EN1 =EN2=V_{BIAS}=5V		Full	---	65	80	µA
		IOUT1 = IOUT2 = 0, VIN1 = VIN2 =5V EN1 = V_{BIAS} = 5V, EN2 = 0V		Full	---	53	---	µA
		IOUT1 = IOUT2 = 0, VIN1 = VIN2 =2.5V EN1 =EN2=V_{BIAS}=2.5V		Full	---	40	48	µA
		IOUT1 = IOUT2 = 0, VIN1 = VIN2 =2.5V EN1 = V_{BIAS} = 2.5V, EN2 = 0V		Full	---	33	---	µA
Shutdown Bias Current	I_{SHDN}	ENx = GND, VOUTx = 0V		Full	---	---	1	µA
Off-state Supply Current	I_{IN_OFF}	ENx = GND, VOUTx = 0V, VINx= 0.8 to 5V		Full	---	0.5	8	µA
EN pin Input leakage Current	I_{EN_LEAK}	EN=5.5V		Full	---	---	1	µA
On -Resistance	$R_{DS(on)}$	Enx = VBIAS, IOUTx = -200mA VBIAS = 5V,	VINx=5V	25 ºC	---	17	23	mΩ
				Full	---	---	27	
			VINx=3.6V	25 ºC	---	16	23	
				Full	---	---	27	
			VINx=1.8V	25 ºC	---	16	23	
				Full	---	---	27	
			VINx=0.8V	25 ºC	---	15	23	
				Full	---	---	27	

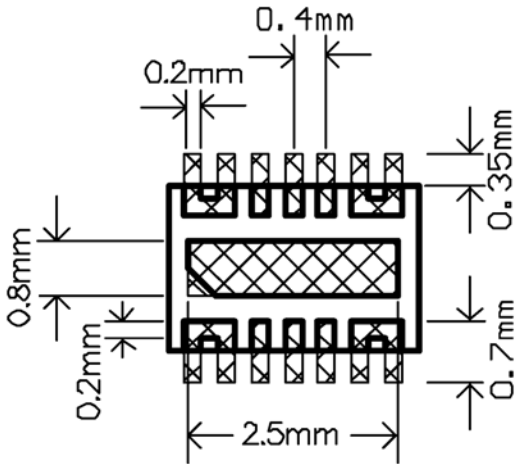
Electrical Characteristics (Continued)

(V_{IN1} = 0.8V to 5.5V, V_{IN2} = 0.8V to 5.5V, V_{BIAS}= 5V, T_A = –40ºC to 85ºC (unless otherwise noted)

PARAMETER	SYMBOL	Conditions		T_A	MIN	TYP	MAX	UNITS
On -Resistance	$R_{DS(on)}$	Enx =VBIAS, IOUTx = -200mA VBIAS = 2.5V,	VINx=2.5V	25 ºC	---	18	25	mΩ
				Full	---	---	30	
			VINx=1.8V	25 ºC	---	17	25	
				Full	---	---	30	
			VINx=1.2V	25 ºC	---	16	25	
				Full	---	---	30	
			VINx=0.8V	25 ºC	---	15	25	
				Full	---	---	30	
Discharge Resistance	R_{DIS}	VINx = 5.0V,ENx = 0V, IOUTx = 1mA		Full	---	250	450	Ω
High level input voltage on EN pin	VIH				1.2	--	5.5	V
Low level input voltage on EN pin	VIL				---	0	0.5	V
Over Temperature Threshold	OT				---	155	---	ºC

Minimum Footprint PCB Layout Section

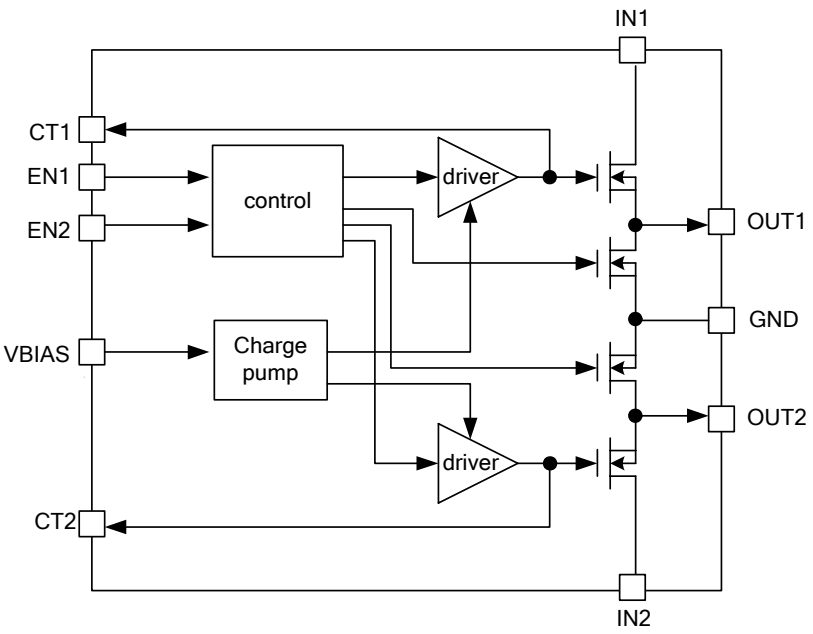
TDFN2X3-14



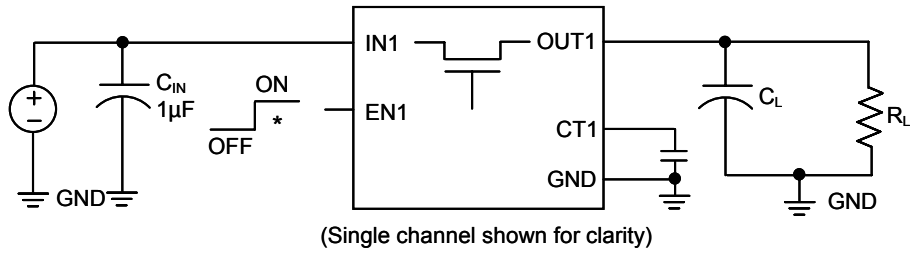
Pin Description

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	IN1	I	Switch1 Input
2	IN1	I	Switch1 Input
3	EN1	I	Switch 1 Control Input
4	VBIAS	I	Input Bias Supply
5	EN2	I	Switch 2 Control Input
6	IN2	I	Switch 2 Input
7	IN2	I	Switch 2 Input
8	OUT2	O	Switch 2 Output
9	OUT2	O	Switch 2 Output
10	CT2	O	Switch2 Ramp capacitor input
11	GND	-	Ground
12	CT1	O	Switch 1 Ramp capacitor input
13	OUT1	O	Switch 1 Output
14	OUT1	O	Switch 1 Output
15	Thermal Pad	O	Exposed Pad to alleviate thermal stress. Solder to GND in PCB layout.

Block Diagram

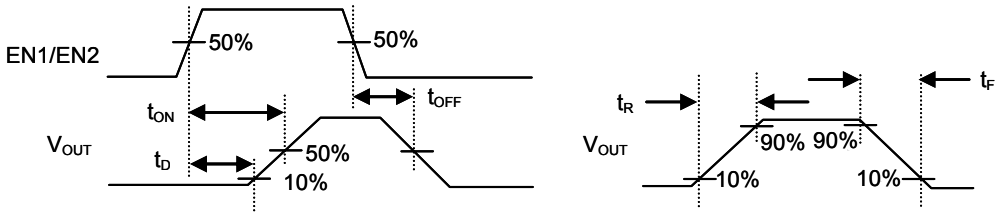


Parametric Measurement Information



(Single channel shown for clarity)

Test Circuit



t_{ON} / t_{OFF} WAVEFORMS

*. Rising and falling time of control signal EN1,EN2 is 100ns

Figure 1. Test Circuit and t_{ON} / t_{OFF} Waveforms

SWITCHING CHARATERISTICS

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}=V_{EN}=V_{BIAS}=5V, T_A=25ºC (unless otherwise noted)					
t_{ON}	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	1210	---	µs
t_{OFF}	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	1	---	
t_R	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	1600	---	
t_F	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	2	---	
t_D	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	410	---	
V_{IN}=0.8V, V_{EN}=V_{BIAS}=5V, T_A=25ºC (unless otherwise noted)					
t_{ON}	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	440	---	µs
t_{OFF}	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	1	---	
t_R	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	315	---	
t_F	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	3	---	
t_D	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	280	---	
V_{IN}=2.5V, V_{EN}=5V, V_{BIAS}=2.5V, T_A=25ºC (unless otherwise noted)					
t_{ON}	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	790	---	µs
t_{OFF}	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	2	---	
t_R	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	870	---	
t_F	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	3	---	
t_D	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	360	---	
V_{IN}=0.8V, V_{EN}=5V, V_{BIAS}=2.5V, T_A=25ºC (unless otherwise noted)					
t_{ON}	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	460	---	µs
t_{OFF}	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	2	---	
t_R	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	330	---	
t_F	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	3	---	
t_D	R_L=10Ω, C_L=0.1µF, C_T=1000pF	---	300	---	

Application Information

V_{IN} and V_{BIAS} voltage range

For optimal $R_{DS(on)}$ performance, make sure $V_{IN} \leqq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit $R_{DS(on)}$ greater than what is listed in the Electrical characteristics table. See Figure below for an example for a typical device. Notice the increasing $R_{DS(on)}$ as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

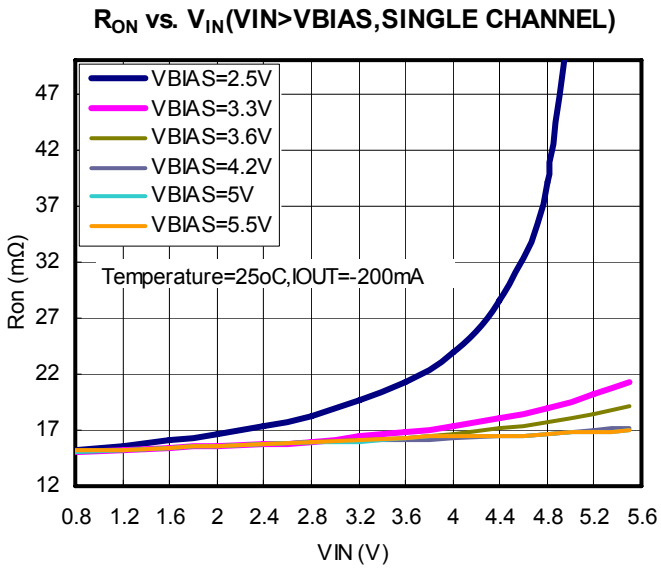


Figure 2. $R_{DS(on)}$ vs. V_{IN} (V_{IN}>V_{BIAS} Single Channel)

Adjustable rise time

A capacitor to GND on the CT pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25V should be used on the CT pin. An approximate formula for the relationship between CT and slew rate is (the equation below accounts for 10% to 90% measurement on VOUT and does NOT apply for CT = 0pF. Use table below to determine rise times for when CT=0pF):

$$SR = 0.37 \times CT + 17.8$$

Where,

SR = slew rate (in µs/V)

CT = the capacitor value on the CT pin (in pF)

The units for the constant 17.8 is in µs/V.

Rise time can be calculated by multiplying the input voltage by the slew rate. The table below contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition and the EN pin is asserted high.

CTx(pF)	Rise time (µs) 10% - 90%, C_L=0.1µF, C_{IN}=1µF, R_L=10Ω Typical values at 25ºC, V_{BIAS}=5V						
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	0.8V
0	99	72	50	44	39	36	32
220	496	338	198	170	142	128	103
470	920	616	348	298	246	220	177
1000	1708	1148	658	556	456	408	328
2200	4250	2770	1550	1290	1052	940	736
4700	8520	5680	3160	2650	2160	1910	1520
10000	18400	12280	6860	5760	4700	4230	3360

Application Information

Input capacitor (optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharge load capacitor or short-circuit, a capacitor need to be placed between V_{IN} and GND. A 1μF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

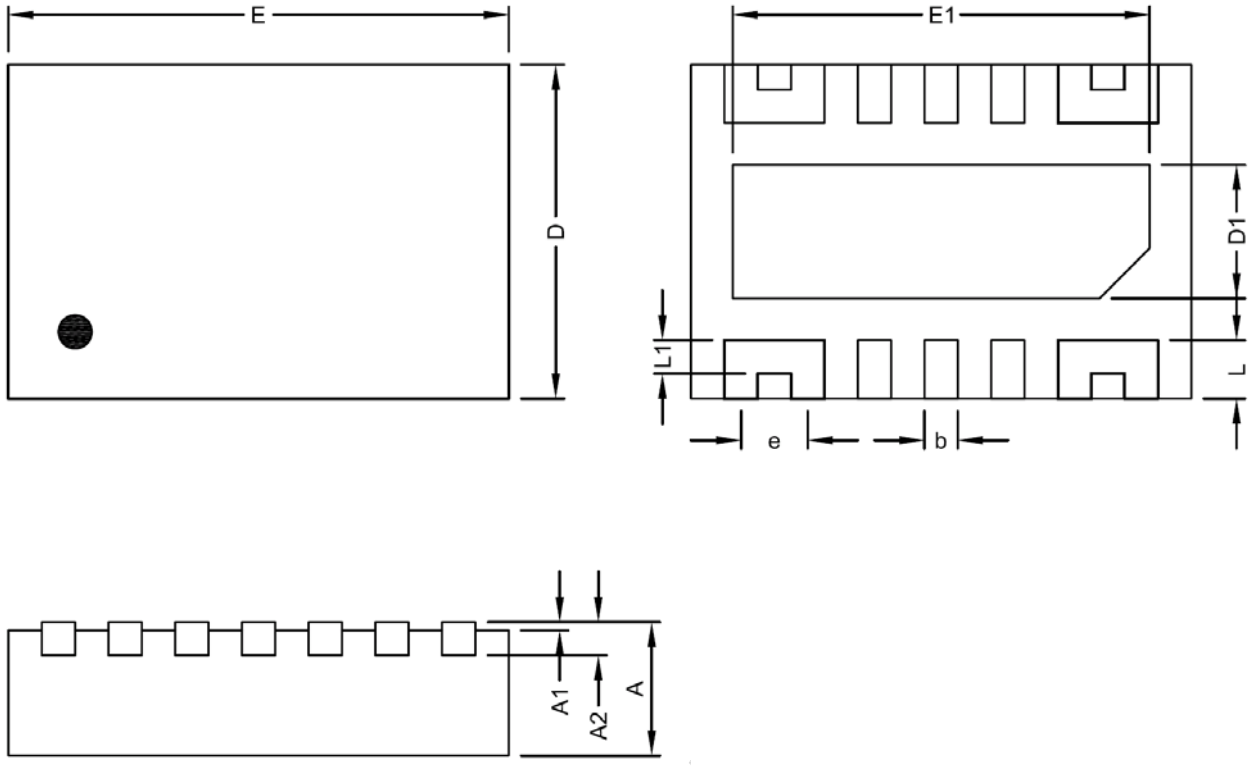
Output capacitor (optional)

Due to the integrated body diode in the NMOS switch, a CIN greater than CL is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance in not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time.

PCB Layout Guidelines

1. To have lower voltage drop in field application, short and wide PCB trace is recommended. The IN/OUT pins are located in corner of IC. It is beneficial to route a wide and short PCB trace.
2. To absorb voltage bounce that is caused by parasitic inductor of PCB trace at quick load transient, placing Cin /Cout close to IN/OUT pin of IC is recommended.
3. The wide trace of Vin/VOUT and GND can help minimize the parasitic electrical effects and the case to ambient thermal impedance. Using thermal vias located under the exposed thermal pad helps thermal dissipation of the device

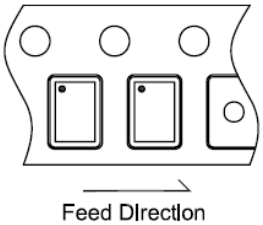
Package Information



TDFN2X3-14 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	2.95	3.00	3.05	0.1161	0.1181	0.1201
D1	0.75	0.85	0.95	0.0295	0.0335	0.0374
E1	2.45	2.50	2.55	0.0965	0.0984	0.1004
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.30	0.35	0.40	0.0118	0.0138	0.0157
L1	0.20 BSC			0.0079 BSC		

Taping Specification



PACKAGE	Q'TY/BY REEL
TDFN2X3-14	3,000 ea