100mΩ, 2A Slew Rate Controlled Load Switch

General Description

The RT9724 is a cost-effective, low-voltage, single N-MOSFET high-side Power Switch IC. Low switch-on resistance (typ. 100mΩ) and low supply current (typ. 50uA) are realized in this IC. The RT9724 integrates an over-current protection circuit, a short fold back circuit, a thermal shutdown circuit and an under-voltage lockout circuit for overall protection. Besides, a slew rate controlled function is embedded for turn-on rising time control. The RT9724 is available in SOT-23-5 and WDFN-8L 2x2 package.

Ordering Information

RT9724 □□

- Package Type
  - B : SOT-23-5
  - QW : WDFN-8L 2x2 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

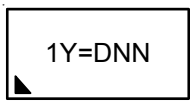
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT9724GB



1Y= : Product Code

DNN : Date Code

RT9724GQW

GV : Product Code

W : Date Code

Features

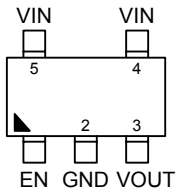
- **100mΩ (typ.) N-MOSFET Switch**
- **Operating Range : 2.7V to 5.5V**
- **Reverse Blocking Current**
- **Under Voltage Lockout**
- **Thermal Protection with Foldback**
- **Over Current Protection**
- **Short Circuit Protection**
- **Slew Rate Limited Turn-On Time 3ms (5V)**
- **RoHS Compliant and Halogen Free**

Applications

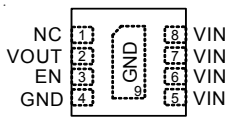
- Cellular Phones
- Digital still Camera
- Hot swap Supplies
- Notebook Computers
- Personal Communication Devices
- Personal Digital Assistants

Pin Configurations

(TOP VIEW)

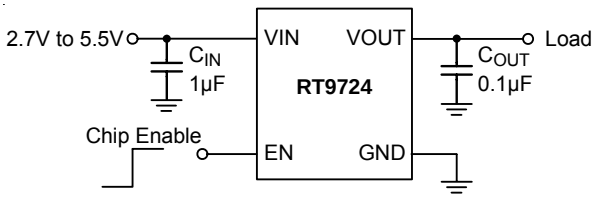


SOT-23-5



WDFN-8L 2x2

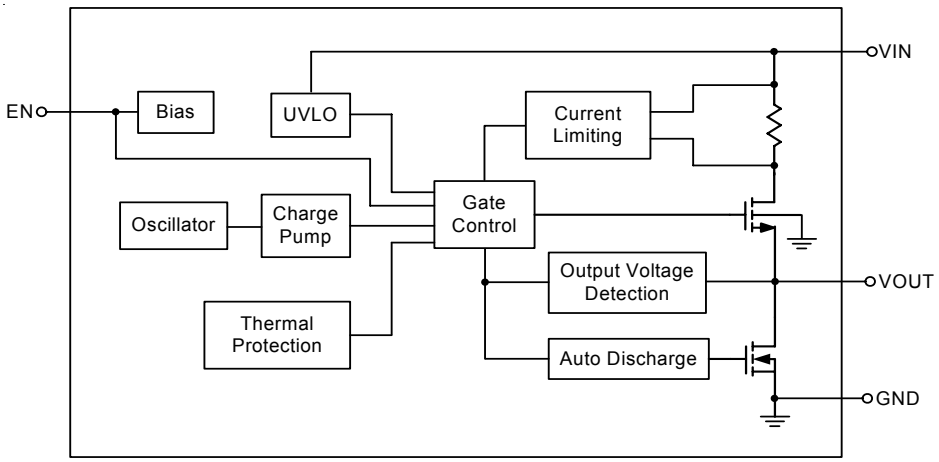
Typical Application Circuit



Functional Pin Description

Pin No.		Pin Name	Pin Function
SOT-23-5	WDFN-8L 2x2		
1	3	EN	Chip Enable (Active High).
2	4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	2	VOUT	Power-Switch Output.
4, 5	5, 6, 7, 8	VIN	Power Input Voltage.
--	1	NC	No Internal Connection.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- 6V
- Enable Input Voltage, EN ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-5 ---------- 0.458W
  WDFN-8L 2x2 ---------- 0.833W
- Package Thermal Resistance (Note 2)
  SOT-23-5, θ_{JA} ---------- 218.1°C/W
  WDFN-8L 2x2, θ_{JA} ---------- 120°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 4kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 2.7V to 5.5V
- Enable Input Voltage, EN ---------- 0V to 5.5V
- Junction Temperature Range ---------- –40°C to 100°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, C_{IN} = 1µF, C_{OUT} = 0.1µF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage		V_{IN}		2.7	--	5	V
Under Voltage Lookout		V_{UVLO}	V_{IN} Falling	1.3	1.7	2.1	V
Under Voltage Lockout Hysteresis		ΔV_{UVLO}		--	50	--	mV
Quiescent Current		I_Q	EN = High	--	50	70	µA
Off Supply Current		I_{SHDN}	EN = Low, V_{OUT} = Open	--	--	1	µA
Off Switch Current		$I_{LEAKAGE}$	EN = Low, V_{OUT} = 0	--	--	1	µA
On-Resistance		$R_{DS(ON)}$	V_{IN} = 3.3V, I_{OUT} = 1.3 A	--	100	120	mΩ
Current Limiting		I_{LIM}	V_{IN} = 3.3V, V_{OUT} = 2.3V	1.5	2	2.5	A
Short Circuit Current		I_{SC_FB}	V_{OUT} = 0V, Measured Prior to Thermal Shutdown	0.4	0.8	1.5	A
Thermal shutdown Threshold		T_{SD}	V_{OUT} > 1V	--	130	--	°C
			V_{OUT} = 0V	--	100	--	°C
Hysteresis				--	20	--	°C
EN Threshold Voltage	Logic-Low	V_{IL}	V_{IN} = 2.7V to 5.5V	--	--	0.8	V
	Logic-High	V_{IH}	V_{IN} = 2.7V to 5.5V	2	--	--	V
Enable Input Leakage		I_{EN}	V_{EN} = 5.5V	--	--	1	µA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Turn-On Delay Time	T_{D_ON}	V_{IN} = 5V, R_{LOAD} = 10Ω	--	60	100	μs
Output Turn-On Rise Time	T_{ON}	V_{IN} = 5V, R_{LOAD} = 10Ω	1	3	--	ms
Output Turn-Off Delay Time	T_{D_OFF}	V_{IN} = 5V, R_{LOAD} = 10Ω	--	4	10	μs
Output Pull-Down Resistance During OFF	$R_{DISCHARGE}$	EN = Low	--	150	--	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

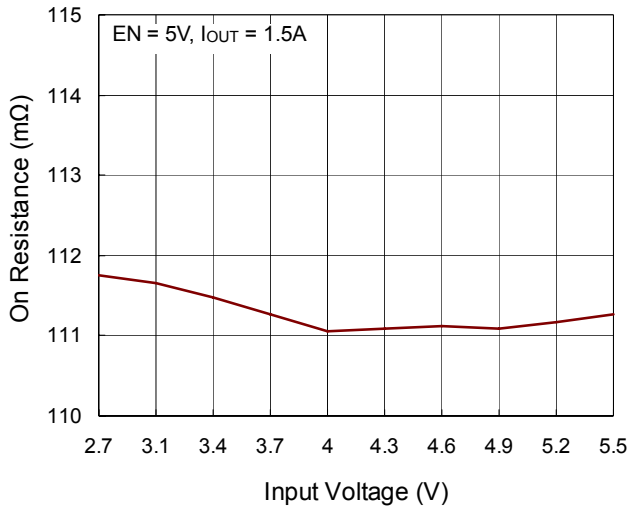
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

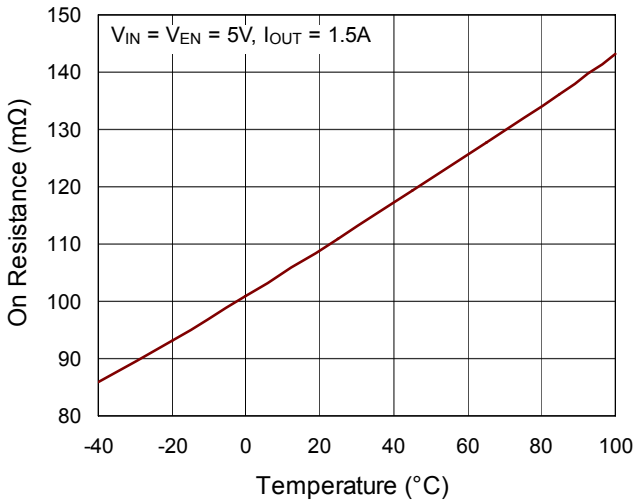
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

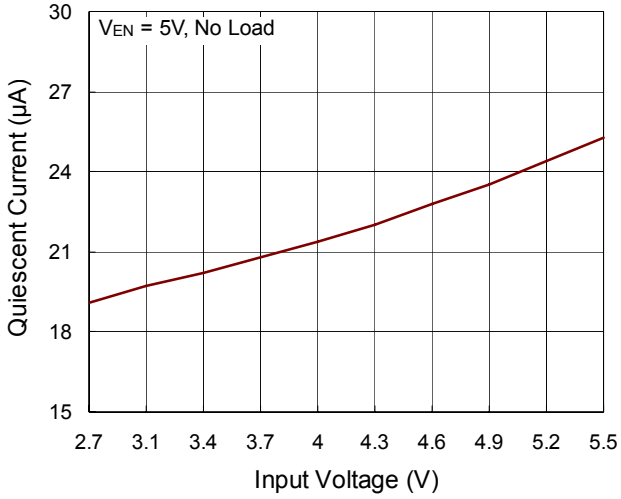
On Resistance vs. Input Voltage



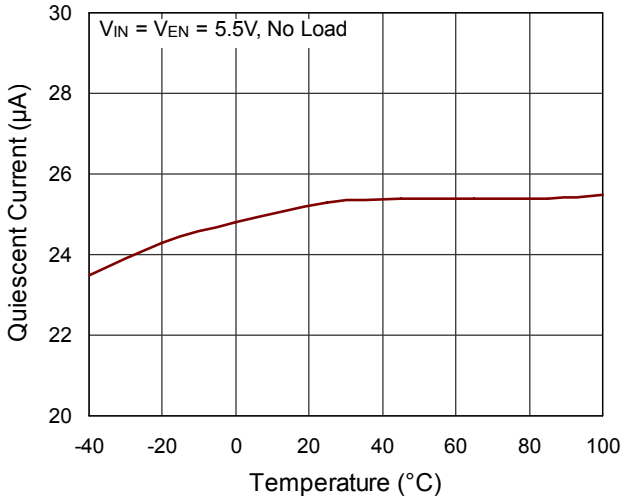
On Resistance vs. Temperature



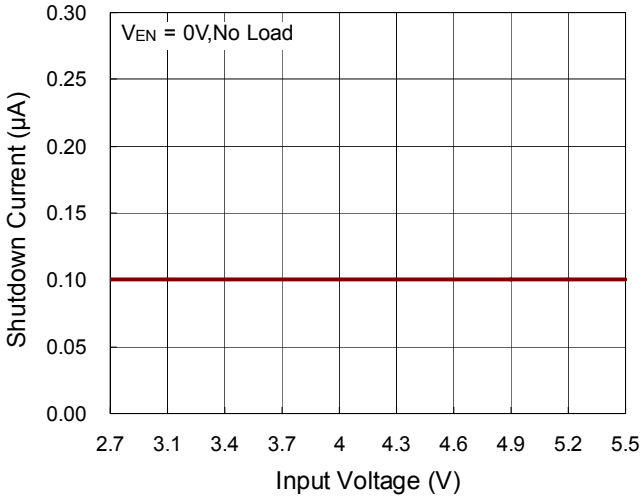
Quiescent Current vs. Input Voltage



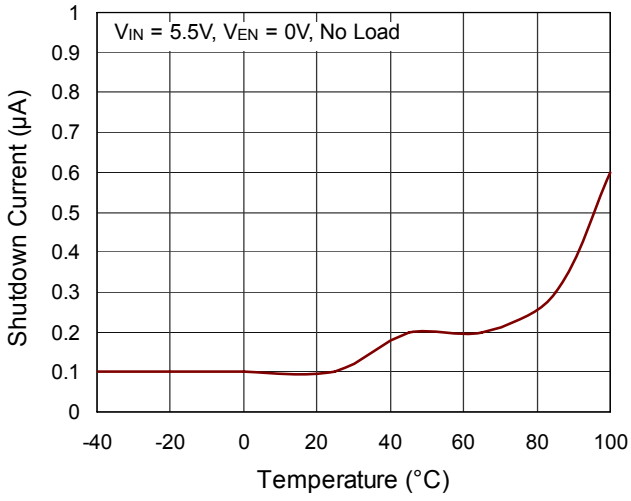
Quiescent Current vs. Temperature



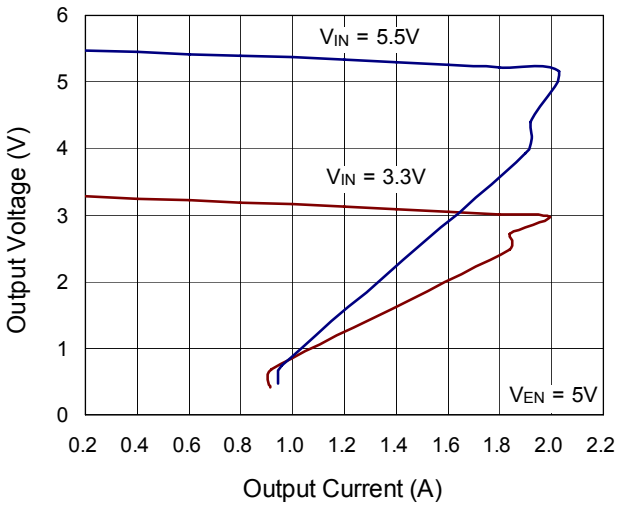
Shutdown Current vs. Input Voltage



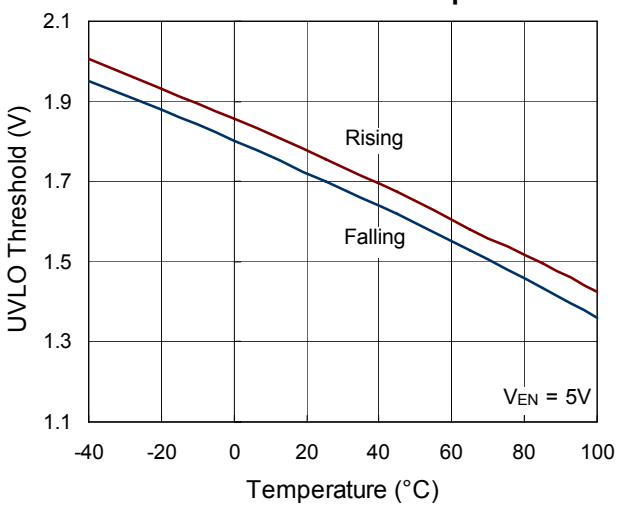
Shutdown Current vs. Temperature



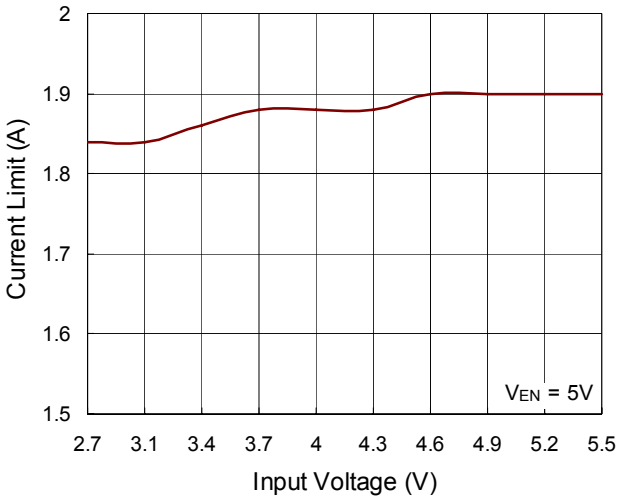
Output Voltage vs. Output Current



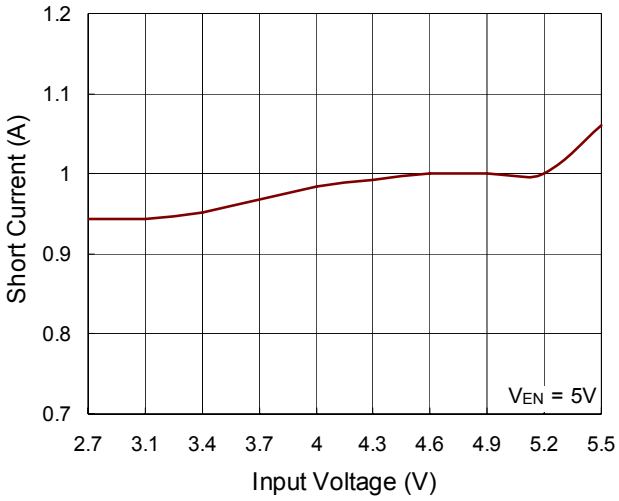
UVLO Threshold vs. Temperature



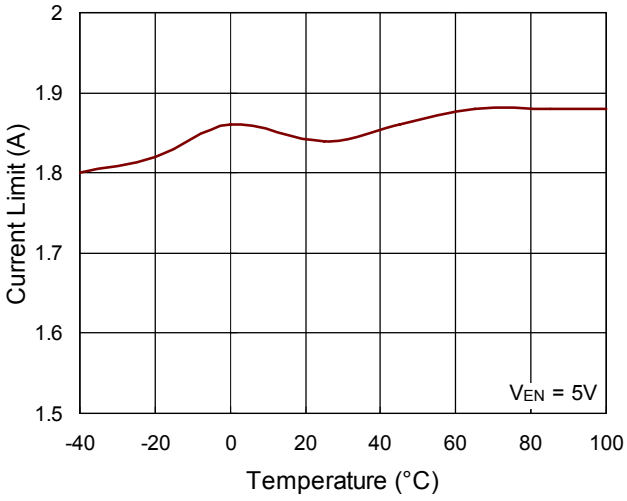
Current Limit vs. Input Voltage



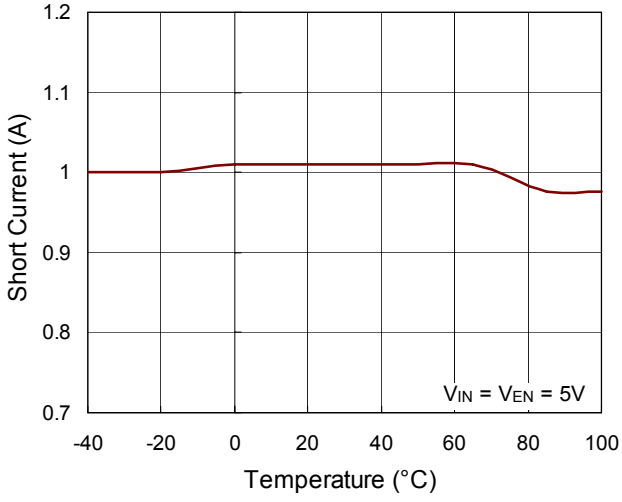
Short Current vs. Input Voltage



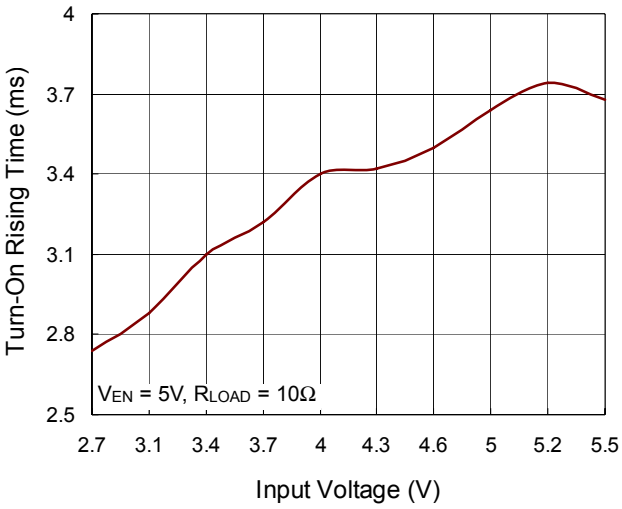
Current Limit vs. Temperature



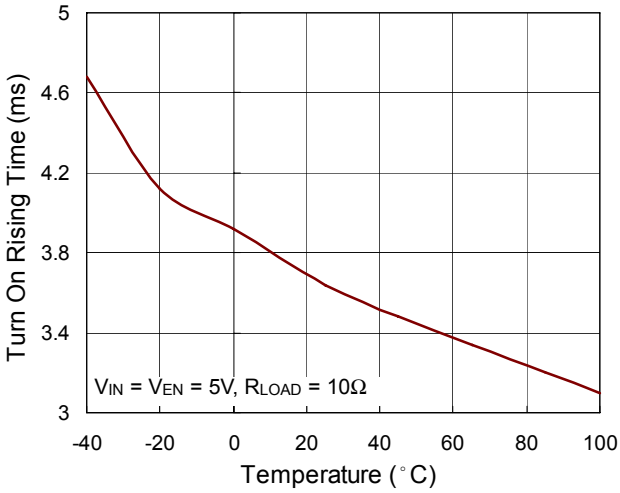
Short Current vs. Temperature



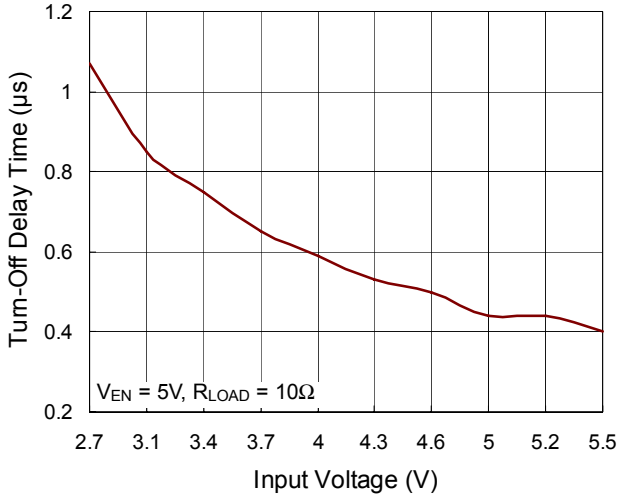
Turn-On Rising Time vs. Input Voltage



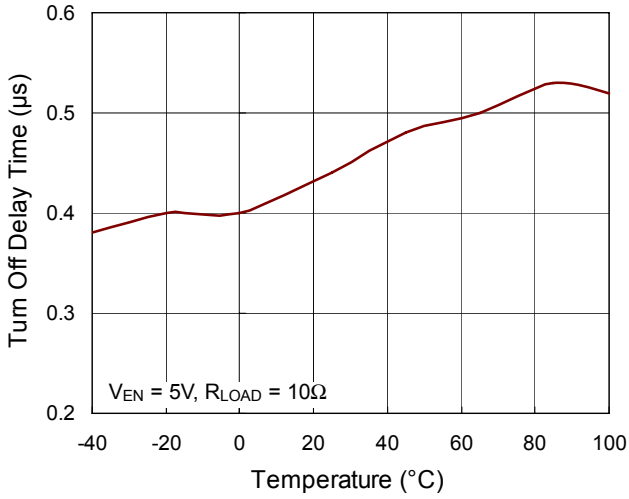
Turn On Rising Time vs. Temperature



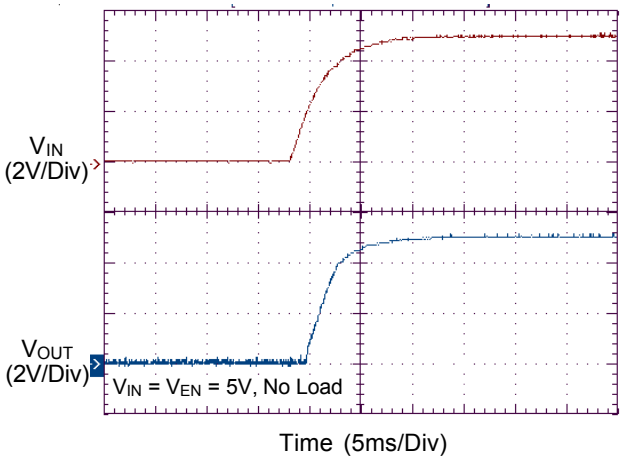
Turn-Off Delay Time vs. Input Voltage



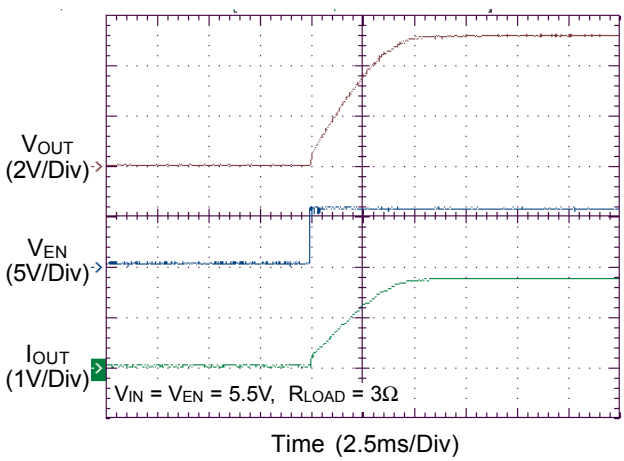
Turn Off Delay Time vs. Temperature



Power On from V_{IN}



Power On from EN



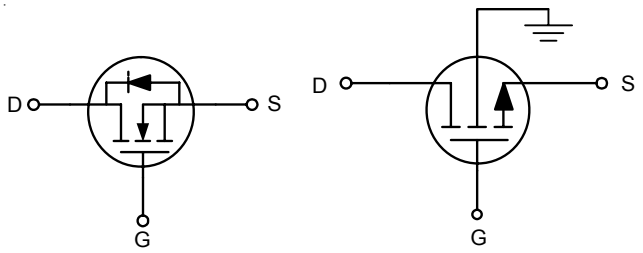
Applications Information

The RT9724 is a single N-MOSFET high-side power switches with enable input, optimized for self-powered and bus-powered Universal Serial Bus (USB) applications. The RT9724 is equipped with a charge pump circuitry to drive the internal N-MOSFET switch; the switch's low $R_{DS(ON)}$, 100mΩ, meets USB voltage drop requirements.

Input and Output

V_{IN} (input) is the power source connection to the internal circuitry and the drain of the MOSFET. V_{OUT} (output) is the source of the MOSFET. In a typical application, current flows through the switch from V_{IN} to V_{OUT} toward the load. If V_{OUT} is greater than V_{IN}, current will flow from V_{OUT} to V_{IN} since the MOSFET is bidirectional when on.

Unlike a normal MOSFET, there is no parasitic body diode between drain and source of the MOSFET, the RT9724 prevents reverse current flow if V_{OUT} is externally forced to a higher voltage than V_{IN} when the chip is disabled (V_{EN} < 0.8V).



Normal MOSFET RT9724

Chip Enable Input

The switch will be disabled when the EN pin is in a logic low condition. During this condition, the internal circuitry and MOSFET will be turned off, reducing the supply current to 0.1μA typical. Floating the EN may cause unpredictable operation. EN should not be allowed to go negative with respect to GND. The EN pin may be directly tied to V_{IN} to keep the part on.

Soft Start for Hot Plug-In Applications

In order to eliminate the upstream voltage droop caused by the large inrush current during hot-plug events, the "soft-start" feature effectively isolates the power source from extremely large capacitive loads, satisfying the USB voltage droop requirements.

Under Voltage Lockout

Under Voltage Lockout (UVLO) prevents the MOSFET switch from turning on until the input voltage exceeds approximately 1.75V. If input voltage drops below approximately 1.7V, UVLO turns off the MOSFET switch. Under-voltage detection functions only when the switch is enabled.

Current Limiting and Short-Circuit Protection

The current limit circuitry prevents damage to the MOSFET switch and the hub downstream port but can deliver load current up to the current limit threshold of typically 2A. When a heavy load or short circuit is applied to an enabled switch, a large transient current may flow until the current limit circuitry responds. Once this current limit threshold is exceeded, the device enters constant current mode until the thermal shutdown occurs or the fault is removed.

Universal Serial Bus (USB) & Power Distribution

The goal of USB is to enable device from different vendors to interoperate in an open architecture. USB features include ease of use for the end user, a wide range of workloads and applications, robustness, synergy with the PC industry, and low-cost implementation. Benefits include self-identifying peripherals, dynamically attachable and reconfigurable peripherals, multiple connections (support for concurrent operation of many devices), support for as many as 127 physical devices, and compatibility with PC Plug-and-Play architecture.

The Universal Serial Bus connects USB devices with a USB host: each USB system has one USB host. USB devices are classified either as hubs, which provide additional attachment points to the USB, or as functions, which provide capabilities to the system (for example, a digital joystick). Hub devices are then classified as either Bus-Power Hubs or Self-Powered Hubs.

A Bus-Powered Hub draws all of the power to any internal functions and downstream ports from the USB connector power pins. The hub may draw up to 500mA from the upstream device. External ports in a Bus-Powered Hub can supply up to 100mA per port, with a maximum of four external ports.

Self-Powered Hub power for the internal functions and downstream ports does not come from the USB, although the USB interface may draw up to 100mA from its upstream connection, to allow the interface to function when the remainder of the hub is powered down. The hub must be able to supply up to 500mA on all of its external downstream ports. Please refer to Universal Serial Specification Revision 2.0 for more details on designing compliant USB hub and host systems.

Over current protection devices such as fuses and PTC resistors (also called polyfuse or polyswitch) have slow trip times, high on-resistance, and lack the necessary circuitry for USB-required fault reporting.

The faster trip time of the RT9724 power distribution allows designers to design hubs that can operate through faults. The RT9724 provides low on-resistance and internal fault-reporting circuitry to meet voltage regulation and fault notification requirements.

Because the devices are also power switches, the designer of self-powered hubs has the flexibility to turn off power to output ports. Unlike a normal MOSFET, the devices have controlled rise and fall times to provide the needed inrush current limiting required for the bus-powered hub power switch.

Supply Filter/Bypass Capacitor

A 1uF low-ESR ceramic capacitor from V_{IN} to GND, located at the device is strongly recommended to prevent the input voltage drooping during hot-plug events. However, higher capacitor values will further reduce the voltage droop on the input. Furthermore, without the bypass capacitor, an output short may cause sufficient ringing on the input (from source lead inductance) to destroy the internal control circuitry. The input transient must not exceed 6V of the absolute maximum supply voltage even for a short duration.

Output Filter Capacitor

A low-ESR 150uF aluminum electrolytic or tantalum between V_{OUT} and GND is strongly recommended to meet the 330mV maximum droop requirement in the hub V_{BUS} (Per USB 2.0, output ports must have a minimum 120μF of low-ESR bulk capacitance per hub). Standard bypass methods should be used to minimize inductance and resistance between the bypass capacitor and the downstream connector to reduce EMI and decouple voltage droop caused when downstream cables are hot-insertion transients. Ferrite beads in series with V_{BUS}, the ground line and the 0.1μF bypass capacitors at the power connector pins are recommended for EMI and ESD protection. The bypass capacitor itself should have a low dissipation factor to allow decoupling at higher frequencies.

Voltage Drop

The USB specification states a minimum port-output voltage in two locations on the bus, 4.75V out of a Self-Powered Hub port and 4.4V out of a Bus-Powered Hub port. As with the Self-Powered Hub, all resistive voltage drops for the Bus-Powered Hub must be accounted for to guarantee voltage regulation (see Figure 7-47 of Universal Serial Specification Revision 2.0).

The following calculation determines $V_{OUT\ (MIN)}$ for multiple ports (N_{PORTS}) ganged together through one switch (if using one switch per port, N_{PORTS} is equal to 1) :

$$V_{OUT\ (MIN)} = 4.75V - [\ I_I \times (\ 4 \times R_{CONN} + 2 \times R_{CABLE}\ )\ ] - (0.1A \times N_{PORTS} \times R_{SWITCH}\ ) - V_{PCB}$$

Where

R_{CONN} = Resistance of connector contacts

(two contacts per connector)

R_{CABLE} = Resistance of upstream cable wires

(one 5V and one GND)

R_{SWITCH} = Resistance of power switch

(90mΩ typical for RT9715)

V_{PCB} = PCB voltage drop

The USB specification defines the maximum resistance per contact (R_{CONN}) of the USB connector to be 30mΩ and the drop across the PCB and switch to be 100mV. This basically leaves two variables in the equation: the resistance of the switch and the resistance of the cable.

If the hub consumes the maximum current (I_I) of 500mA, the maximum resistance of the cable is 90mΩ.

The resistance of the switch is defined as follows :

R_{SWITCH} = { 4.75V – 4.4V – [0.5A x (4 x 30mΩ + 2 x 90mΩ)] – V_{PCB} } ÷ (0.1A x N_{PORTS})

= (200mV – V_{PCB}) ÷ (0.1A x N_{PORTS})

If the voltage drop across the PCB is limited to 100mV, the maximum resistance for the switch is 250mΩ for four ports ganged together. The RT9724, with its maximum 100mΩ on-resistance over temperature, can fit the demand of this requirement.

Thermal Shutdown

Thermal protection limits the power dissipation in the RT9724. When the operation junction temperature exceeds 130°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools to 80°C. The RT9724 lowers its OTP trip level from 130°C to 100°C when output short circuit occurs (V_{OUT} < 1V) as shown in Figure 1.

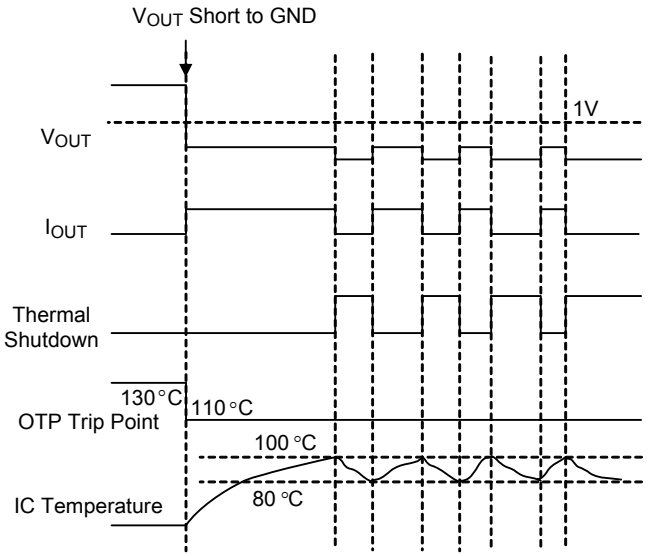


Figure 1. Short Circuit Thermal Folded Back Protection when Output Short Circuit Occurs (Patent)

Thermal Considerations

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOT-23-5 package, the thermal resistance θ_{JA} is 218.1°C/W on the standard JEDEC 51-7 four layers thermal test board. For WDFN-8L 2x2 package, the thermal resistance θ_{JA} is 120°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (218.1°C/W) = 0.458W for SOT-23-5 package

$P_{D(MAX)}$ = (125°C – 25°C) / (120°C/W) = 0.833W for WDFN-8L 2x2 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

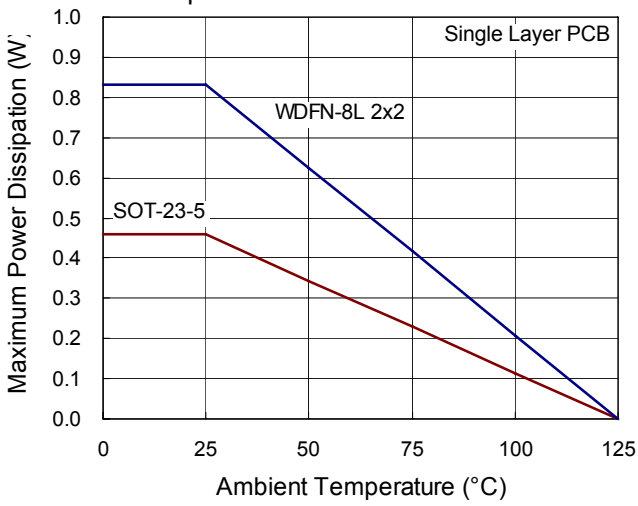


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Consideration

For best performance of the RT9724.The following guidelines must be followed :

- Input and Output capacitors should be placed close to the IC and connected to ground plane to reduce noise coupling.
- The GND shoule be connected to a strong ground plane for heat sink.
- Keep the main current traces as possible as short and wide.

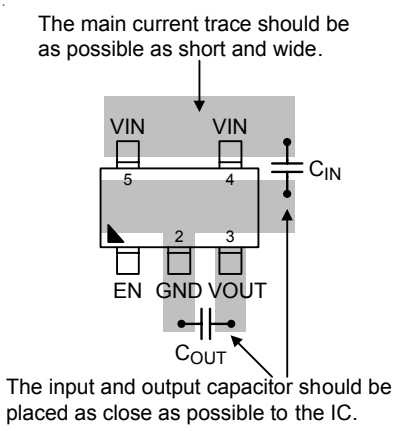


Figure 3. PCB Layout Guide for SOT-23-5 Package

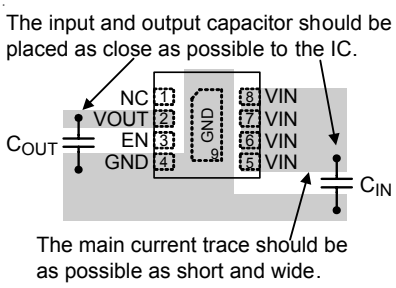
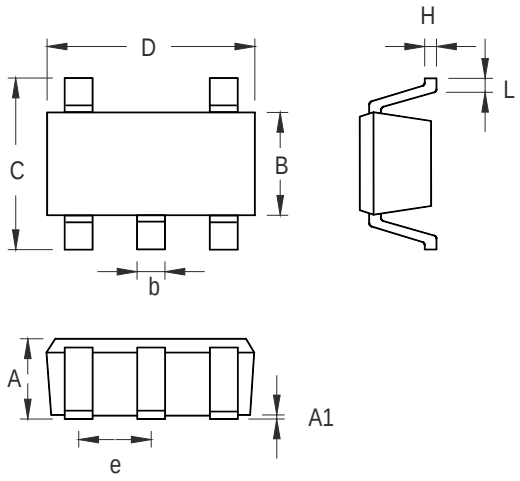


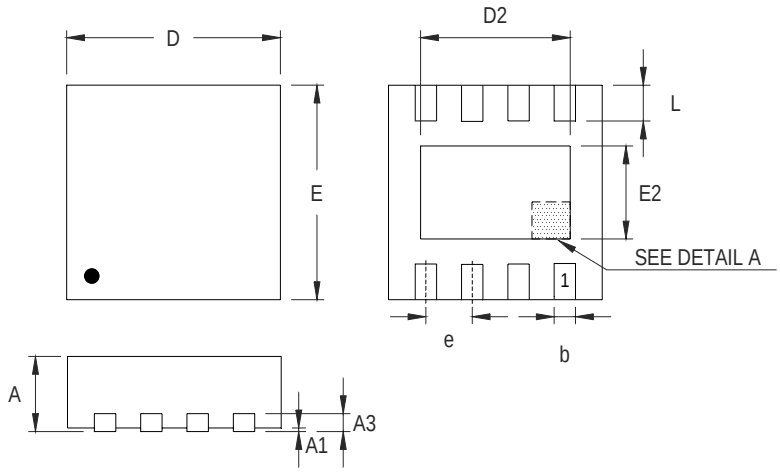
Figure 4. PCB Layout for WDFN Package

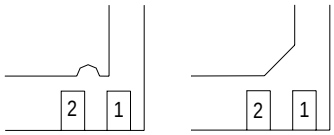
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

W-Type 8L DFN 2x2 Package

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