SGM61012/SGM61022
1.2A/2A High-Efficiency Buck Converters with AHP-COT Mode

GENERAL DESCRIPTION

The SGM61012 and SGM61022 are efficient high frequency synchronous Buck converters with an input voltage range of 2.3V to 5.5V and a wide output current range that is optimized for compact solutions. It operates in PWM mode at heavy loads and automatically enters power-save mode (PSM) at light loads to maintain its high efficiency.

Setting the MODE pin can enable deep sleep mode. This device operates with an ultra-low quiescent current, and it can maintain high efficiency at very low load. This function keeps the standby current at its lowest level, and can increase the standby time of battery-powered application. To meet the requirements of system power rails, the output capacitors with values above 100μF can be used by the internal loop compensation.

With its adaptive hysteresis and pseudo-constant on-time control (AHP-COT) architecture, the load transient performance is excellent and the output voltage regulation accuracy is achieved.

The SGM61012 and SGM61022 are available in a Green TDFN-2×2-8AL package.

FEATURES

- **Input Voltage Range: 2.3V to 5.5V**
- **AHP-COT Architecture**
- **Output Current:**
  - **SGM61012: 1.2A**
  - **SGM61022: 2A**
- **9μA Ultra-Low Quiescent Current in Deep Sleep Mode**
- **Fast Transient Regulation**
- **100% Duty Cycle Capability**
- **High-Efficiency Deep Sleep Mode under Light Load**
- **Output Discharge**
- **Short-Circuit Protection**
- **Power Good Output**
- **Thermal Shutdown**
- **Available in a Green TDFN-2×2-8AL Package**

APPLICATIONS

General Purpose Point-of-Load Power Supplies
Battery-Powered Applications

TYPICAL APPLICATION

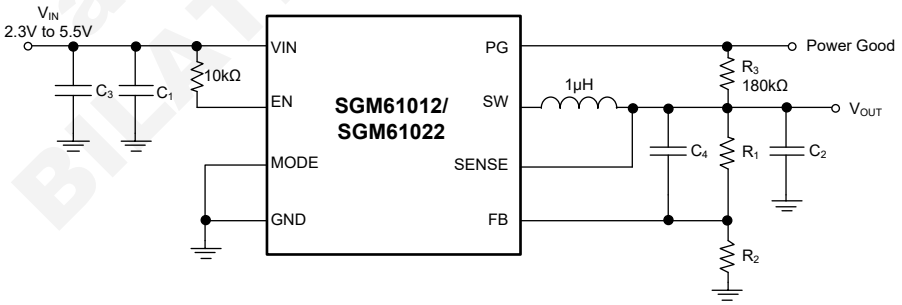


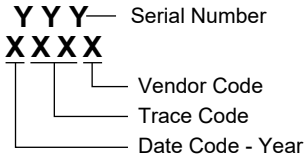
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61012	TDFN-2×2-8AL	-40℃ to +125℃	SGM61012XTDE8G/TR	GKG XXXX	Tape and Reel, 3000
SGM61022	TDFN-2×2-8AL	-40℃ to +125℃	SGM61022XTDE8G/TR	GJZ XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, PG and SENSE Voltages ..... -0.3V to 6V
SW Voltage ..... -TBDV to TBDV
FB Voltage ..... -0.3V to 3.6V
EN and MODE Voltages ..... -0.3V to V_{IN} + 0.3V
Sink Current at PG ..... 0mA to 0.5mA
Package Thermal Resistance
TDFN-2×2-8AL, θ_{JA} ..... TBD℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.3V to 5.5V
Output Voltage Range ..... 0.5V to 4V
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

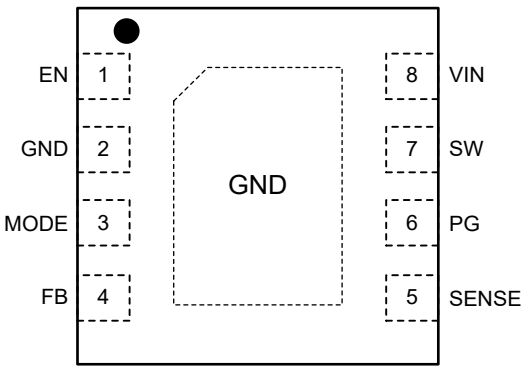
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-8AL

PIN DESCRIPTION

PIN	NAME	I/O (1)	DESCRIPTION
1	EN	I	Logic high sets the device active, logic low disables it and turns it into shutdown mode. It can connect a 10kΩ resistor to VIN pin if it is needed. Do not leave this pin floating.
2	GND	G	Power and Signal Ground.
3	MODE	I	Enable Setting for Deep Sleep Mode. The device adaptively goes into deep sleep mode when logic high, and does not enter it when logic low. Do not leave this pin floating.
4	FB	I	Feedback Input. An external feedback divider is needed for setting the output voltage.
5	SENSE	I	Output Voltage Sense Pin. Must be connected to output voltage.
6	PG	O	Power Good Open-Drain Output. If the output voltage is less than the regulation limit, this pin is pulled low. Leave this pin floating when not in use.
7	SW	P	Switching Node.
8	VIN	P	Power Supply Voltage Input.
Exposed Pad	GND	—	Connect it to GND. The thermal pad must be soldered to improve heat dissipation.

NOTE: 1. I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_J = +25℃, MODE = Low, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Input Voltage Range	V_{IN}		2.3		5.5	V
Quiescent Current into VIN	I_Q	I_{OUT} = 0mA, device no switching		25		μA
Quiescent Current into VIN (Deep Sleep Mode)		I_{OUT} = 0mA, device no switching, MODE = High		9		μA
Shutdown Current into VIN	I_{SD}	EN = Low			TBD	μA
Under-Voltage Lockout	V_{UVLO}	Input voltage falling		1.8		V
Under-Voltage Lockout Hysteresis		Rising above V_{UVLO}		120		mV
Thermal Shutdown	T_{JSD}	Temperature rising		+160		℃
Thermal Shutdown Hysteresis		Temperature falling below T_{JSD}		+25		℃
Logic Interface (EN Mode)						
High Level Input Voltage	V_{IH}	V_{IN} = 2.3V to 5.5V	1			V
Low Level Input Voltage	V_{IL}	V_{IN} = 2.3V to 5.5V			0.4	V
Input Leakage Current	I_{LKG}			0.01	TBD	μA
Power Good						
Power Good Threshold	V_{PG}	V_{OUT} falling referenced to V_{OUT} nominal		-10		%
Power Good Hysteresis				5		%
Low Level Voltage	V_{OL}	I_{SINK} = 500μA			TBD	V
PG Leakage Current	$I_{PG,LKG}$	V_{PG} = 5.0V		0.01	TBD	μA
Output						
Output Voltage Range	V_{OUT}		0.5		4.0	V
Deep Sleep Mode Output Voltage Accuracy		MODE = High; V_{IN} ≥ 2.3V and V_{IN} ≥ V_{OUT} + 1V	TBD		TBD	%
Feedback Regulation Voltage	V_{FB}	V_{IN} ≥ 2.3V and V_{IN} ≥ V_{OUT} + 1V		0.45		V
Feedback Input Bias Current	I_{FB}	V_{FB} = 0.45V		1	TBD	nA
Output Discharge Resistor	R_{DIS}	EN = Low, V_{OUT} = 1.8V		0.9		kΩ
Line Regulation				TBD		%/V
High-side MOSFET On-Resistance	$R_{DS(ON)}$	I_{SW} = 500mA		119		mΩ
Low-side MOSFET On-Resistance		I_{SW} = 500mA		80		mΩ
High-side MOSFET Switch Current Limit	I_{LIM}	Rising inductor current (SGM61012)		2.8		A
		Rising inductor current (SGM61022)		3.5		A

FUNCTIONAL BLOCK DIAGRAM

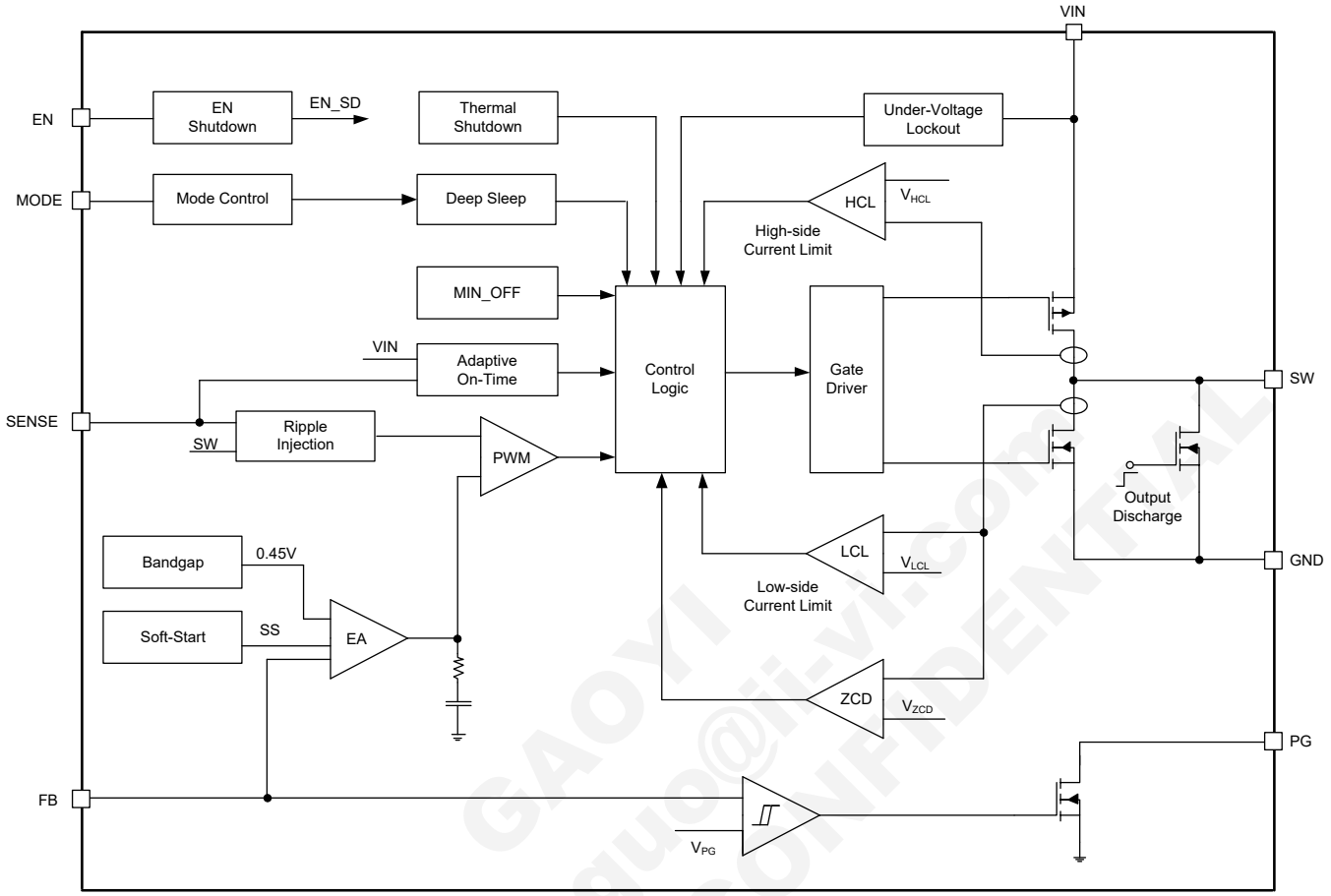


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61012 and SGM61022 are high-efficient Buck converters with AHP-COT architecture and advanced regulation topology.

At medium to heavy loads, the device works in pulse width modulation (PWM) mode. At light load, it automatically switches to power-save mode (PSM). In PWM mode, the device works with a nominal switching frequency of 2MHz. When the load current falls, the device goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current.

When pulling up the MODE pin, the device can enter deep sleep mode automatically at very light load to achieve high efficiency. If the circuit has no load current, 9μA low quiescent current is sufficient to maintain the output voltage. Deep sleep mode can reduce the standby energy consumption of system. During shutdown mode, the energy consumption falls below 1μA.

Under-Voltage Lockout (UVLO)

The device implements the under-voltage lockout (UVLO) with a 120mV (TYP) hysteresis. When the input voltage falls below the V_{UVLO}, it shuts down the device.

Enable and Disable

A logic high input to EN activates the device, and a logic low disables the device. A 10kΩ resistor is recommended to add between EN and VIN, and do not leave it floating.

Power Good (PG)

The power good output of SGM61012 and SGM61022 will be low in the condition that the output voltage less than its nominal value. If the output exceeds 95% of the regulated voltage, the power good is in high impedance state. If the output voltage is less than 90% of the regulated voltage, the power good is driven to low.

The PG pin is an open-drain output with a maximum of 0.5mA sink current. A pull-up resistor connecting to power good output is required. When the device is disabled or under-voltage lockout, the PG pin is driven to low (see Table 1). The PG signal connected to the EN pin of other converters can be used for multiple rails sequences. Leave the PG pin floating when not in use.

Table 1. Logic Table of PG Pin

Device Information		Logic Status	
		High Z	Low
Enable (EN = High)	$V_{FB} \geq V_{PG}$	√	
	$V_{FB} \leq V_{PG}$		√
Shutdown (EN = Low)		√	
UVLO	$0.7V < V_{IN} < V_{UVLO}$	√	
Thermal Shutdown	$T_J > T_{JSD}$	√	
Power Supply Removal	$V_{IN} < 0.7V$	√	

100% Duty Cycle

The device provides low input-to-output voltage drop by going into 100% duty cycle mode. In this mode, the high-side MOSFET is constantly turned on and the low-side MOSFET is turned off. This function can increase the operation time to the utmost extent for battery powered applications. To maintain an appropriate output voltage, the minimum input voltage is calculated by:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

- V_{IN_MIN} is the minimum input voltage.
- I_{OUT_MAX} is the maximum output current.
- R_{DSON} is the high-side MOSFET on-resistance.
- R_L is the inductor ohmic resistance.

Output Discharge

Whenever the device is disabled by enable, thermal shutdown or under-voltage lockout, the output is discharged by the SW pin through a typical discharge resistor of R_{DIS}.

DETAILED DESCRIPTION (continued)

Soft-Start

When EN is set to logic high and after about 150μs delay, the device starts switching and V_{OUT} increases with 600μs (TYP) internal soft-start circuit.

Inductor Current Limit

The device implements an inductor current limit if there is over-current or short-circuit. Both the peak current of high-side and valley current of low-side power MOSFETs are limited to protect the device. The high-side MOSFET is turned off and the low-side MOSFET is turned on to reduce the inductor current when the high-side switch current limit is triggered. The low-side MOSFET is turned off and the high-side switch is turned on again when the inductor current drops to the low-side switch current limit. It repeats until the inductor current falls below the high-side switch current limit. The actual current limit value may larger than the static current limit due to internal propagation delays.

Power-Save Mode (PSM)

Once the load current decreases, setting MODE pin low, the SGM61012 and SGM61022 will enter power-save mode. Then, the device has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency. In power-save mode, the inductor current is discontinuous. Then a fixed on-time architecture is activated and the typical on-time is t_{ON} = 500ns × (V_{OUT}/V_{IN}).

Deep Sleep Mode

The SGM61012 and SGM61022 provide a deep sleep mode function, which is enabled by setting MODE pin high. The device enters into this mode when load current decreases to about 6.5mA (1), and exits when load current is greater than 15mA (1). Once enters deep sleep mode, all other control blocks are shut down, and only a dedicated low power consuming block monitors the output voltage. In this mode, the quiescent current consumption of the device is about 9μA (TYP), and the output voltage is 2% higher than the setting voltage approximately.

Even in the deep sleep mode, the dynamic load regulation of SGM61012 or SGM61022 is excellent.

NOTE: 1. Test condition: V_{IN} = 3.6V, V_{OUT} = 1.8V, L = 1μH.

Thermal Shutdown

To protect the device from overheating damage, thermal protection is included in the device. If the junction temperature exceeds the typical T_{JSD} (+160℃ TYP), the switching will stop. When the device temperature drops below the threshold minus hysteresis, the switching will resume automatically.

APPLICATION INFORMATION

The SGM61012 and SGM61022 are synchronous Buck converters with output voltage adjusted by feedback dividers. Taking SGM61012 typical application as a reference, the following sections discuss the design of external components and how to achieve the application.

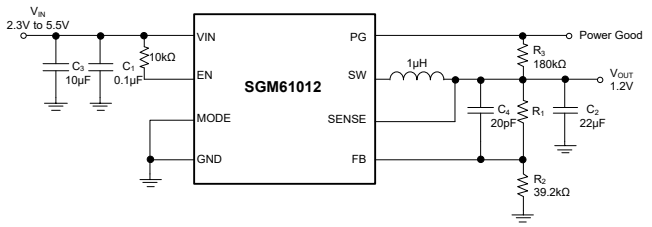


Figure 3. SGM61012 Typical Application Circuit

Requirements

The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage	2.3V to 5.5V
Output Voltage	1.2V
Output Ripple Voltage	< 20mV
Output Current (MAX)	1.2A

Design Details

Table 3 shows the components included in this example.

Table 3. Components List

Reference	Description	Manufacturer
L_1	1μH, Power Inductor, SGM61012 3A or SGM61022 4.5A	Std
C_1	0.1μF, Ceramic Capacitor, 10V, X7R, Size 0603	Std
C_2	22μF, Ceramic Capacitor, 6.3V, X7R, Size 0805	Std
C_3	10μF, Ceramic Capacitor, 10V, X7R, Size 0805	Std
C_4	20pF, Ceramic Capacitor, 50V, C0G, Size 0603	Std
R_1	Depending on the output voltage, Chip Resistor, 1/16W, 1%, Size 0603	Std
R_2	39.2kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std
R_3	180kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Std

Adjustable Output Voltage

An external resistor divider connected to FB pin is used for setting the output voltage. Through adjusting R_1 and R_2, the output voltage can be programmed to the desired value. Calculate R_1 and R_2 with Equation 2.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.45V \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

R_2 should be less than 40kΩ for higher accuracy. Make sure that the current flowing through R_2 is at least 100 times greater than the current of FB pin. A lower value of R_2 increases the robustness against noise injection, and higher values reduce the input current.

A feed-forward capacitor is recommended to improve the performance of smooth transition into power-save mode and reduce undershoot during load transient. 10 to 20pF is enough for typical applications.

Output Filter

The output low pass filter is the combination of inductor and output capacitor. Table 4 shows the suggested value.

Table 4. Inductor and Capacitor Combinations

L (μH) (1)	C_{OUT} (μF) (2)		
	10	22	47
0.47		√	√
1	√	√ (3) (4)	√
2.2	√	√	

NOTES:

1. Expected inductor tolerance and current de-rating. Effective inductance has +20% and -30% variation.
2. Expected capacitance tolerance and bias voltage de-rating. Effective capacitance has +20% and -50% variation.
3. "√" means the recommended filter combinations.
4. Filter combination in typical application.

APPLICATION INFORMATION (continued)

Inductor Design

Equation 3 is conventionally used to calculate the output inductance of a Buck converter. The inductor should be selected by its value and the saturation current. The saturation current of inductor should be higher than I_{L_MAX} in Equation 3, and sufficient margin should be reserved. Typically, the current above high-side current limit is enough, and a 10% to 30% ripple current is selected to calculate the inductance. Larger inductor can reduce the ripple current, but with an increasing response time.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (3)$$

where:

- I_{OUT_MAX} is the maximum output current.
- ΔI_L is the inductor current ripple.
- f_{SW} is the switching frequency.
- L is the inductor value.

Capacitor Design

For input capacitor design, a X5R/X7R dielectric ceramic capacitor should be selected for its low ESR and high frequency performance. 10μF is enough for most applications. The voltage rating of input capacitor must be considered for its significant bias effect. The input ripple voltage can be calculated from Equation 4.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (4)$$

The ripple current rating of input capacitor should be greater than I_{CIN_RMS} in Equation 5 and the maximum value occurs at 50% duty cycle. A 0.1μF capacitor is suggested to add for further input decoupling of device.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN}-V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (5)$$

For output capacitor design, output ripple, transient response and loop stability should be considered. Minimum capacitance of output ripple criteria can be calculated from Equation 6.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (6)$$

Both the input and output capacitors should be placed as close to VIN/Sense and GND pins as possible to reduce noise caused by PCB parasitic parameters.

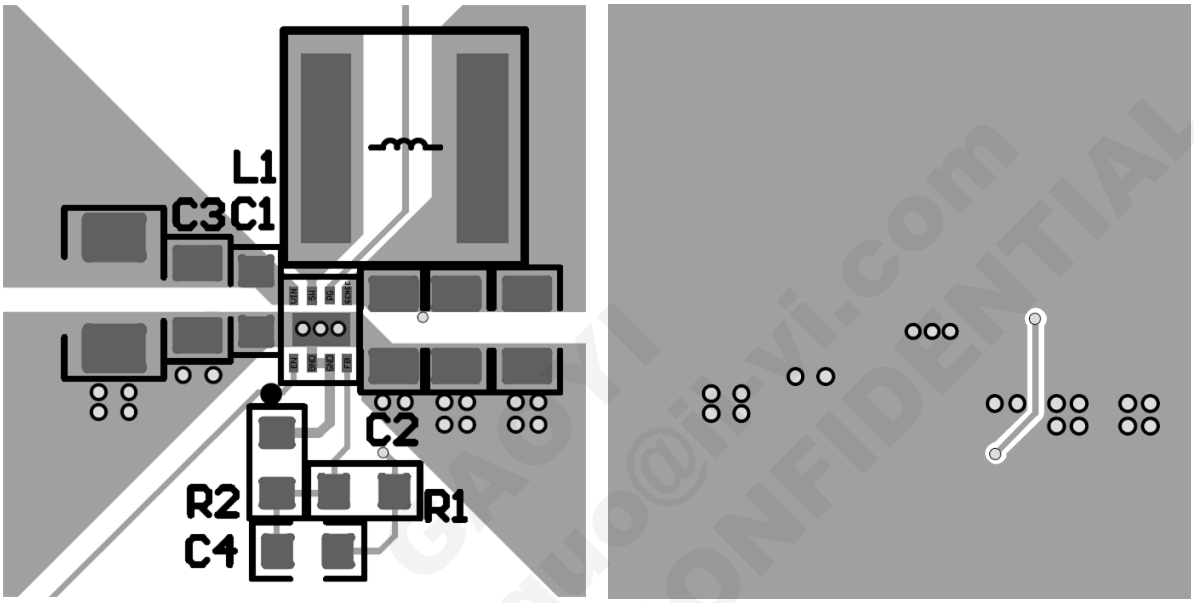
To simplify customer's design process, the inductor and output capacitor combinations are recommended in Table 4.

Layout Considerations

Good PCB layout is the key factor for high performance operation of a device regarding the stability, regulation, efficiency and other performance measures.

A list of guidelines for designing the PCB layout of SGM61012/SGM61022 is provided below:

- Place the power components close together and connect them with short and wide routes. The low-side of the capacitors must be connected to GND properly to avoid potential shift.
- Signal traces are connected to the FB and SENSE pins. Connect the inductor with a short trace. Keep the traces away from SW nodes.
- Typical suggested layout is provided in Figure 4.

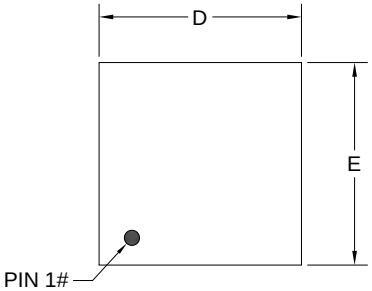


Top Layer Bottom Layer

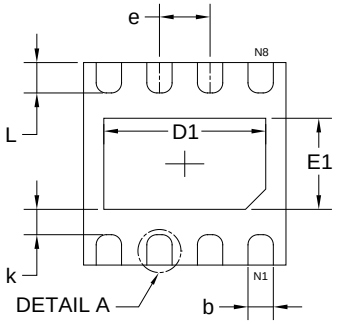
Figure 4. PCB Layout

PACKAGE OUTLINE DIMENSIONS

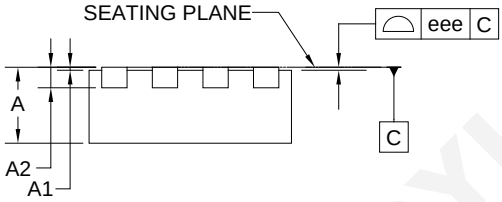
TDFN-2×2-8AL



TOP VIEW

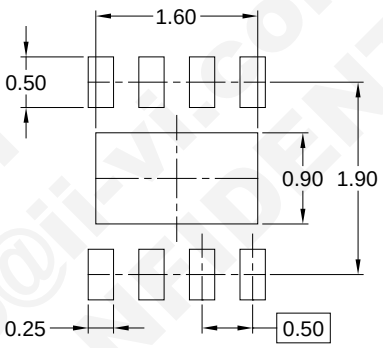


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



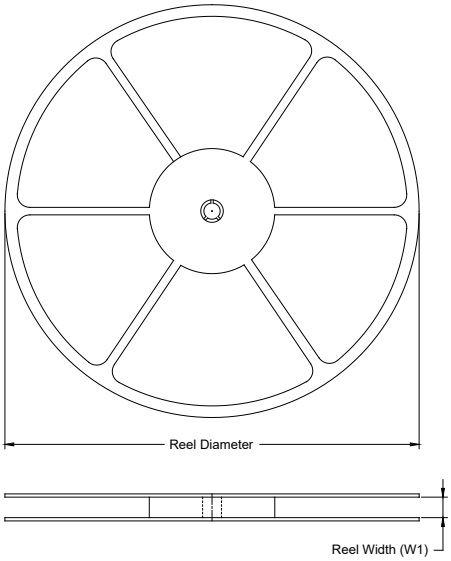
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	0.250	0.300
D	1.900	2.000	2.100
D1	1.450	1.600	1.700
E	1.900	2.000	2.100
E1	0.750	0.900	1.000
k	0.150	0.250	0.350
e	0.450	0.500	0.550
L	0.200	0.300	0.400
eee	0.080		

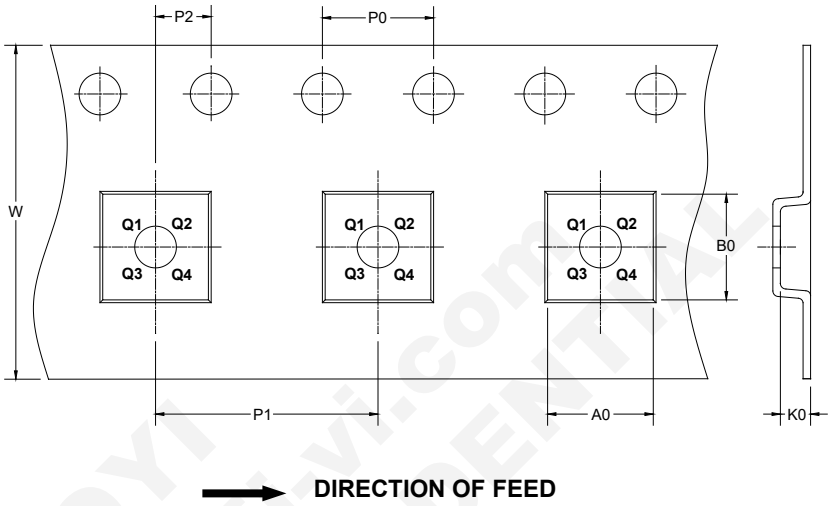
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



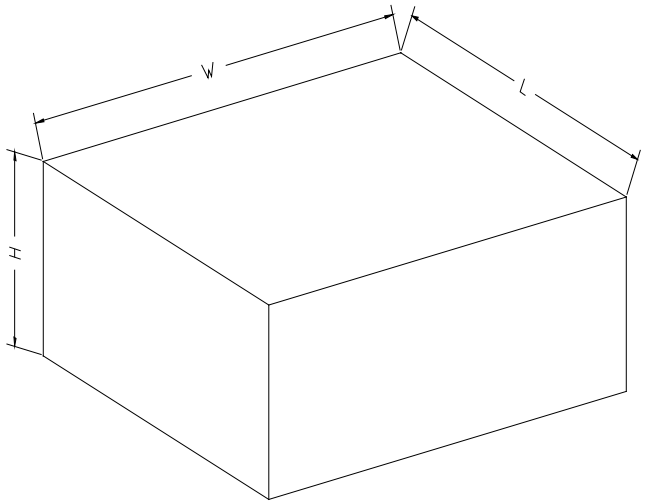
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002