Application Note: SY8501

High Efficiency 500kHz, 1.0A 100V Input Synchronous Step Down Regulator

General Description

SY8501 develops high efficiency synchronous step-down DC-DC converter capable of delivering 1.0A current. The SY8501 operates over a wide input voltage range from 7V to 100V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The device adopts the instant PWM architecture to achieve fast transient responses for high step down applications.

Ordering Information

SY8501 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8501FCC	SO8E	--

Features

- low $R_{DS(ON)}$ for internal switches (top/bottom): 500mΩ/240mΩ
- 7-100V input voltage range
- 1A output current capability
- Adjustable switching frequency
- Instant PWM architecture to achieve fast transient responses.
- 2ms internal softstart limits the inrush current
- Precious +/-2% 1.2V reference
- RoHS Compliant and Halogen Free
- Compact SO8E package

Applications

- Non-Isolated Telecommunication Buck Regulator
- Secondary High Voltage Post Regulator
- Automotive Systems

Typical Applications

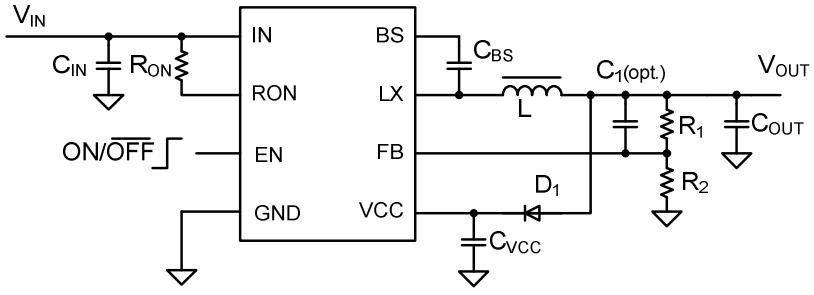


Figure 1. Schematic Diagram

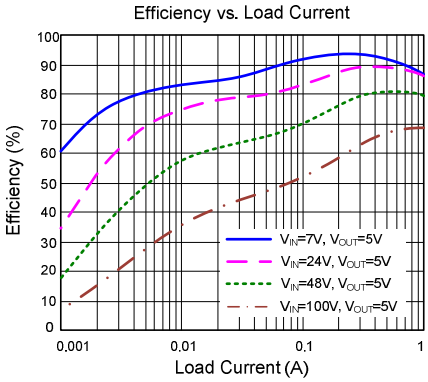
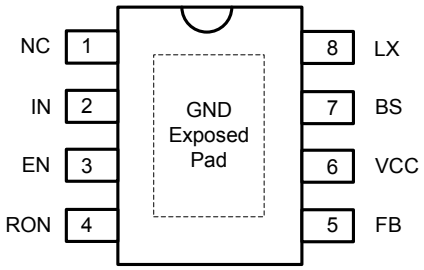


Figure 2. Efficiency

Pinout (top view)



(SO8E)

Top Mark: AMA*xyz* for SY8501FCC (Device code: AMA, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
NC	1	Not connected.
IN	2	Input pin. Decouple this pin to GND with a low ESR ceramic cap.
EN	3	Enable control. The device has an accurate 1.2V rising threshold. This pin can also be used to program the Vin turn on voltage with resistor divider.
RON	4	Connect a resistor from this pin to IN to set the top switch ON time.
FB	5	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=1.2*(1+R1/R2)
VCC	6	Supply input of internal LDO.
BS	7	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap.
LX	8	Inductor pin. Connect this pin to the switching node of inductor
GND	Exposed Pad	Ground pin.

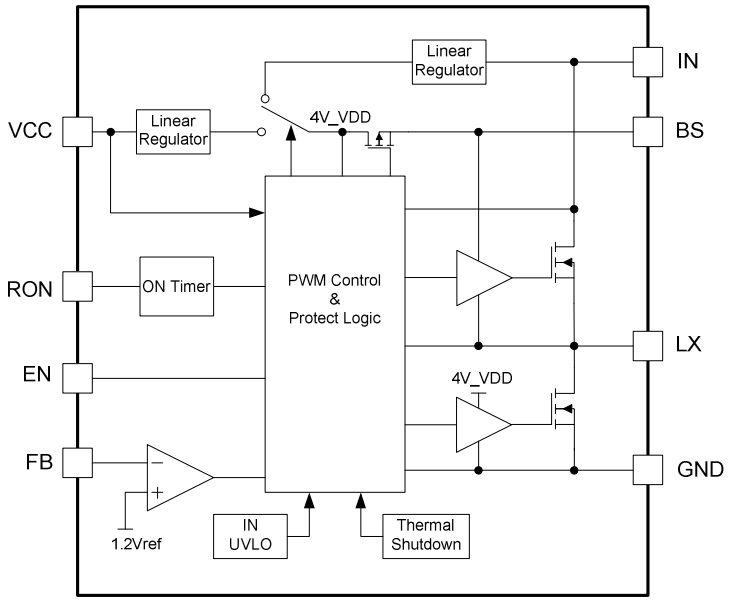
Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 110V
EN, LX---------- VIN + 0.3V
BS ---------- LX + 6V
FB, RON Voltage ---------- 6V
VCC ---------- 30V
Power Dissipation, PD @ T_A = 25°C SO8E ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30°C/W
θ_{JC} ---------- 10°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 7V to 100V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Block Diagram



Electrical Characteristics

(V_{IN} = 48V, V_{OUT} = 12V, L = 47uH, C_{OUT} = 10uF, TA = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		7		100	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}*105%			400	μA
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}		1.176	1.2	1.224	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			500		mΩ
Bottom FET RON	$R_{DS(ON)2}$			240		mΩ
Top FET peak Current Limit	$I_{LIM,Top}$			1.8		A
Bottom FET Valley Current Limit	$I_{LIM,Bottom}$		1			A
EN Rising Threshold	V_{ENH}			1.2		V
EN Falling Threshold	V_{ENL}		0.8			V
Input UVLO Rising Threshold	V_{UVLO}		6	6.5	7	V
Input UVLO Hysteresis	V_{HYS}			0.5		V
Programmable Switching Frequency Range	F_S	$F_S(KHz) = \frac{550}{R_{on}(M\Omega)}$	200		1000	kHz
Min ON Time				120		ns
Min OFF Time				350		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

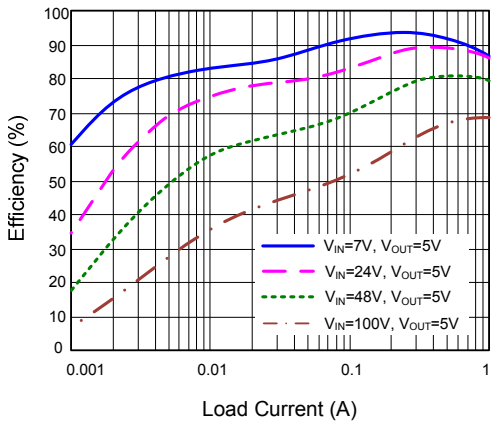
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at TA = 25°C on a low effective 4-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of SO8E packages is the case position for θJC measurement.

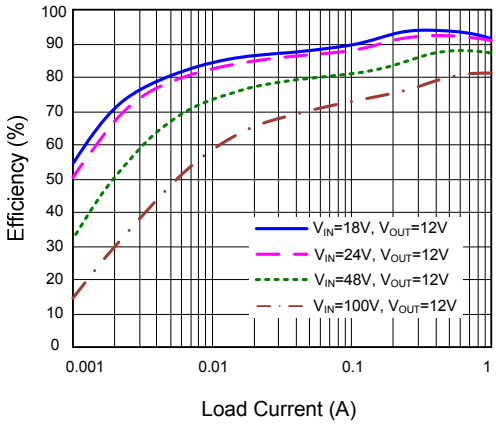
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

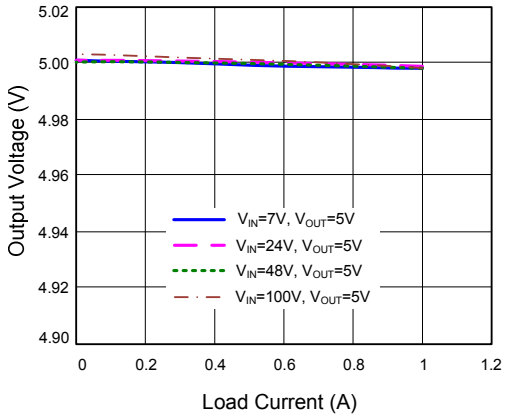
Efficiency vs. Load Current



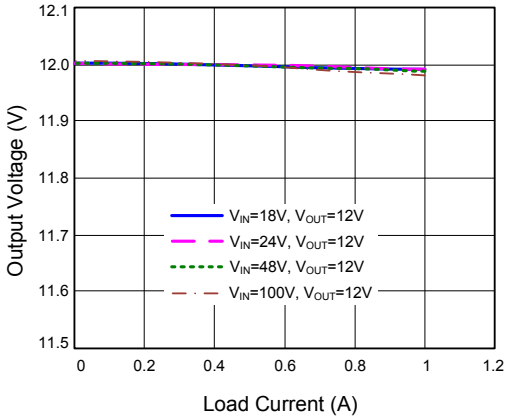
Efficiency vs. Load Current



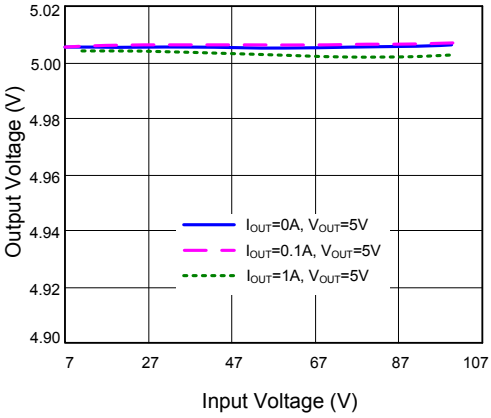
Load Regulation



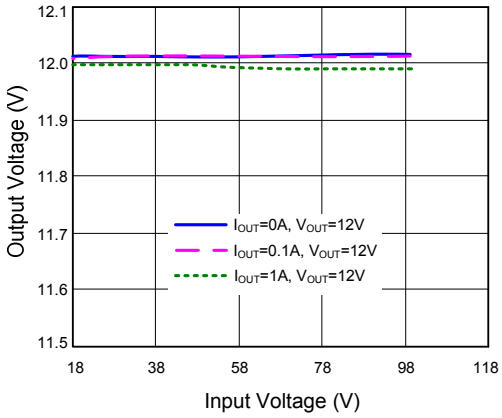
Load Regulation



Line Regulation

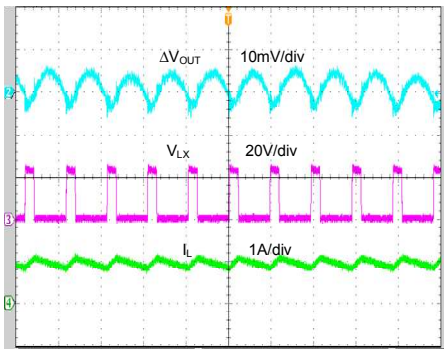


Line Regulation



Output Ripple

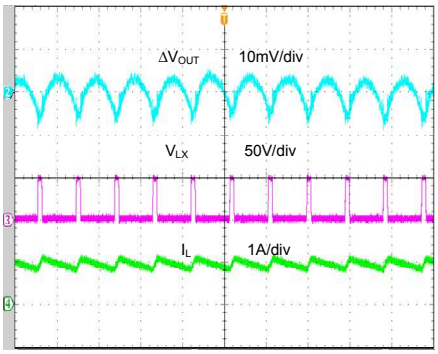
(V_{IN}=24V, V_{OUT}=5V, I_O=1A)



Time (2μs/div)

Output Ripple

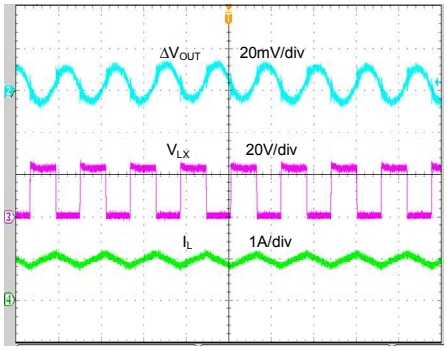
(V_{IN}=48V, V_{OUT}=5V, I_O=1A)



Time (2μs/div)

Output Ripple

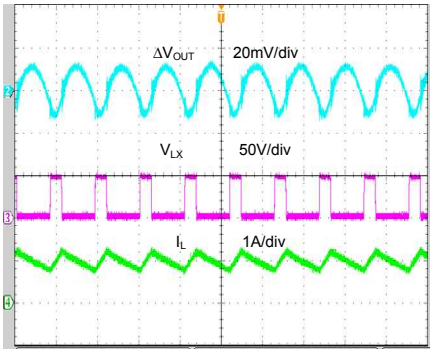
(V_{IN}=24V, V_{OUT}=12V, I_O=1A)



Time (2μs/div)

Output Ripple

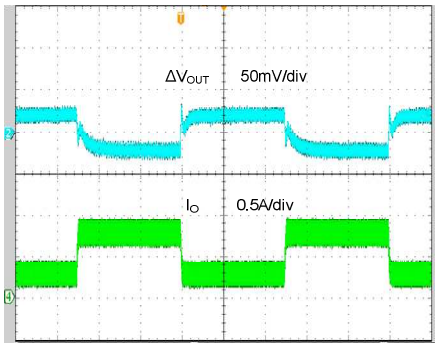
(V_{IN}=48V, V_{OUT}=12V, I_O=1A)



Time (2μs/div)

Load Transient

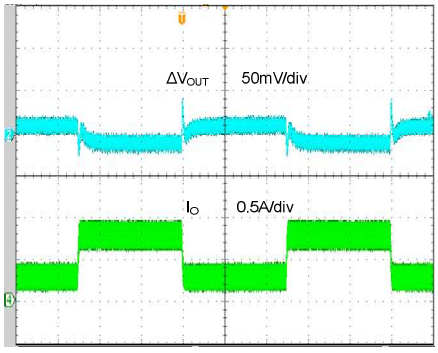
(V_{IN}=24V, V_{OUT}=5V, I_O=0.25 ~ 0.75A)



Time (400μs/div)

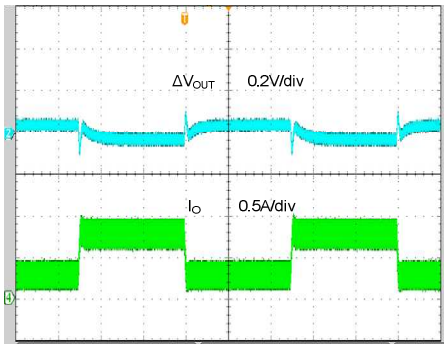
Load Transient

(V_{IN}=48V, V_{OUT}=5V, I_O=0.25 ~ 0.75A)



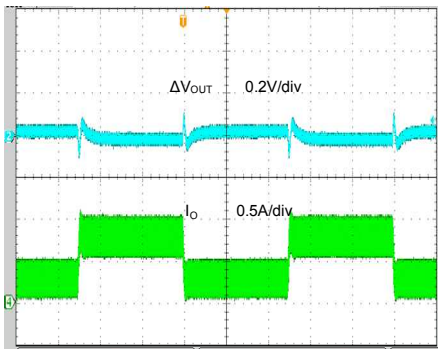
Time (400μs/div)

Load Transient
(V_{IN}=24V, V_{OUT}=12V, I_O=0.25 ~ 0.75A)



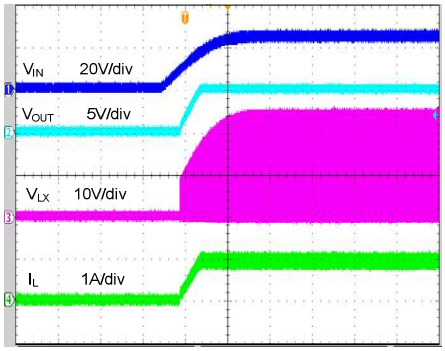
Time (400μs/div)

Load Transient
(V_{IN}=48V, V_{OUT}=12V, I_O=0.25 ~ 0.75A)



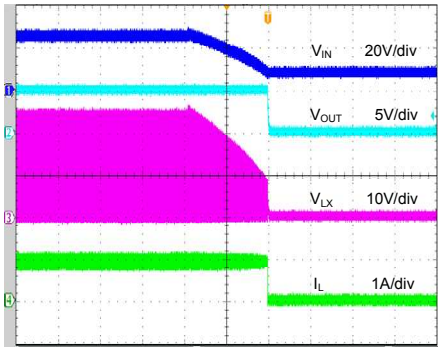
Time (400μs/div)

Startup from V_{IN}
(V_{IN}=24V, V_{OUT}=5V, I_O=1A)



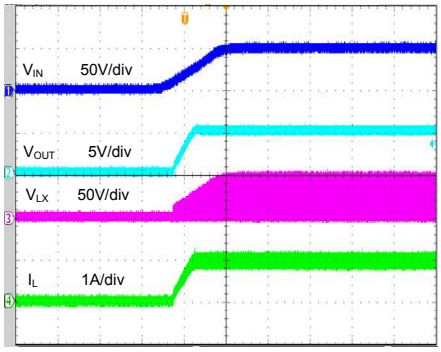
Time (4ms/div)

Shutdown from V_{IN}
(V_{IN}=24V, V_{OUT}=5V, I_O=1A)



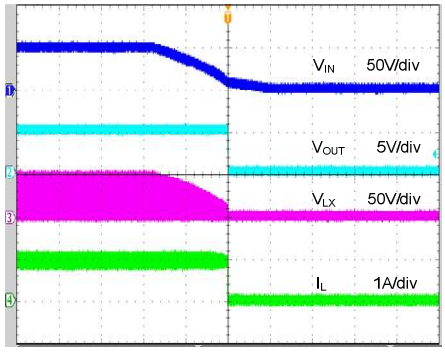
Time (4ms/div)

Startup from V_{IN}
(V_{IN}=48V, V_{OUT}=5V, I_O=1A)



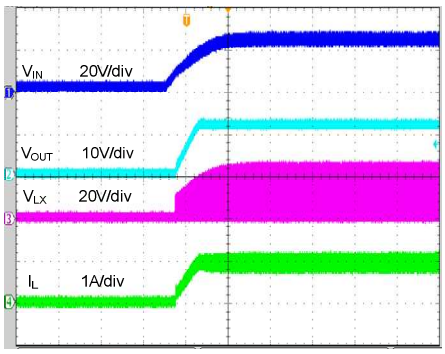
Time (4ms/div)

Shutdown from V_{IN}
(V_{IN}=48V, V_{OUT}=5V, I_O=1A)



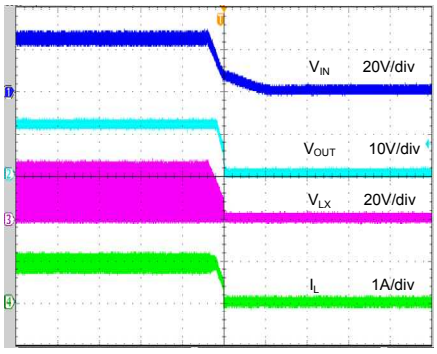
Time (10ms/div)

Startup from V_{IN}
(V_{IN}=24V, V_{OUT}=12V, I_O=1A)



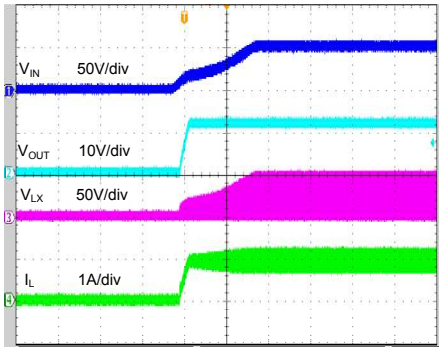
Time (4ms/div)

Shutdown from V_{IN}
(V_{IN}=24V, V_{OUT}=12V, I_O=1A)



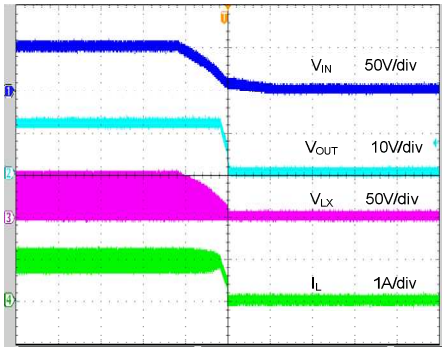
Time (10ms/div)

Startup from V_{IN}
(V_{IN}=48V, V_{OUT}=12V, I_O=1A)



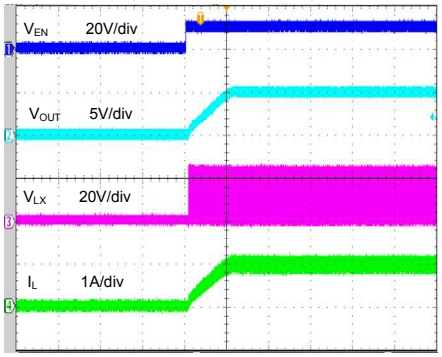
Time (10ms/div)

Shutdown from V_{IN}
(V_{IN}=48V, V_{OUT}=12V, I_O=1A)



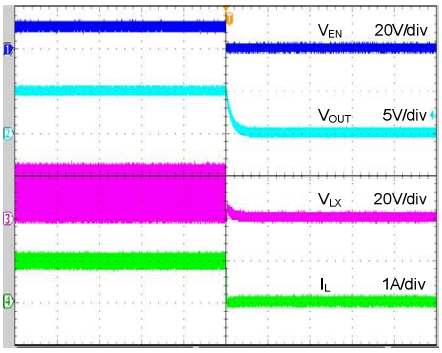
Time (10ms/div)

Startup from Enable
(V_{IN}=24V, V_{OUT}=5V, I_O=1A)



Time (2ms/div)

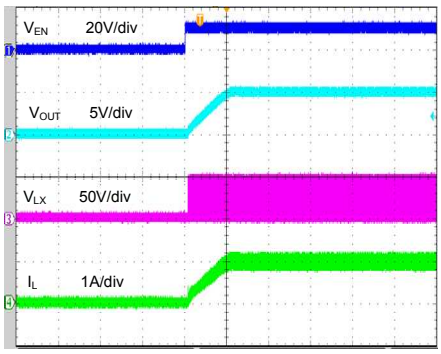
Shutdown from Enable
(V_{IN}=24V, V_{OUT}=5V, I_O=1A)



Time (400μs/div)

Startup from Enable

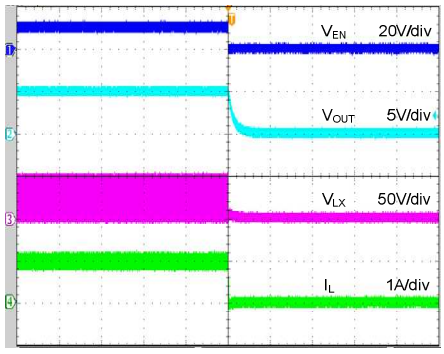
(V_{IN}=48V, V_{OUT}=5V, I_O=1A)



Time (2ms/div)

Shutdown from Enable

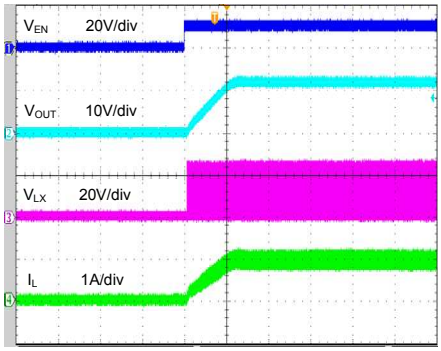
(V_{IN}=48V, V_{OUT}=5V, I_O=1A)



Time (400μs/div)

Startup from Enable

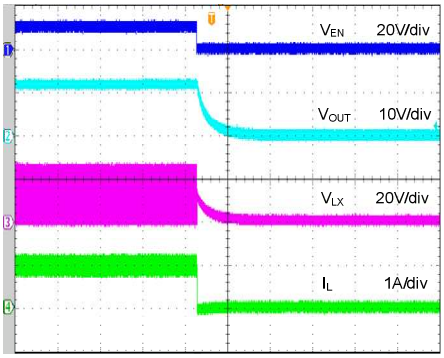
(V_{IN}=24V, V_{OUT}=12V, I_O=1A)



Time (2ms/div)

Shutdown from Enable

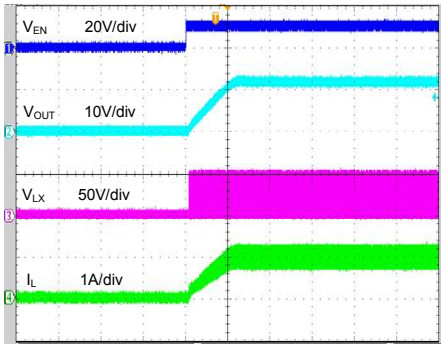
(V_{IN}=24V, V_{OUT}=12V, I_O=1A)



Time (400μs/div)

Startup from Enable

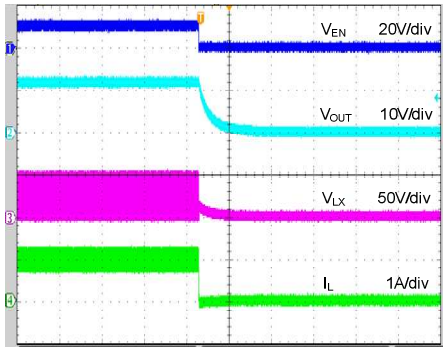
(V_{IN}=48V, V_{OUT}=12V, I_O=1A)



Time (2ms/div)

Shutdown from Enable

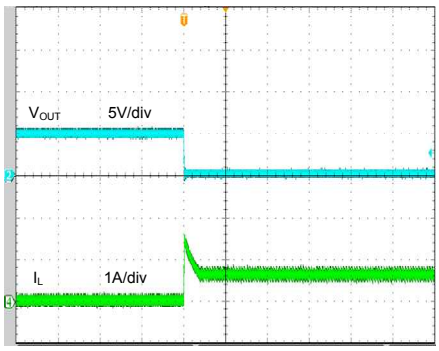
(V_{IN}=48V, V_{OUT}=12V, I_O=1A)



Time (400μs/div)

Short Circuit Protection

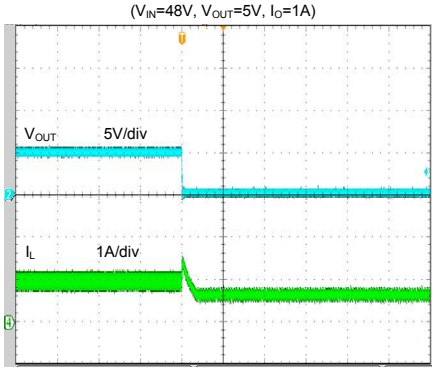
(V_{IN}=48V, V_{OUT}=5V, I_O=0A)



Time (200μs/div)

Short Circuit Protection

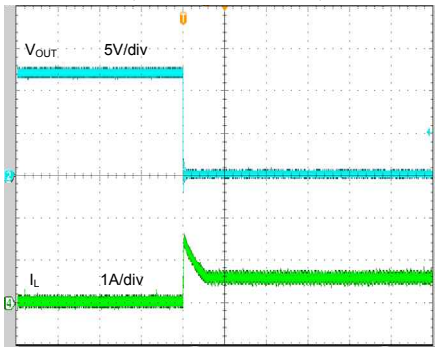
(V_{IN}=48V, V_{OUT}=5V, I_O=1A)



Time (200μs/div)

Short Circuit Protection

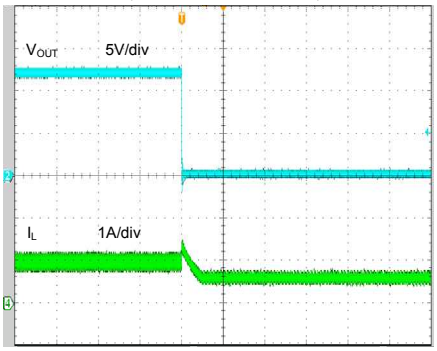
(V_{IN}=48V, V_{OUT}=12V, I_O=0A)



Time (200μs/div)

Short Circuit Protection

(V_{IN}=48V, V_{OUT}=12V, I_O=1A)



Time (200μs/div)

Operation Description

The SY8501 operates over a wide input voltage range from 7V to 100V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. This regulator adopts the instant PWM architecture with an internal ripple control scheme using an on-time inversely proportional to V_{IN} to achieve fast transient responses for high voltage step down applications. This architecture requires no loop compensation. In addition, it operates at pseudo-constant frequency under continuous conduction mode to minimize the size of inductor and capacitor.

Applications Information

Because of the high integration in the SY8501 IC, the application circuit based on this regulator IC is rather simple. Only on-timer resistor R_{ON}, feedback resistors (R1 and R2), input capacitor C_{IN}, output capacitor C_{OUT} and output inductor L need to be selected for the targeted applications specifications.

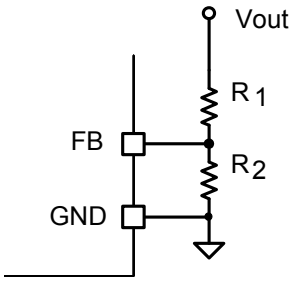
This regulator is well suited for 48 Volt telecom and the new 42V automotive power bus ranges.

Output Voltage Program.

Choose R1and R2 to program the proper output voltage. To minimize the power consumption under light loads,
it is desirable to choose large resistance values for both R1 and R2.

$$V_{out} = (1 + \frac{R1}{R2}) \times V_{FB}$$

V_{FB} is typical 1.2V.



Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L_2 = \frac{V_{OUT} \times (1 - V_{OUT} / V_{IN\_MAX})}{F_S \times I_{OUT\_MAX} \times 40\%}$$

Where Fs is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY8501 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected greater than the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT} \times (1 - V_{OUT} / V_{IN\_MAX})}{F_S \times L_2 \times 2}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with smaller DCR to achieve a good overall efficiency.

Input Capacitor C_{IN}:

The ripple current through input capacitor is calculated as：

$$I_{CIN\_RMS} = I_{OUT\_MAX} \times \sqrt{D(1-D)}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} = \frac{I_{OUT} \times V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta V_{IN} \times F_S \times \eta \times V_{IN}^2}$$

ΔV_{IN} is desired input voltage ripple

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 1uF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. It is recommended to use X5R or better grade ceramic capacitor greater than 10uF capacitance.

On Time

The on-time for the SY8501 is determined by the R_{ON} resistor, and is inversely proportional to the input voltage, resulting in a nearly constant frequency as V_{IN} is varied over its range.

Frequency vs. Ron Resistor:

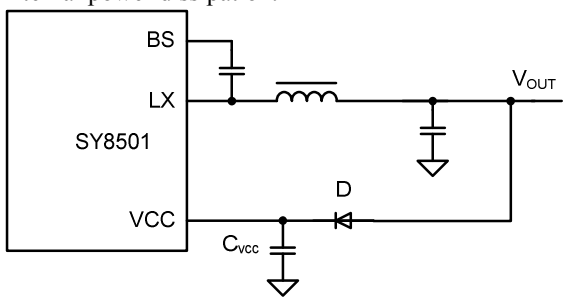
$$F_s(kHz) = \frac{11 \times V_O(V) + 500}{R_{on}(M\Omega)}$$

Notice: Final switch frequency is not only effected by component tolerant but also minimum off and on time limit.

Internal LDO Regulator

The SY8501 consists of two internal LDOs for 4V_VDD from IN pin and VCC pin. Upon power up, the LDO regulator from IN sources current into the capacitor on internal 4V_VDD. When the voltage on the 4V_VDD reaches the under-voltage lockout threshold voltage, the buck switch is enabled. After soft start done and VCC pin voltage is larger than 4.2V, the VCC side LDO is enabled and IN side LDO is disabled. A 0.1uF ceramic capacitor is recommended for C_{VCC} at most applications.

In applications，the input pin (IN) can be connected directly to the line voltages up to 100 Volts, where power dissipation in the VCC regulator is a concern, an auxiliary voltage can be connected to the VCC pin via a diode. Setting the auxiliary voltage to 4.5 -28V will shut off the internal regulator from IN, reducing internal power dissipation.



Soft Start

The SY8501 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC start-up. The typical soft-start time is 2ms.

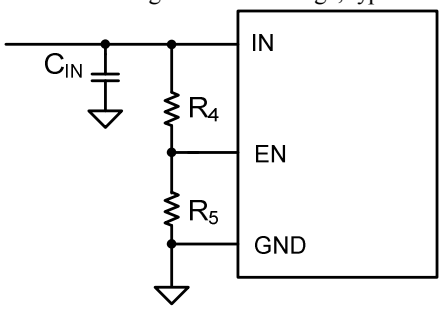
Enable Operation

Pulling the EN pin low will shut down the device. During shut mode, the SY8501 shutdown current drops to lower than 10uA. Driving the EN pin high will turn on the IC again.

Input UVLO can be programmed by EN rising threshold. Minimum V_{UVLO} value need larger than 6.5V

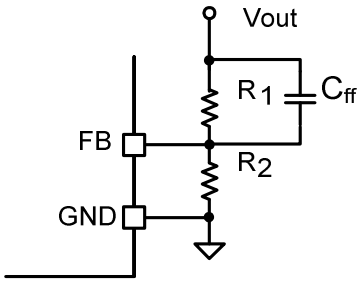
$$V_{UVLO}(V) = (1 + \frac{R_4}{R_5}) \times Vth$$

Vth is EN rising threshold voltage, typical is 1.2V



Load Transient Considerations:

The SY8501 regulator IC adopts the instant PWM architecture to achieve good stability and fast transient responses. Adding a C_{ff} ceramic cap in parallel with R_1 is recommended.



External Boot-strap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.

Over Current Protection

SY8501 provides cycle-by-cycle over current limiting on both high side MOSFET and low-side MOSFET. Under over current condition, if the output voltage drops below 33% of set-point, the device will

fold back valley current limit to 0.5x typical value.

Layout Design:

The layout design of SY8501 is very important for proper operation. Following are the tips for good PCB layout.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

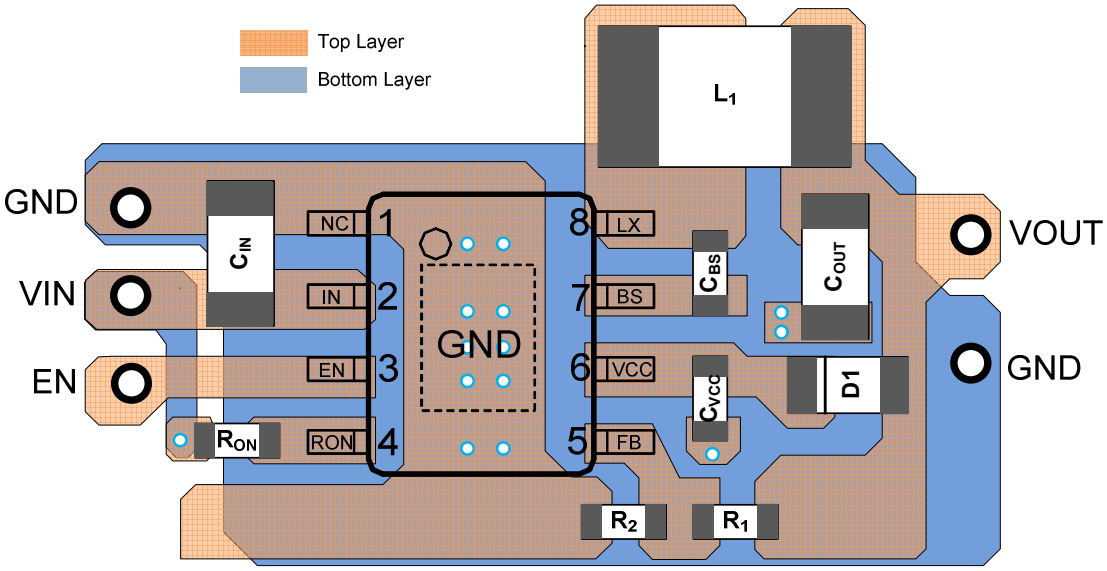
2) C_{IN} must be close to Pin IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) C_{VCC} should be placed close to VCC pin and GND pin.

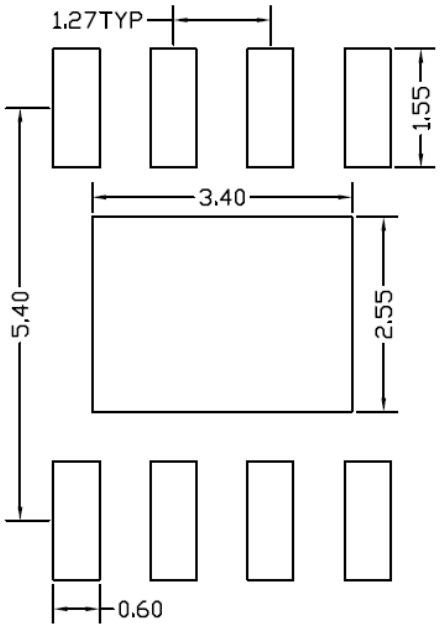
4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

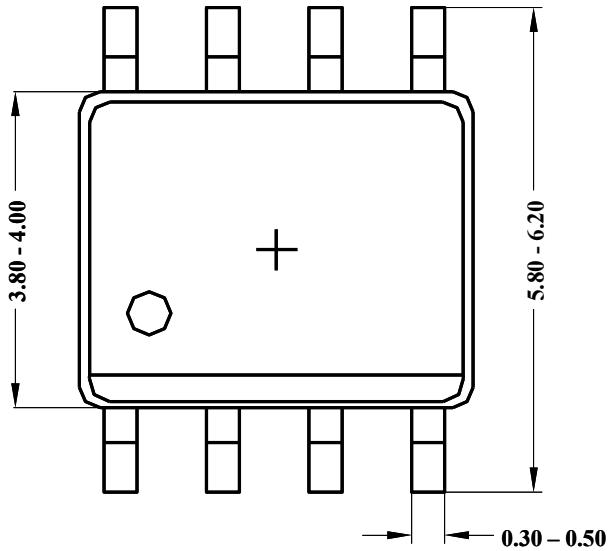
5) The feedback components R_{UP} and R_{DOWN}, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

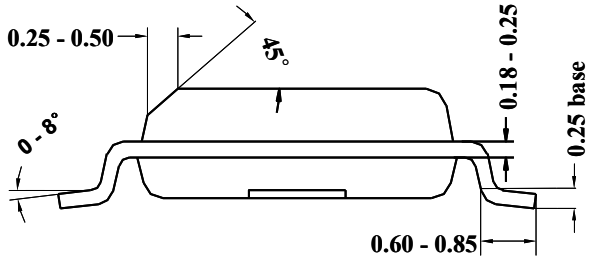


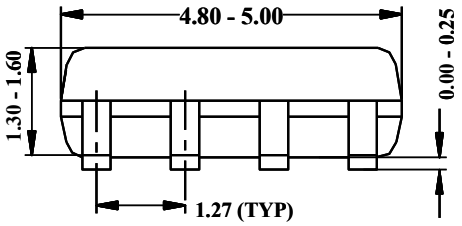
SO8-E Package Outline & PCB layout





Recommended Pad Layout



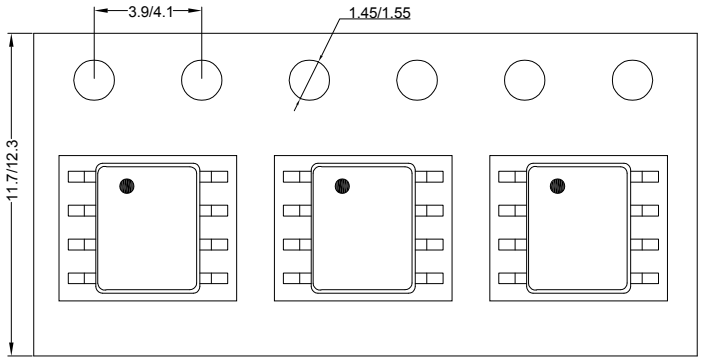


Notes: **All dimension in MM**
All dimension don't not include mold flash & metal burr

Taping & Reel Specification

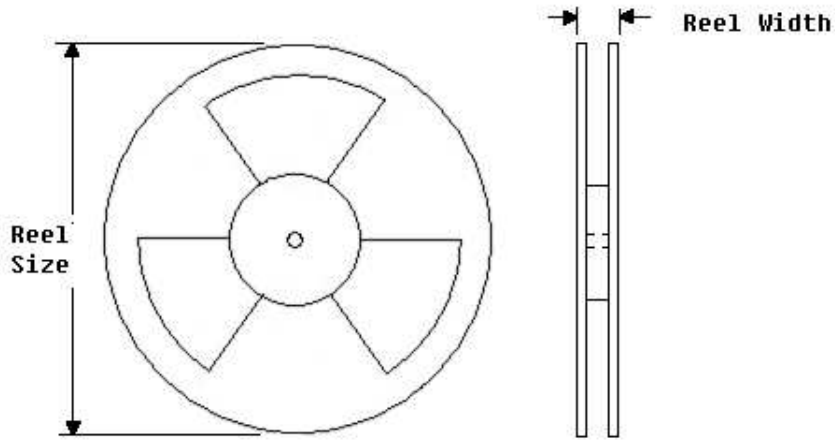
1. Taping orientation

SOP8-EP



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOP8E	12	8	13"	12.4	400	400	2500

3. Others: NA