3.8V-60V Vin, 5A, High Efficiency Step-down DCDC Converter with Programmable Frequency and Soft-start Time

FEATURES

- Wide Input Range: 3.8V-60V
- Up to 5A Continuous Output Current
- 0.8V ±1% Feedback Reference Voltage
- Integrated 80mΩ High-Side
- Ultra low Iq 30uA
- Pulse Skipping Mode (PSM) in light load
- 100ns Minimum On-time
- 4ms Internal Soft-start Time
- Adjustable Frequency 100KHz to 2.5MHz
- External Clock Synchronization
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Derivable Inverting Voltage Regulator
- Over-voltage and Over-Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- 12-V, 24-V, 48-V Industry and Telecom Power System
- Industrial Automation and Motor Control
- Vehicle Accessories

DESCRIPTION

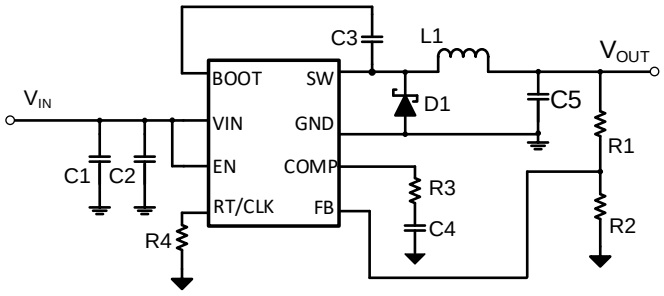
The SCT2650 is 5A buck converters with wide input voltage, ranging from 3.8V to 60V, which integrates a 80mΩ high-side MOSFET. The SCT2650, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2650 features programmable switching frequency from 100 kHz to 2.5 MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 100kHz to 2.5MHz. The SCT2650 allows power conversion from high input voltage to low output voltage with a minimum 100ns on-time of high-side MOSFET.

The device offers programmable soft start to prevent inrush current during the startup of output voltage ramping. Power Good with open drain output signals that the output voltage is within regulation.

The SCT2650 provides cycle-by-cycle current limit, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in a 8-pin ESOP-8 package.

TYPICAL APPLICATION



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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.1: Engineering

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT2650STE	2650	ESOP-8

1) For Tape & Reel, Add Suffix R (e.g. SCT2650STER)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	65	V
BOOT	-0.3	68	V
SW	-1	65	V
BOOT-SW	-0.3	6	V
COMP, FB, RT/CLK	-0.3	6	V
Operating junction temperature TJ(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION

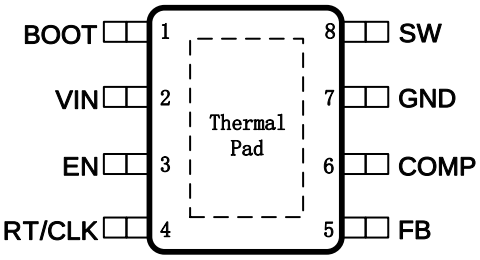

Figure 1. 8-Lead Plastic ESOP

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
BOOT	1	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
VIN	2	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
EN	3	Enable pin to the regulator with internal pull-up current source. Pull below 1.2V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
RT/CLK	4	Set the 20internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency.
FB	5	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
COMP	6	Error amplifier output. Connect to frequency loop compensation network.
GND	7	Ground

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SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.8	60	V
V_{OUT}	Output voltage range	0.8	57	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-10L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	35.1	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	34.1	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2650 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2650. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		3.8		60	V
V_{IN_UVLO}	Input UVLO Threshold Hysteresis	V_{IN} rising		3.5 400	3.7	V mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		2	3	μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		30		μA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		80		mΩ
Reference and Control Loop						
V_{REF}	Reference voltage of FB		0.792	0.8	0.808	V
G_{EA}	Error amplifier trans-conductance	-2μA<I_{COMP}<2μA, V_{COMP}=1V		300		μS

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{COMP_SRC}	EA maximum source current	$V_{FB}=V_{REF}$-100mV, V_{COMP}=1V		30		μA
I_{COMP_SNK}	EA maximum sink current	$V_{FB}=V_{REF}$+100mV, V_{COMP}=1V		30		μA
V_{COMP_H}	COMP high clamp			3		V
V_{COMP_L}	COMP low clamp			0.4		V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold		6.8	8	9.2	A
Enable and Soft Startup						
V_{EN_H}	Enable high threshold			1.2		V
I_{EN_L}	Enable pin pull-up current	EN=1V		1.2		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		3.4		uA
Switching Frequency and External Clock Synchronization						
F_{RANGE_RT}	Frequency range using RT mode		100		2500	kHz
F_{SW}	Switching frequency	R_{RT}=200 kΩ(1%)	450	500	550	kHz
F_{RANGE_CLK}	Frequency range using CLK mode		100		2500	kHz
t_{ON_MIN}	Minimum on-time	V_{IN}=24V		100		ns
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		110 105		% %
V_{BOOTUV}	BOOT-SW UVLO threshold	BOOT-SW falling Hysteresis		2.36 300		V mV
T_{SD}	Thermal shutdown threshold	T_J rising		170		°C

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FUNCTIONAL BLOCK DIAGRAM

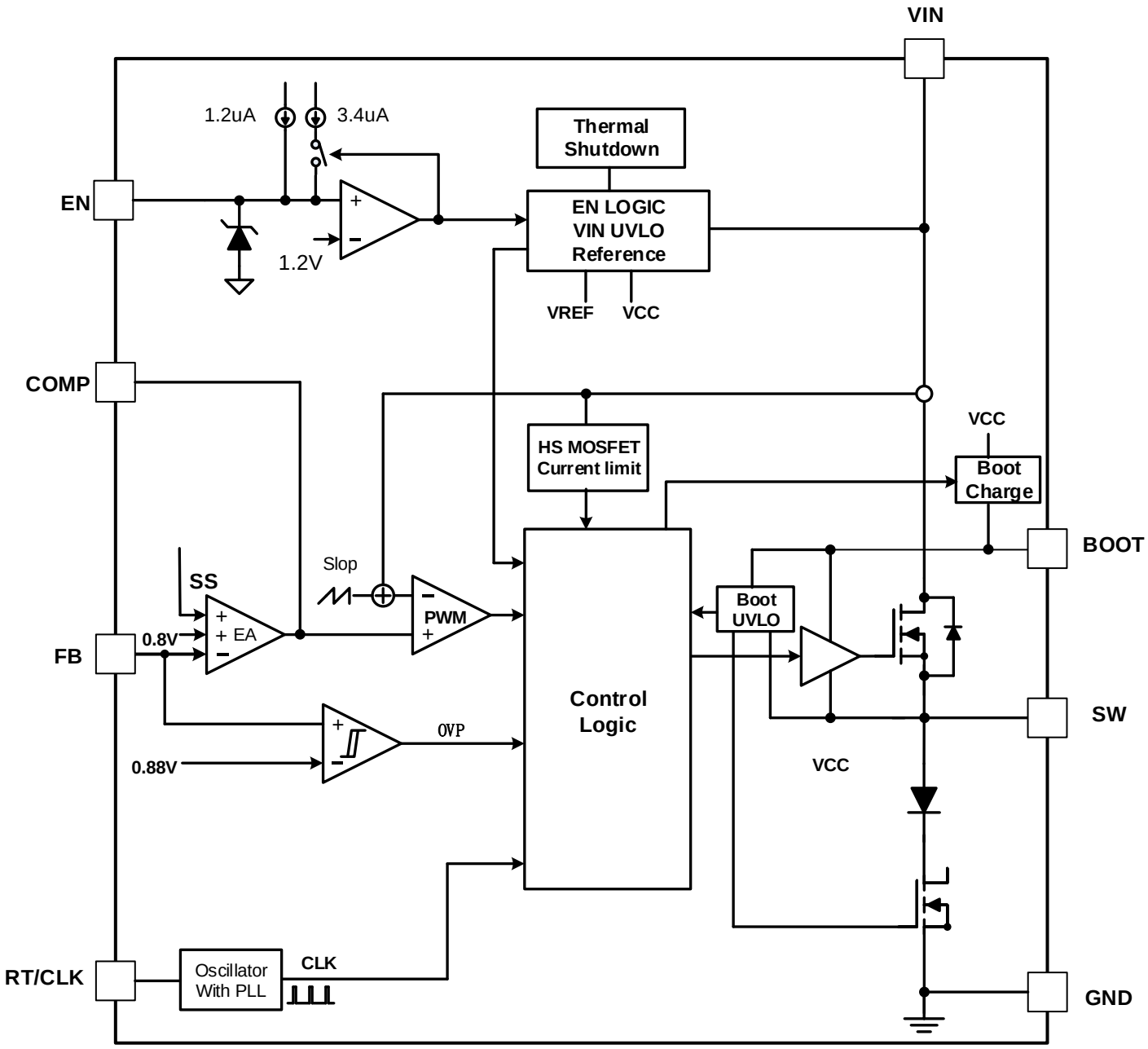

Figure 2. Functional Block Diagram

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OPERATION

Overview

Peak Current Mode Control

Enable and Under Voltage Lockout Threshold

The SCT2650 is enabled when the VIN pin voltage rises about 3.5V and the EN pin voltage exceeds the enable threshold of 1.2V. The device is disabled when the VIN pin voltage falls below 3.1V or when the EN pin voltage is below 1.2V. An internal 1.2uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 15 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$R_1 = \frac{V_{rise} - V_{fall}}{3.4uA} \quad (1)$$

$$R_2 = \frac{1.2}{\frac{V_{rise}-1.2}{R_1} + 1.2uA} \quad (2)$$

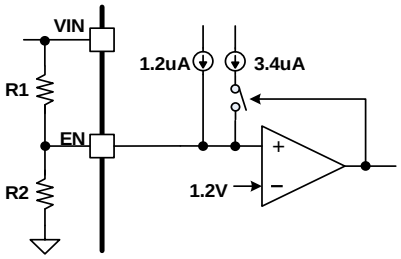

Figure 3. System UVLO by enable divide

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO

Output Voltage

The SCT2650 regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Programmable Soft-Start

The SCT26501 features programmable soft-start time to prevent inrush current during start-up stage. The soft-start time can be programmed easily by connecting a soft-start capacitor C_{ss} (C_{ss} is the C13 on Figure 18) from SS pin to ground.

The SS pin sources an internal 3μA current charging the external soft-start capacitor C_{ss} when the EN pin exceeds turn-on threshold. The device adopts the lower voltage between the internal voltage reference 0.8V and the SS pin voltage as the reference input voltage of the error amplifier and regulates the output. The soft-start completes when the voltage at the SS pin exceeds the internal reference voltage of 0.8V.

The soft-start capacitor value can be calculated going with following Eq. (4). Attention should be taken here that the programmed soft-start time should be larger than 4ms.

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$$C_{soft-start} = t_{ss} * \frac{3uA}{0.8V} \quad (4)$$

Where:

- C_{SS} is the soft-start capacitor connected from SS pin to the ground
- t_{ss} is the soft-start time

Switching Frequency and Clock Synchronization

The switching frequency of the SCT2650 is set by placing a resistor between RT/CLK pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT/CLK pin to the ground sets the switching frequency over a wide range from 100KHz to 2.5MHz. The RT/CLK pin voltage is typical 0.5V. RT/CLK pin is not allowed to be left floating or shorted to the ground. Use Equation 5 or the plot in Figure 16. to determine the resistance for a switching frequency needed.

$$RT(K\Omega) = \frac{100000}{fsw(KHz)} \quad (5)$$

where, fsw is switching clock frequency

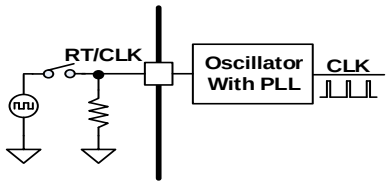

Figure 4. Setting Frequency and Clock Synchronization

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT/CLK pin. The synchronization frequency range is from 100KHz to 2.5MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at RT/CLK pin with typical 66ns time delay. A square wave clock signal to RT/CLK pin must have high level no lower than 2V, low level no higher than 0.4V, and pulse width larger than 80ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown in Figure 16. Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Over Current Limit

Fold back current limit

Over voltage Protection

Thermal Shutdown

The SCT2650 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 170C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 150C, the device restarts with internal soft start phase.

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Layout Guideline

Proper PCB layout is a critical for SCT2650's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
7. UVLO adjust and RT resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
8. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.
9. For achieving better thermal performance, a four-layer layout is strongly recommended.

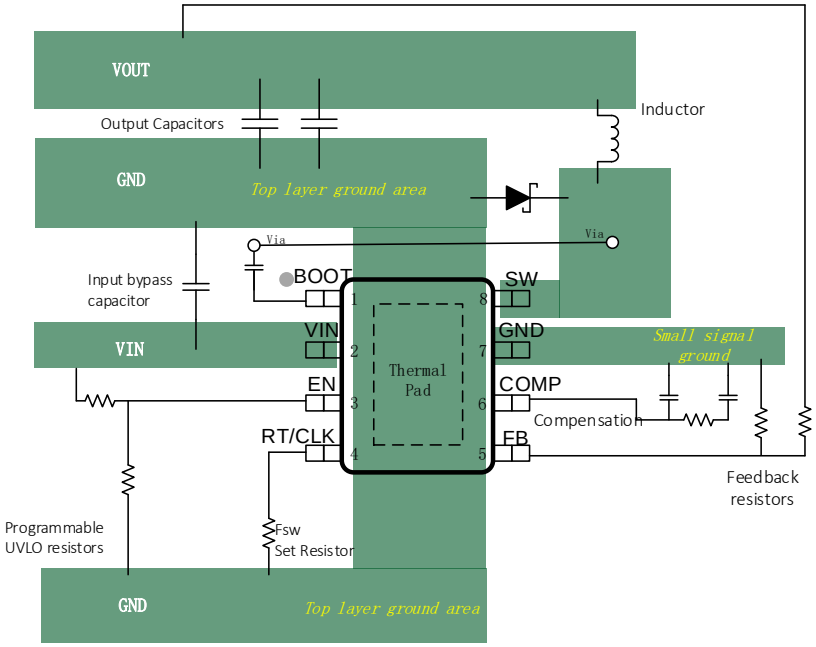

Figure 26. PCB Layout Example

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