SY7069B

5.5V Maximum Output, 3A Valley Current, 1MHz Synchronous Boost with Auto Bypass Function

General Description

SY7069B is a high efficiency synchronous, step-up Boost converter designed for one-cell Li-Ion or Li-polymer, or a two to three-cell alkaline Ni-Cd or Ni-MH battery powered applications. It can convert down to 2.5V input voltage and up to 5.5V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch.

SY7069B can disconnect the output from input during the shutdown mode. When input voltage exceeds the regulated output voltage, SY7069B enters bypass mode automatically.

Features

- 2.5V Minimum Input Voltage
- Adjustable Output Voltage from 2.5V to 5.5V
- Min 3A Valley Current Limit
- Capable for Seamless Transition between Boost and Bypass Mode
- Load Disconnect During Shutdown
- Low $R_{DS(ON)}$ (Main Switch/Synchronous Switch) at 5.0V Output: 50mΩ/90mΩ
- Output OVP Protection
- Compact package TSOT23-6

Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment.

Ordering Information

SY7069 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7069BADC	TSOT23-6	----

Typical Applications

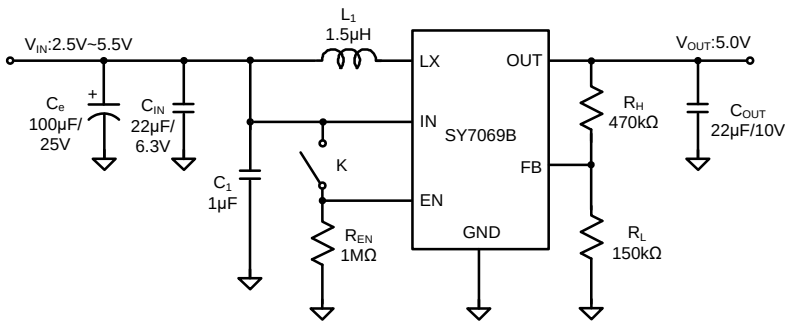


Figure 1. Schematic Diagram

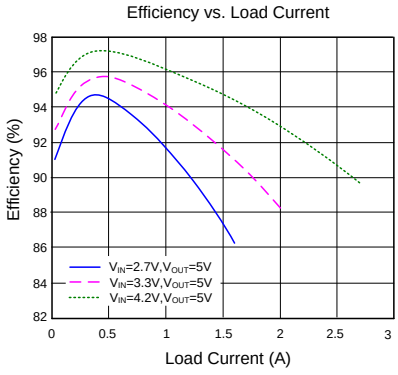
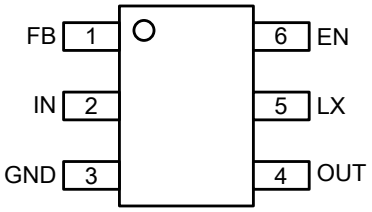


Figure2. Efficiency vs. Load Current

Pinout (top view)



(TSOT23-6)

Top mark: **bD*xyz*** (Device code: bD, ***x=year code, y=week code, z= lot number code*****)**

Name	Pin Number	Description
FB	1	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=1.2× (1+R_H/R_L).
IN	2	Signal input pin. Decouple this pin to GND pin with at least a 1μF ceramic capacitor for noise immunity consideration.
GND	3	Ground pin.
OUT	4	Output pin. Decouple this pin to GND pin with at least a 22μF ceramic capacitor.
LX	5	Inductor node. Connect an inductor between the IN pin and the LX pin.
EN	6	Enable pin. Pull high to turn on. Do not leave it floating.

Block Diagram

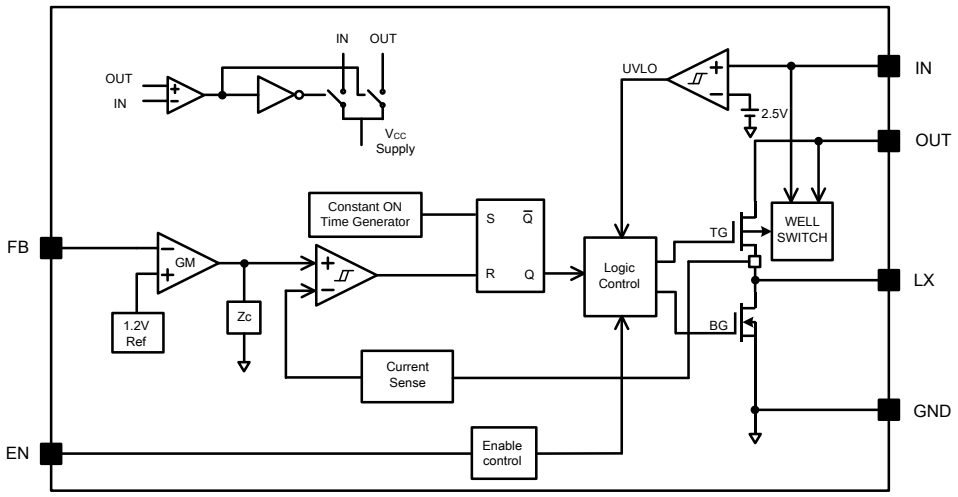


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

All Pins ---------- 6.0V
Power Dissipation, P_D@ T_A=25°C, TSOT23-6----------1.92W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 52°C/W
θ_{JC} ---------- 32°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- 65°C to 150°C

Recommended Operating Conditions (Note 3)

IN ---------- 2.5V to 5.5V
OUT---------- 2.5V to 5.5V
EN, FB ---------- 0V to V_{OUT}+0.3V
All other pins ---------- 0-5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} =3.0V, V_{OUT}=5.0V, I_{OUT}=500mA, T_A = 25°C unless otherwise specified)

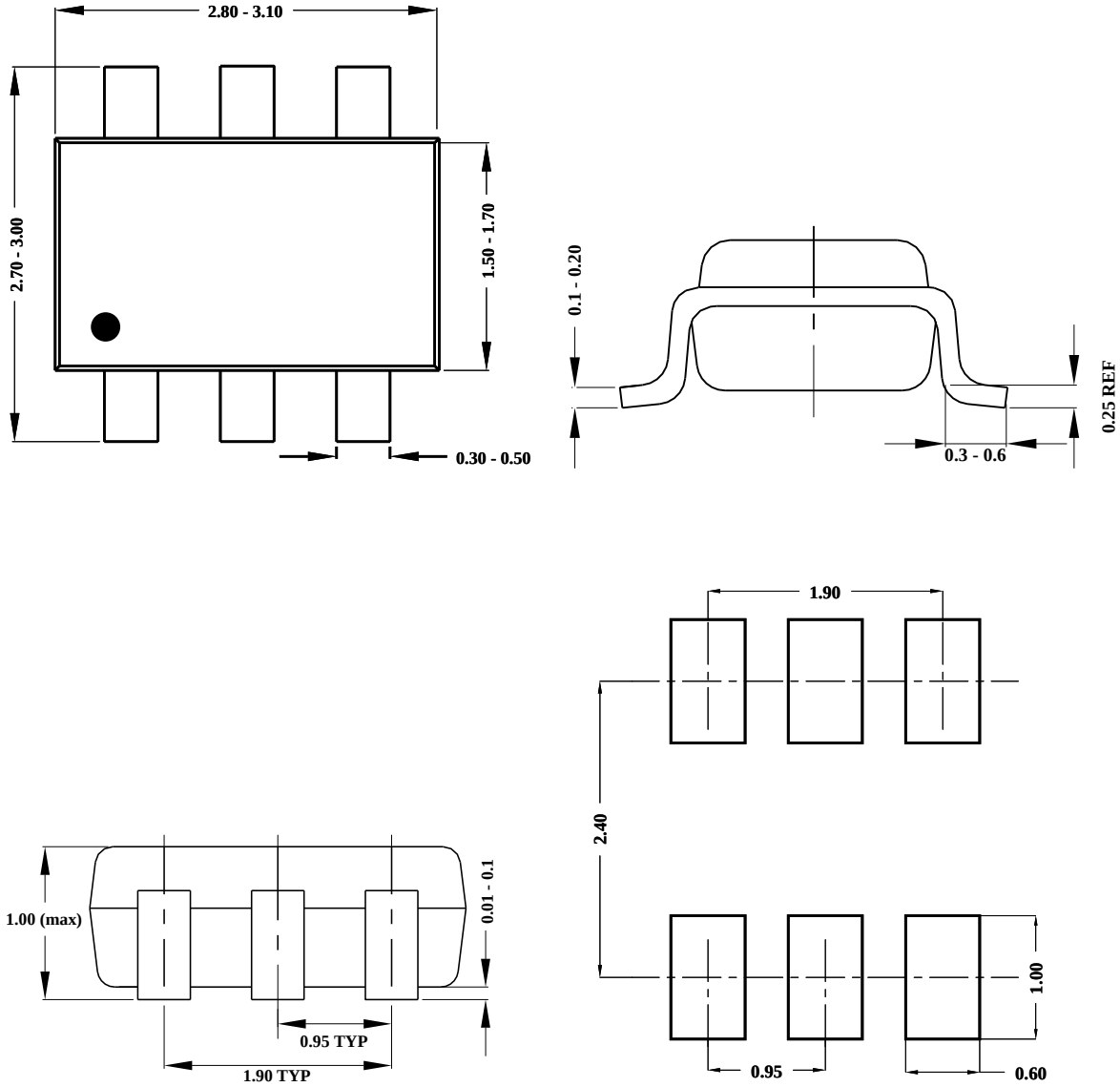
Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		2.5		5.5	V
Output Voltage Range		V_{OUT}		2.5		5.5	V
Quiescent Current	V_{IN}	I_Q	Io=0A,V_{EN}=V_{IN}=3.0V,		8		μA
	V_{OUT}		V_{OUT}=5.0V,V_{FB}=105%V_{REF}		32		μA
Shutdown Current		I_{SHDN}	V_{EN}=0V, V_{IN}=3.0V		0.1	1	μA
Linear Charge Current		I_{CHARGE}	V_{OUT}<0.5V_{IN}		1.5		A
Input Vin UVLO Threshold		V_{UVLO}				2.5	V
V_{IN} UVLO Hysteresis		V_{SYS}			0.1		V
EN Rising Threshold		V_{ENH}		1.2			V
EN Falling Threshold		V_{ENL}				0.4	V
Low Side Main FET R_{ON}		$R_{DS(ON)1}$	V_{OUT}=5.0V		50		mΩ
Synchronous FET R_{ON}		$R_{DS(ON)2}$	V_{OUT}=5.0V		90		mΩ
Synchronous FET Current Limit		I_{LIM}		3.0			A
Switching Frequency		Fsw			1.0		MHz
Feedback Reference Voltage		V_{REF}		1.182	1.2	1.218	V
Minimum ON Time		t_{ON_MIN}			80		ns
Minimum OFF Time		t_{OFF_MIN}			80		ns
OUT Pin OVP Protection					6.0		V
OUT Pin OVP Hysteresis		OVP_{HYS}			0.25		V
Thermal Shutdown Temperature		T_{SD}			150		°C
Thermal Shutdown Hysteresis		T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

TSOT23-6 Package outline & PCB layout



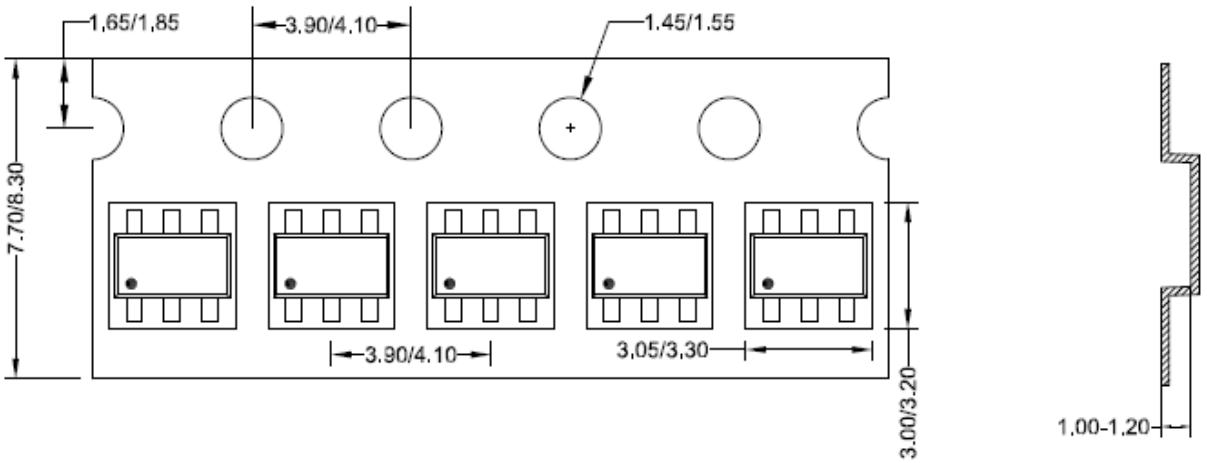
Recommended Pad Layout

Notes: **All dimensions are in millimeters**
All dimensions don't include mold flash & metal burr

Taping & Reel Specification

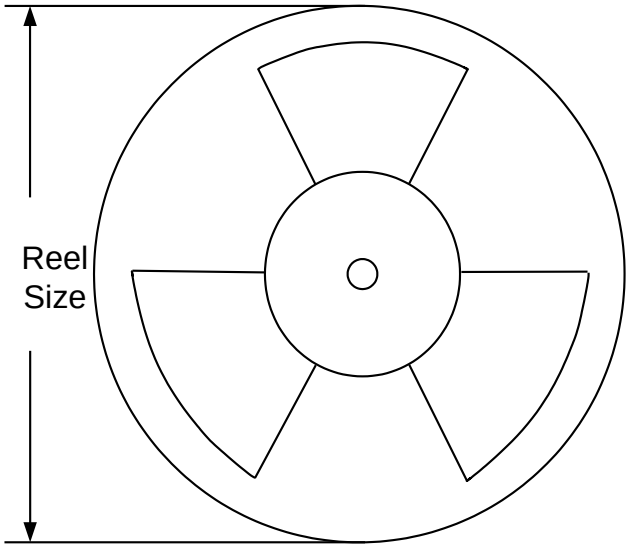
1. Taping orientation

TSOT23-6



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-6	8	4	7	400	160	3000

3. Others: NA