LV2841/2

High Efficiency Wide Input Voltage Range Buck Regulator

Description

The LV2841 and LV2842 are PWM DC/DC buck (step-down) regulators. With a wide input range from 4V-40V, they are suitable for a wide range of application from industrial to automotive for power conditioning from unregulated source. An ultra low 1uA current can further prolong battery life in shutdown mode. Operating frequency is fixed at 1.1MHz(X version) and 2.1MHz(Y version) allowing the use of small external components while still being able to have low output ripple voltage. Soft-start and compensation circuits are implemented internally, and these allow the device to be used with minimized external components.

The LV2842 is optimized for up to 600mA load currents while the LV2841 is optimized for up to 300mA load current. They all have a 0.765V nominal feedback voltage.

The device has built-in protection features such as pulse by pulse current limit, thermal sensing and shutdown due to excessive power dissipation. The LV2841 and LV2842 are available in a low profile TSOT-6L package.

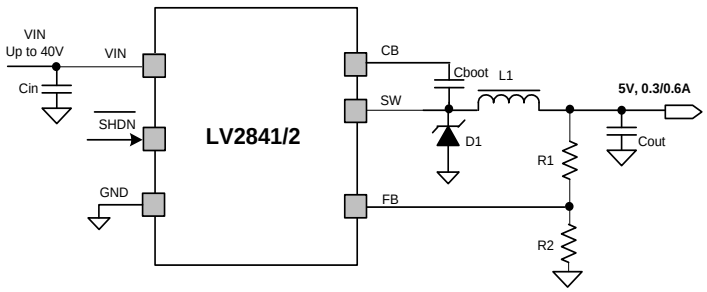
Applications

- Power Meter
- Collector
- Concentrator
- Industrial Distributed Power Applications

Features

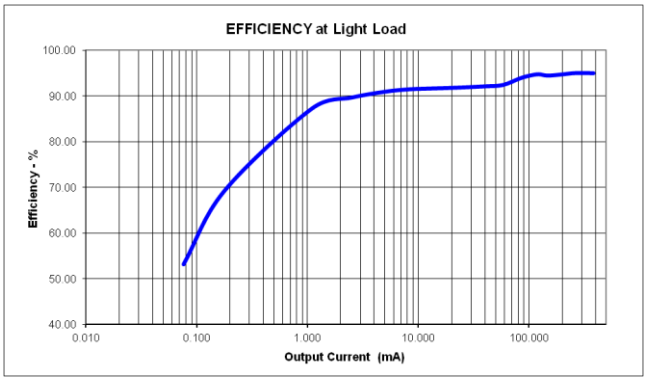
- **Input Range 4V to 40V with 45V Transients**
- **1.1MHz(X) or 2.1MHz(Y) Switching Frequency**
- **Ultra High Efficiency for Light Load with Eco Mode**
- **Low Dropout Operation**
- **Output Current Options of 300mA and 600mA**
- **High Voltage Precision Enable Input**
- Over Current Protection
- Over Temperature Protection
- Internal Compensation
- Soft Start Circuitry
- Small Overall Solution Size (TSOT-6L Package)

Typical Application Circuit



Efficiency vs. Light Load Current

(Fsw=1.1MHz, Vin=18V/Vout=12V)



Part Ordering Information

X=1.1MHz, Y=2.1MHz Switching frequency

Order Number	Package	Supplied As
LV2842XLVDDCT	TSOT-6	250 Units on Tape and Reel
LV2842XLVDDCR		3000 Units on Tape and Reel
LV2842YDDCT		250 Units on Tape and Reel
LV2842YDDCR		3000 Units on Tape and Reel

ABSOLUTE MAXIMUM RATINGS [(1)]

NO.	DESCRIPTION		VALUE	UNIT
1.1	VIN, /SHDN	Unregulated inputs	45	V
1.2	FB	Sense voltage for error amplifiers	7	V
1.3	SW	Switch point for buck converter	45 -2V for 30nS	V
1.4	CB	Bootstrap capacitor voltage	50	V
1.5	ESD	Electrostatic Discharge HBM	2	kV
1.6	Top	Operating ambient temperature	-40 to 125	℃
1.7	T_S	Storage Temperature Range	-55 to 165	℃
1.8	T_J	Operating junction temperature range	-40 to 150	℃

Note (1): Stresses at or beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC		VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	102	℃/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	36.9	
θ_{JB}	Junction-to-board characterization parameter	28.4	

RECOMMEDED OPERATING CONDITIONS

FUNCTION	TERMINAL	VALUE	UNIT
Buck Regulator	VIN	4 to 40	V
	CB	3.8 to 45	V
	SW	-1 to 40	V
	FB	0 to 5	V
Control	/SHDN	0 to 40	V

Electrical characteristics

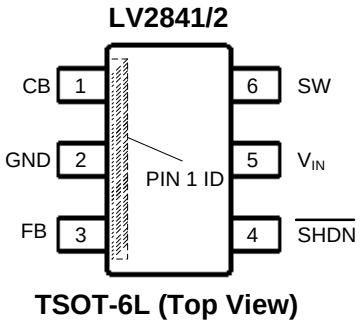
VIN = 6V to 27V, /SHDN = VIN, T_A = 25℃, unless otherwise noted.

1.0	PARAMETER	TEST CONDITIONS		Min	Typ	Max	Unit
1.1	**VIN (Input Power Supply)**						
1.2	Operating input voltage			4		40	V
1.3	Shutdown supply current	EN = 0 V			1	2	µA
1.4	Undervoltage lockout thresholds	Rising				4	V
1.5		Falling		3			
1.6	Device on : not switching	Eco mode, no load, VIN = 12 V			30		µA
1.7	**ENABLE AND UVLO(/SHDN PIN)**						
1.8	Enable Threshold voltage			1.05	1.25	1.38	V
1.9	Input current	Enable threshold + 50 mV			-4.2		µA
1.10		Enable threshold - 50 mV			-1		
1.11	Hysteresis current				-3		µA
1.12	**HIGH-SIDE MOSFET**						
1.13	On-resistance	VIN = 12 V, CB2SW=5.8V			500		mΩ
1.14	t_{ON-min}	fsw = 2.1MHz			95		ns
1.15	D_{MAX} : Maximum duty cycle	LV2841/2 X			96		%
1.16		LV2841/2 Y			97		
1.17	V_{FB} : Feedback voltage			0.746	0.765	0.784	V
1.18	**CURRENT LIMIT**						
1.19	Current limit threshold	VIN = 12 V	LV2841		600		mA
			LV2842		1200		mA
1.20	f_{SW} Switching frequency	LV2841/2X		830	1100	1580	kHz
1.21		LV2841/2Y		1680	2100	2520	kHz
1.22	**Thermal Performance**						
1.23	$T_{SHUTDOWN}$ Thermal shutdown trip point				170		℃
1.24	T_{hys}	Hysteresis			10		℃

Pin Configuration

DDC PACKAGE

(TOP VIEW)



TSOT-6L (Top View)

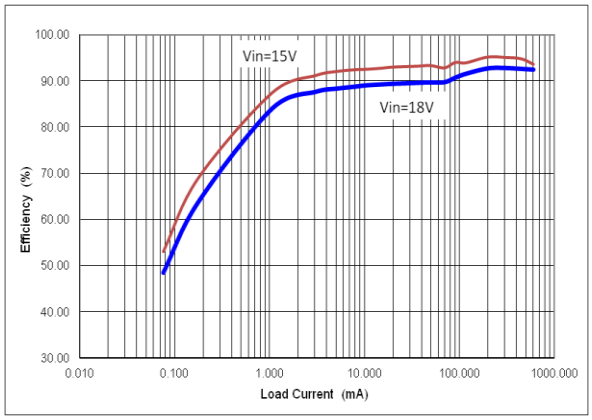
PIN FUNCTIONS

Name	NO.	I/O	Description
CB	1	O	SW FET Gate Bias voltage. Connect Cboot cap between CB and SW
GND	2	-	Ground Connection
FB	3	I	Feedback Pin: Set feedback voltage divider ratio with $V_{OUT} = V_{FB}$ (1+(R1/R2))
/SHDN	4	I	Enable and disable input pin(high voltage tolerant). Internal pull-up current source. Pull below 1.25V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
VIN	5	I	Power input voltage pin: Input for internal supply and drain node input for internal high-side MOSFET
SW	6	I	Switch node, Connect to inductor, diode, and Cboot cap

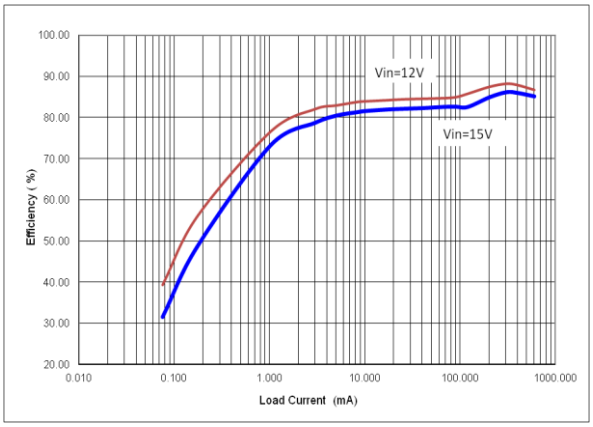
TYPICAL CHARACTERISTICS

Unless otherwise specified the following conditions apply: Vin = 12V, Fsw=2.1MHz, T_A = 25℃.

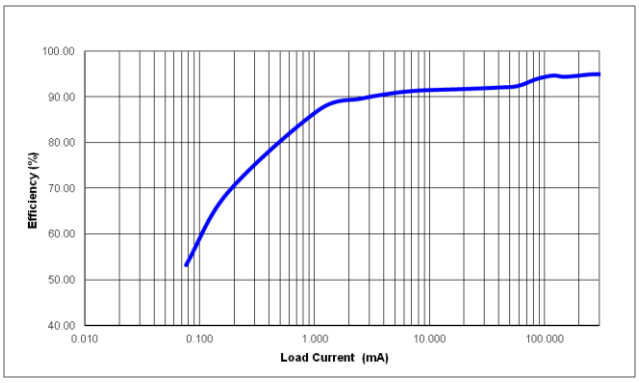
Efficiency vs. Load Current
(Fsw=2.1MHz, Vout=12V)



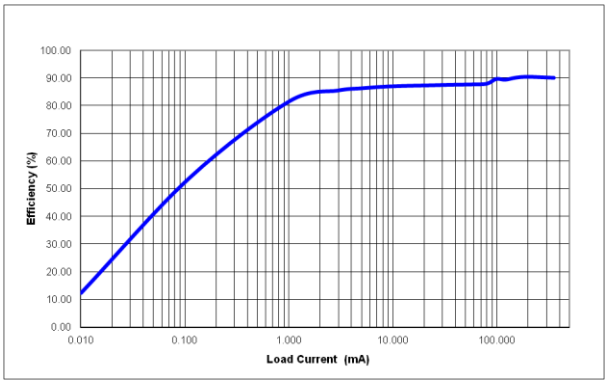
Efficiency vs. Load Current
(Fsw=2.1MHz, Vout=5V)



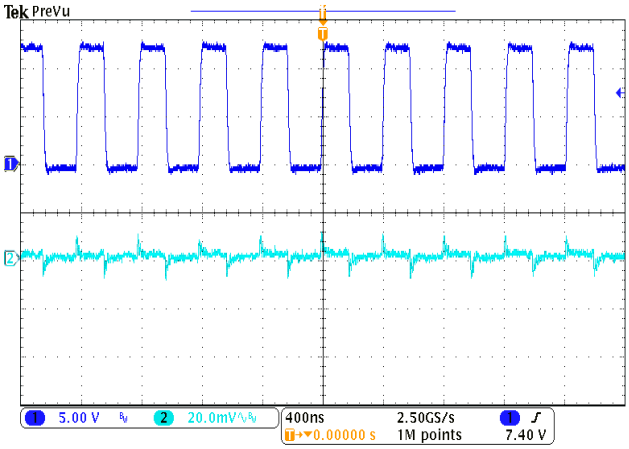
Efficiency vs. Load Current
(Fsw=1.1MHz, Vin=18V/Vout=12V)



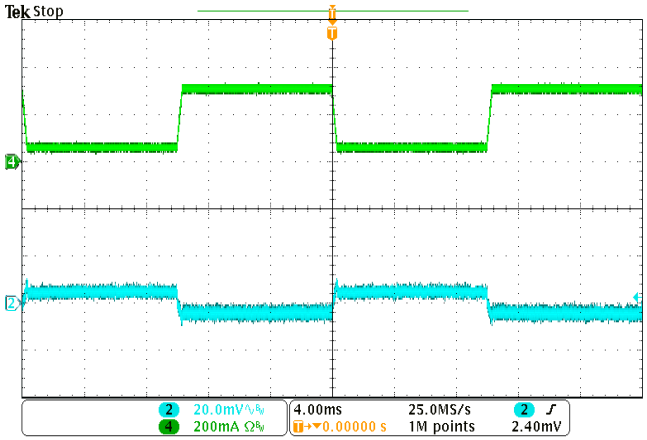
Efficiency vs. Load Current
(Fsw=1.1MHz, Vin=12V/Vout=5V)



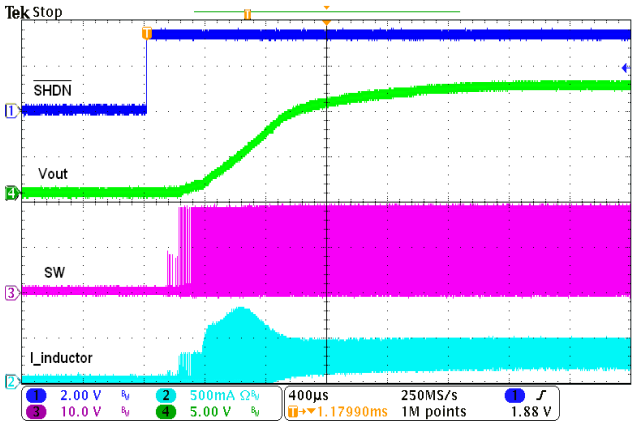
Switching Node and Output Voltage Waveform (300mA)



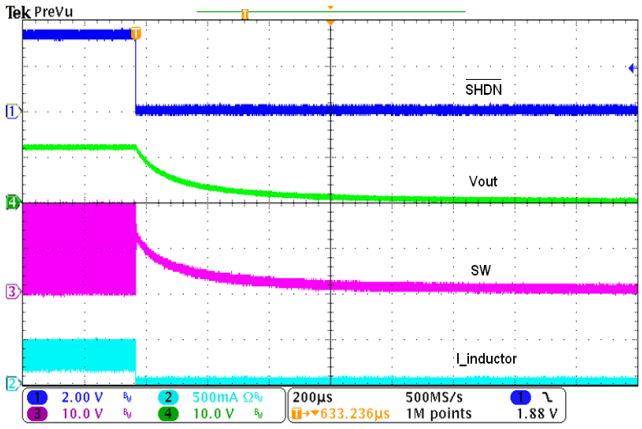
Load Transient Waveform (50mA to 300mA)



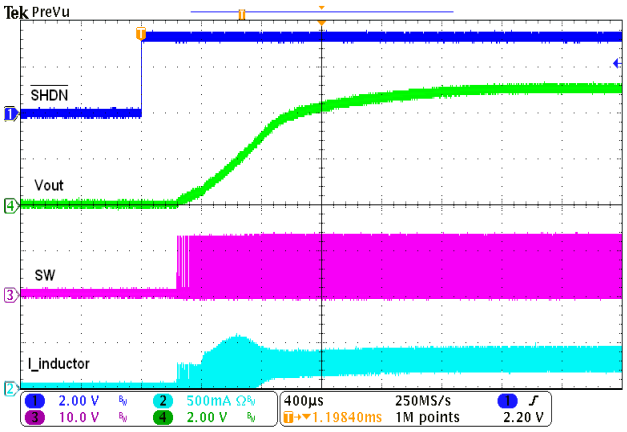
Start-up Waveform (12V/300mA)



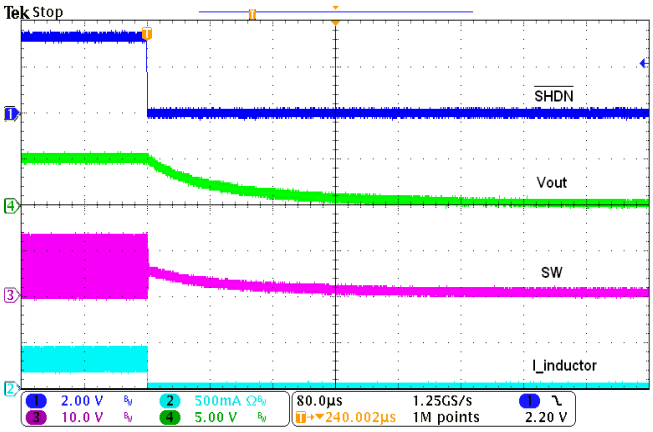
Shutdown Waveform (12V/300mA)



Start-up Waveform (5V/300mA)



Shutdown Waveform (5V/300mA)

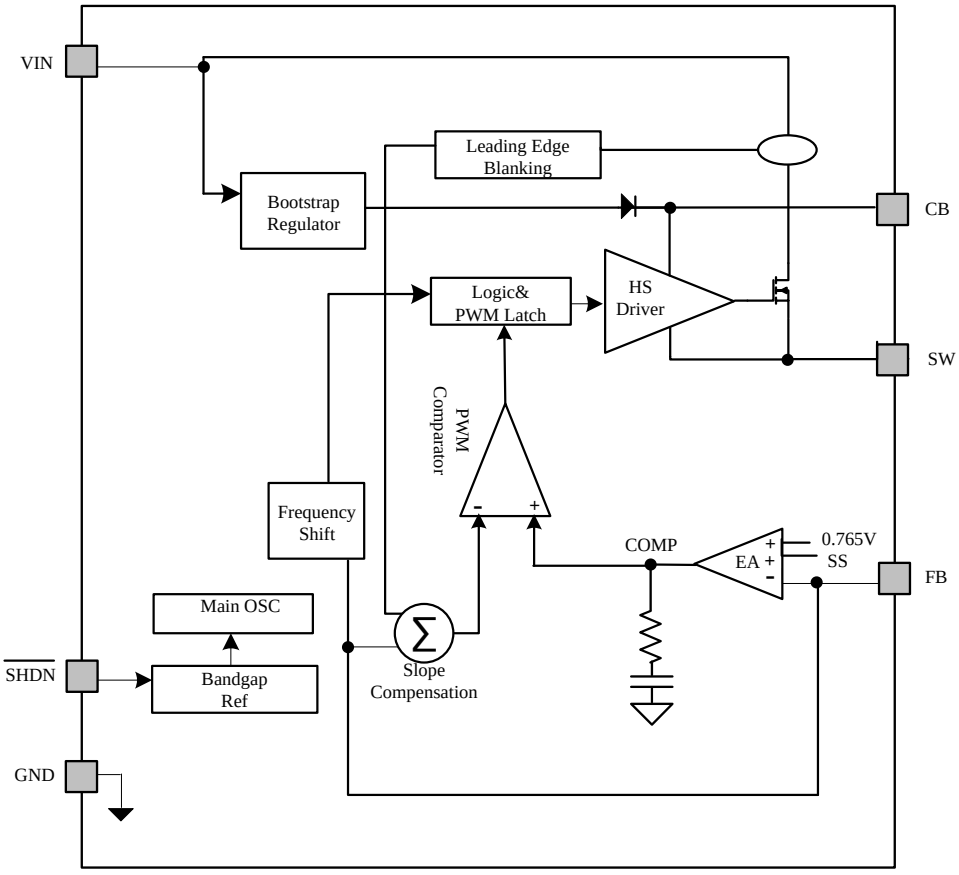


DETAILED DESCRIPTION

The LV2841/2 device is a 40V, 300mA/600mA, step-down (buck) converter. The buck regulator has a very low quiescent current during the light load to prolong the battery life.

For LV2841/2, to improve performance during line and load transients it implements a constant frequency, current mode control which reduces output capacitance and simplifies frequency compensation design. Two switching frequency options, 1.1MHz and 2.1MHz, are available, thus smaller inductor and capacitor can be used. The LV2841/2 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the CB to SW pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The LV2841/2 can operate at high duty cycles because of the boot UVLO and refresh wimp FET. The output voltage can be stepped down to as low as the 0.8V reference. Internal soft start is featured to minimize inrush currents.

INTERNAL FUNCTIONAL BLOCKS



Continuous Conduction Mode

The LV2841/2 steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the buck regulator operates in two cycles. The power switch is connected between VIN and SW. In the first cycle of operation the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by Cout and the rising current through the inductor. During the second cycle the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as: D=VOUT/VIN and D' = (1-D) where D is the duty cycle of the switch, D and D' will be required for design calculations.

Fixed Frequency PWM Control

The LV2841/2 has two fixed frequency options, and it implements peak current mode control. The output voltage is compared through external resistors on the VFB pin to an internal voltage reference by an error amplifier which drives the internal COMP node. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch is turned off. The internal COMP node voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

Sleep Mode

The LV2841/2 operates in sleep mode at light load currents to improve efficiency by reducing switching and gate drive losses. The LV2841/2 is designed so that if the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the sleep current threshold, the device enters sleep mode. For sleep mode operation, the LV2841/2 senses peak current, not average or load current, so the load current where the device enters sleep mode is dependent on the output inductor value. When the load current is low and the output voltage is within regulation, the device enters a sleep mode and draws only 30uA input quiescent current.

When in sleep mode, the COMP node voltage is clamped at 500mV and the high side MOSFET is inhibited. Further decreases in load current or in output voltage cannot drive the COMP node below this clamp voltage level.

Since the device is not switching, the output voltage begins to decay. As the voltage control loop compensates for the falling output voltage, the COMP node voltage begins to rise. At this time, the high side MOSFET is enabled and a switching pulse initiates on the next switching cycle. The peak current is set by the COMP node voltage. The output voltage re-charges the regulated value, then the peak switch current starts to decrease, and eventually falls below the sleep mode threshold at which time the device again enters sleep mode.

Bootstrap Voltage (CB)

The LV2841/2 has an integrated boot regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high side MOSFET. The CB capacitor is refreshed when the high side MOSFET is off and the low side diode conducts.

To improve drop out, the LV2841/2 is designed to operate at 100% duty cycle as long as the CB to SW pin voltage is greater than 2.1V. When the voltage from CB to SW drops below 2.1V, the high side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the CB capacitor. Since the supply current sourced from the CB capacitor is low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low side diode and printed circuit board resistance. During operating conditions in which the input voltage drops and the regulator is operating in continuous conduction mode, the high side MOSFET can remain on for 100% of the duty cycle to maintain output regulation, until the CB to SW voltage falls below 2.1V.

Attention must be taken in maximum duty cycle applications which experience extended time periods with light load or no load. When the voltage across the CB capacitor falls below the 2.1V UVLO threshold, the high side MOSFET is turned off, but there may not be enough inductor current to pull the SW pin down to recharge the CB capacitor. The high side MOSFET of the regulator stops switching because the voltage across the CB capacitor is less than 2.1V. The output capacitor then decays until the difference in the input voltage and output voltage is greater than 2.1V, at which point the CB UVLO threshold is exceeded, and the device starts switching again until the desired output voltage is reached. This operating condition persists until the input voltage and/or the load current increases. To charge the CB capacitor when LV2841/2 tries to turn on the high side MOSFET continuously, during the high side off state the internal small low side MOSFET will be turned on for a short time. Then the SW node will be pulling low to recharge the CB capacitor for maximum duty cycle operation.

Set the output voltage

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown on the front page schematic. The feedback pin voltage 0.765V, so the ratio of the feedback resistors sets the output voltage according to the following equation: Vout=0.765V (1+(R1/R2)) Typically R2 will be given as 1kΩ - 100kΩ for a starting value. To solve for R1 given R2 and Vout uses R1=R2 ((Vout/0.765V)-1).

Enable (/SHDN) and VIN Under Voltage Lockout

LV2841/2 /SHDN pin is a high voltage tolerant input with an internal pull up circuit. The device can be enabled even if the /SHDN pin is floating. The regulator can also be turned on using 1.23V or higher logic signals. If the use of a higher voltage is desired due to system or other constraints it may be used, a 100kΩ or larger resistor is recommended between the applied voltage and the /SHDN pin to protect the device. When /SHDN is pulled down to 0V, the chip is turned off and enters the lowest shutdown current mode. In shutdown mode the supply current will be decreased to approximately 1uA. If the shutdown function is not to be used the /SHDN pin may be tied to VIN. The maximum voltage to the SHDN pin should not exceed 40V.

LV2841/2 has an internal UVLO circuit to shutdown the output if the input voltage falls below an internally fixed UVLO threshold level. This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator will power up when the input voltage exceeds the voltage level. If there is a requirement for a higher UVLO voltage, the /SHDN can be used to adjust the input voltage UVLO by using external resistors.

Current Limit

The LV2841/2 implements current mode control which uses the internal COMP voltage to turn off the high side MOSFET on a cycle by cycle basis. Each cycle the switch current and internal COMP voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

Overvoltage Transient Protection

The LV2841/2 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will respond by clamping the error amplifier output to a high voltage. Thus, requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low value output capacitor, by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 108% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold, the high side MOSFET is allowed to turn on at the next clock cycle.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170℃(typ). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160℃(typ), the device reinitiates the power up sequence.

APPLICATION INFORMATION

Design Guide – Step By Step Design Procedure

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level:

Input Voltage, V_{IN}		9V to 16V, Typical 12V
Output Voltage, V_{OUT}		5.0V ±3%
Maximum Output Current Example I_{O_max}		0.6A
Minimum Output Current Example I_{O_min}		0.03A
Transient Response 0.03A to 0.6A		5%
Output Voltage Ripple		1%
Switching Frequency f_{SW}		2.1MHz
Target during Load Transient	Over Voltage Peak Value	106% of Output Voltage
	Under Voltage Value	91% of Output Voltage

Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for

lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage and the output voltage and the frequency shift limitation. For this example, the output voltage is 5V and the maximum input voltage is 16 V, a switching frequency of 2100 kHz is used.

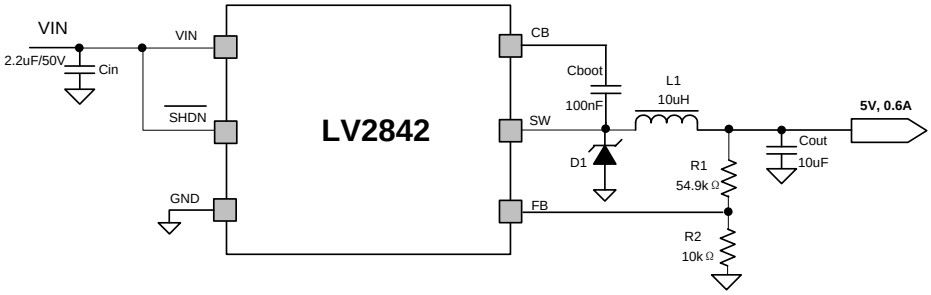


FIGURE 1. Application Circuit, 5V Output

Output Inductor Selection

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. To calculate the minimum value of the output inductor, use Equation 1. A reasonable value is setting the ripple current to be 30% of the DC output current. For this design example, the minimum inductor value is calculated to be 9.1 µH, and a nearest standard value was chosen: 10 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 3 and Equation 4. The inductor ripple current is 0.16A, and the RMS current is 0.602A. As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. A good starting point for most applications is a 10µH with 1A current rating. Using a rating near 1A will enable the LV2841/2 to current limit without saturating the inductor. This is preferable to the LV2841/2 going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other long-term overload.

$$L_{o\min} = \frac{V_{in\max} - V_{out}}{I_o \times K_{IND}} \times \frac{V_{out}}{V_{in\max} \times f_{sw}} \quad (1)$$

$$I_{ripple} = \frac{V_{out} \times (V_{in\max} - V_{out})}{V_{in\max} \times L_o \times f_{sw}} \quad (2)$$

$$I_{L-RMS} = \sqrt{I_o^{\,2} + \frac{1}{12} I_{ripple}^{\,2}} \quad (3)$$

$$I_{L-peak} = I_o + \frac{I_{ripple}}{2} \quad (4)$$

Output Capacitor Selection

The selection of Cout is mainly driven by three primary considerations. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 5 shows the minimum output capacitance necessary to accomplish this. For this example, the transient load response is specified as a 3% change in Vout for a load step from 0.03 A to 0.6 A (full load). For this example, ΔIout = 0.6 -0.03 = 0.57 A and ΔVout = 0.03 × 5 = 0.15 V. Using these numbers gives a minimum capacitance of 3.6 µF. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. Equation 6 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the final peak output voltage, and V_i is the initial capacitor voltage. For this example, the worst case load step will be from 0.6 A to 0.03 A. The output voltage will increase during this load transition and the stated maximum in our specification is 3 % of the output voltage. This will make Vo_overshoot = 1.03 × 5 = 5.15V. V_i is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 6 yields a minimum capacitance of 2.36 µF.

Equation 7 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vo_ripple is the maximum allowable output voltage ripple, and I_L_ripple is the inductor ripple current. Equation 7 yields 0.21 µF.

Equation 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 8 indicates the ESR should be less than 277 mΩ.

Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which will increase this minimum value. For this example, 10µF ceramic capacitors will be used. Capacitors in the range of 4.7µF-100 µF are a good starting point with an ESR of 0.1Ω or less.

$$C_{out} > \frac{2 \times \Delta I_{out}}{fsw \times \Delta V_{out}} \tag{5}$$

$$C_{out} > L_O \times \frac{(Ioh^2 - Iol^2)}{(Vf^2 - Vi^2)} \tag{6}$$

$$C_{out} > \frac{1}{8 \times fsw} \times \frac{1}{\frac{V_{o\_ripple}}{I_{L\ -ripple}}} \tag{7}$$

$$R_{ESR} < \frac{V_{o\_ripple}}{I_{L\ -ripple}} \tag{8}$$

Schottky Diode Selection

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. The current rating for the diode should be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with

a lower average current rating, approximately (1-D)×I_{OUT} however the peak current rating should be higher than the maximum load current. A 0.5 to 1A rated diode is a good starting point.

Input Capacitor Selection

A low ESR ceramic capacitor is needed between the V_{IN} pin and ground pin. This capacitor prevents large voltage transients from appearing at the input. Use a 1μF-10μF value with X5R or X7R dielectric. Depending on construction, a ceramic capacitor's value can decrease up to 50% of its nominal value when rated voltage is applied. Consult with the capacitor manufactures data sheet for information on capacitor derating over voltage and temperature. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the LV2841/2. The input ripple current can be calculated using below Equations.

For this example design, one 2.2μF, 50V capacitor is selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 10. Using the design example values, Ioutmax = 0.6 A, Cin = 2.2μF, *f*sw = 2100 kHz, yields an input voltage ripple of 32.5 mV and a rms input ripple current of 0.3 A.

(9)

(10)

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor or larger is recommended for the bootstrap capacitor (C_{BOOT}). For applications where the input voltage is close to output voltage a larger capacitor is recommended, generally 0.1μF to 1μF to ensure plenty of gate drive for the internal switches and a consistently low R_{DSON}. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage.

Other Typical Application Circuits

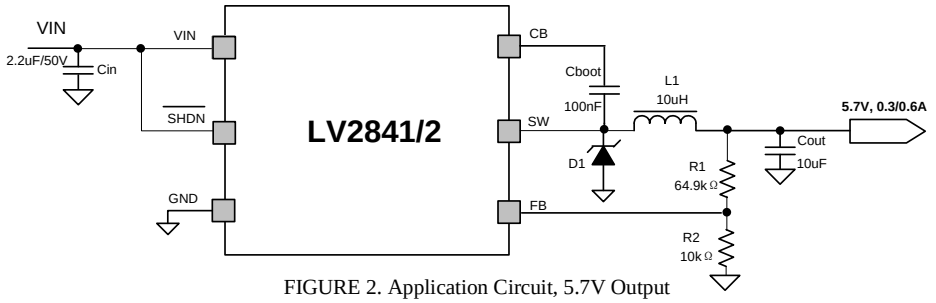


FIGURE 2. Application Circuit, 5.7V Output

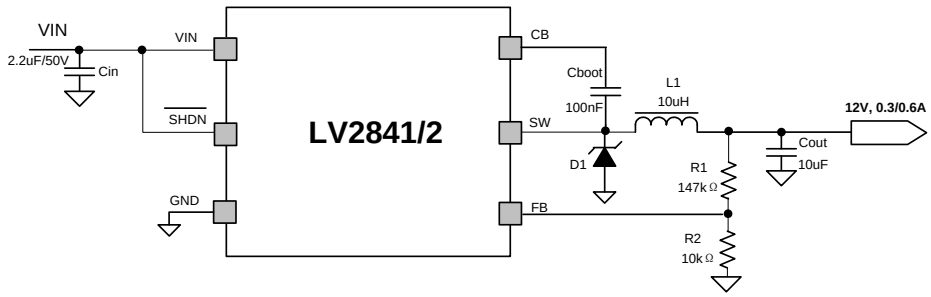


FIGURE 3. Application Circuit, 12V Output

Below are the recommended typical output voltage inductor/capacitor combinations for optimized total solution size.

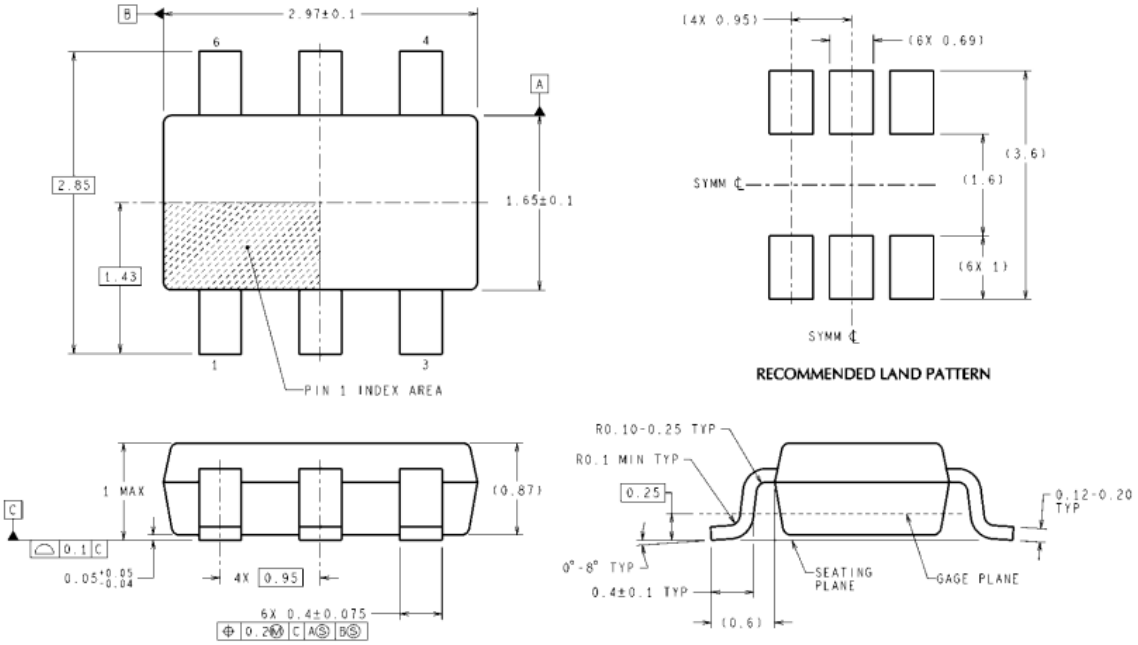
P/N	Vout(V)	R1(kΩ)	R2(kΩ)	L(μH)	Cout(μF)
LV2841/2 Y	5	54.9(1%)	10(1%)	3.3	10
LV2841/2 Y	5.7	64.9(1%)	10(1%)	3.3	10
LV2841/2 Y	12	147(1%)	10(1%)	3.3	10

Layout Considerations

To reduce problems with conducted noise pick up the ground side of feedback network should be connected directly to the GND pin with its own connection. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor to minimize coupling noise into the feedback pin. The input bypass capacitor C_{IN} must be placed close to the V_{IN} pin. This will reduce copper trace resistance which effects input voltage ripple of the IC. The inductor L1 should be placed close to the SW pin to reduce magnetic and electrostatic noise. The output capacitor, C_{OUT} should be placed close to the junction of L1 and the diode D1. The L1, D1, and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency. The ground connection for the diode, C_{IN}, and C_{OUT} should be as small as possible and tied to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane. For more detail on switching power supply layout considerations see Application Note AN-1149.

Mechanical Package Outline for TSOT-23

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

MK06A (Rev E)

TSOT 6 Pin Package (MK)
For Ordering, Refer to Ordering Information Table
NS Package Number MK06A