4.5V-100V Vin, 0.6A, High Efficiency Synchronous Step-down DCDC Converter with Programmable Frequency

FEATURES

- Wide Input Range: 4.5V-100V
- 0.6A Continuous Output Current
- 0.8V ±1% Feedback Reference Voltage
- Integrated 770mΩ High-Side and 460mΩ Low-Side Power MOSFETs
- Pulse Frequency Modulation (PFM) with 100uA Quiescent Current in Sleep Mode
- 4ms Internal Soft-start Time
- Adjustable Frequency 300KHz to 800KHz
- Precision Enable Threshold for Programmable Input Voltage Under-voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Cycle-by-Cycle Current Limiting
- Over-Voltage Protection
- Over-Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- E-Tools
- E-bike, Scooter
- GPS Tracker

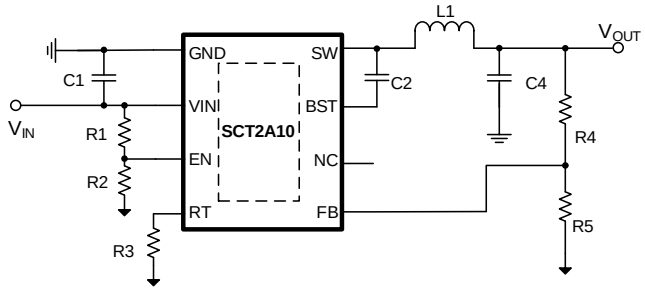
DESCRIPTION

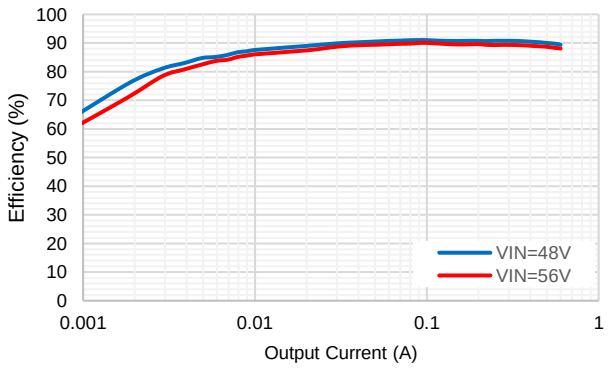
The SCT2A1 is 0.6A synchronous buck converters with wide input voltage, ranging from 4.5V to 100V, which integrates an 770mΩ high-side MOSFET and a 460mΩ low-side MOSFET. The SCT2A10, adopting the constant-on time (COT) mode control, supports the PFM with typical 100uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The SCT2A10 features programmable switching frequency from 300 kHz to 800kHz, which provides the flexibility to optimize either efficiency or external component size.

The SCT2A10 offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin thermally enhanced SOP-8 package.

TYPICAL APPLICATION





Efficiency of VOUT=12V

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 0.87: Engineering

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT2A10	2A10	8-Lead Plastic ESOP

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	102	V
BOOT	-0.3	108	V
SW	-1	102	V
BOOT-SW	-0.3	6	V
FB, RT	-0.3	6	V
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

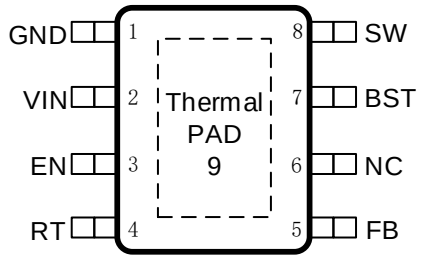


Figure 1. 8-Lead Plastic E-SOP

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
GND	1	Ground
VIN	2	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
EN	3	Enable pin to the regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
RT	4	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency.
FB	5	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
NC	6	NC

BST	7	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.5	100	V
V_{OUT}	Output voltage range	0.8	24	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-20L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	42	°C/W
$R_{\theta JC}$	Junction to case thermal resistance(1)	45.8	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2A10 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2A10. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=48V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		4.5		100	V
V_{IN_UVLO}	Input UVLO Threshold	V_{IN} rising		4.2		V
	Hysteresis			400		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		3		μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		100		μA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		770		mΩ

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DSON_L}	Low-side MOSFET on-resistance			460		mΩ
Reference and Control Loop						
V_{REF}	Reference voltage of FB			0.8		V
G_{EA}	Error amplifier trans-conductance	-2μA<I_{COMP}<2μA, V_{COMP}=1V		300		μS
G_{COMP}	COMP-IL trans-conductance			10		A/V
Enable and Soft-startup						
V_{EN_H}	Enable high threshold			1.21		V
V_{EN_L}	Enable low threshold			1.05		V
I_{EN_L}	Enable pin pull-up current	EN=1V		1.5		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		5.5		uA
T_{ss}	Internal soft start time			4		ms
Switching Frequency Timing						
F_{RANGE_RT}	Frequency range using RT mode		300		800	kHz
F_{SW}	Switching frequency	R_{RT}=200 kΩ(1%)	450	500	550	kHz
T_{ON_MIN}	Minimum on-time	V_{IN}=80V		100		ns
T_{OFF_MIN}	Minimum off-time	V_{IN}=80V				ns
Current Limit and Over Current Protection						
I_{LIM_P}	LS MOSFET positive current limit	From source to drain		0.8		A
T_{HICCUP}	Hiccup waiting time	Numbers of soft-start cycles		3		cycles
D_{HICCUP}	Hiccup duty cycle				12.5	%
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		110 105		% %
T_{SD}	Thermal shutdown threshold	T_J rising Hysteresis		170 25		°C °C

TYPICAL CHARACTERISTICS

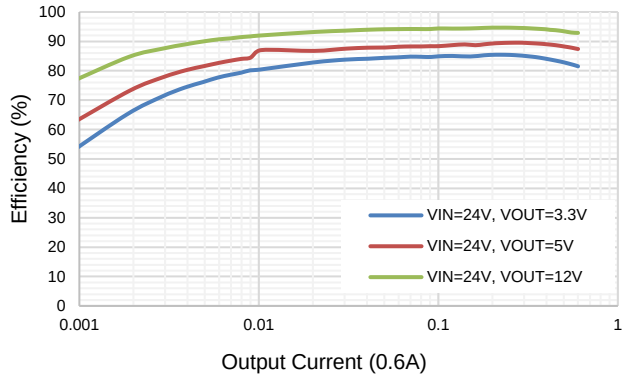


Figure 2. Efficiency vs Load Current, Vin=100V

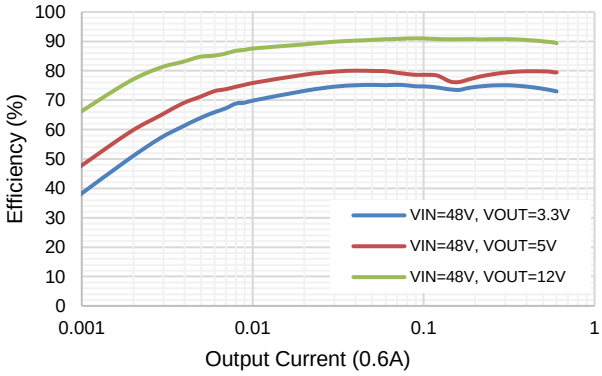


Figure 3. Efficiency vs Load Current, Vin=24V

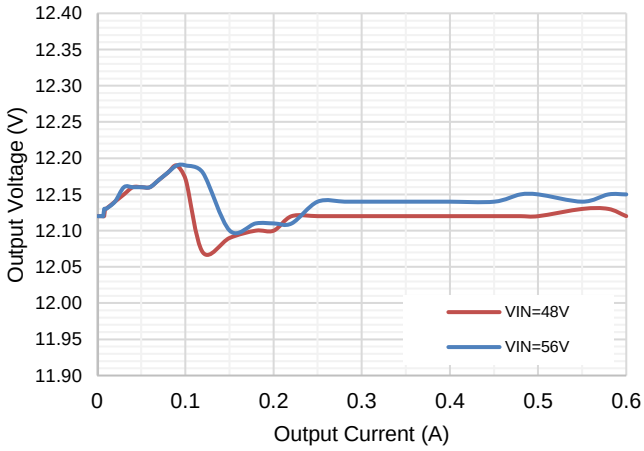


Figure 4. Load Regulation (Vout=12V)

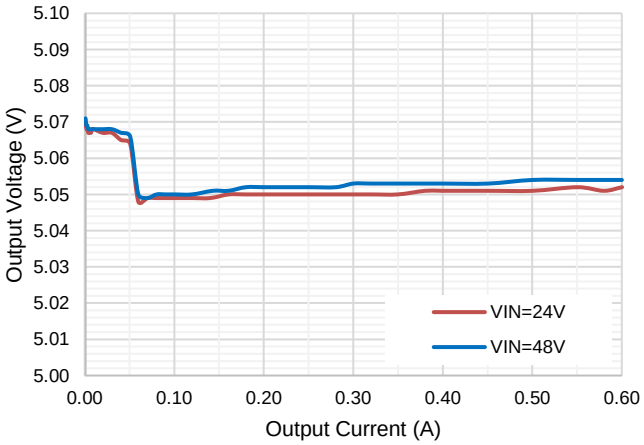


Figure 5. Load Regulation (Vout=5V)

FUNCTIONAL BLOCK DIAGRAM

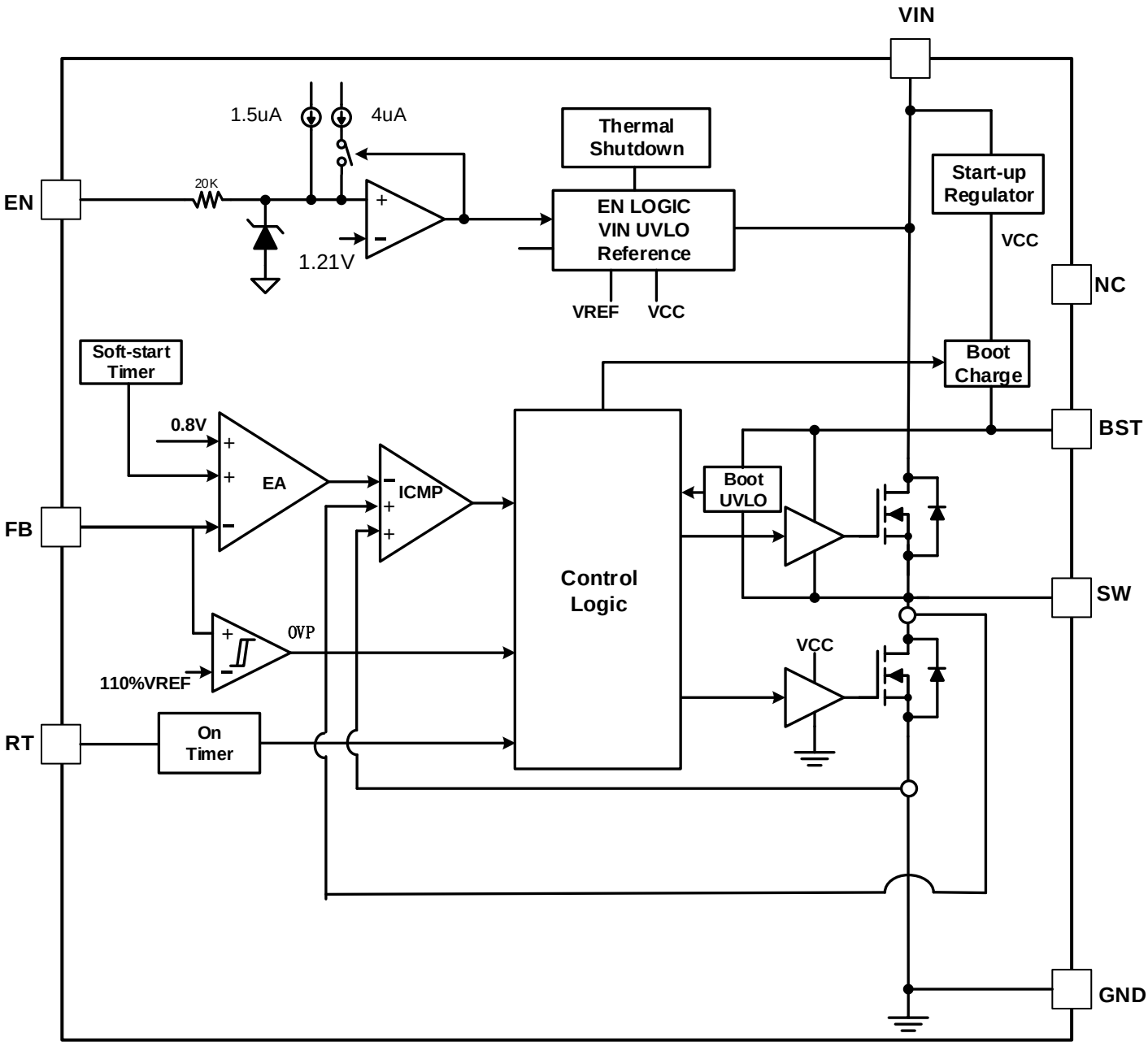


Figure 6. Functional Block Diagram

OPERATION

Overview

The SCT2A10 is a 4.5V-100V input, 0.6A output, internal-compensated synchronous buck converter with built-in 770mΩ Rdson high-side and 460mΩ Rdson low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response.

The switching frequency is programmable from 300kHz to 800KHz with resistor setting to optimizes either the power efficiency or the external components' sizes. The SCT2A10 features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PFM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 100uA under no load or sleep mode condition to achieve high efficiency at light load.

The SCT2A10 has a default input start-up voltage of 3.5V with 400mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The SCT2A10 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Constant On-Time Mode Control

The SCT2A10 employs constant-Off-Time Mode control providing fast transient with pseudo fixed switching frequency. At the beginning of each switching cycle, since the feedback voltage (VFB) is lower than the internal reference voltage (VREF), the high-side MOSFET (Q1) is turned on and the inductor current rises to charge up the output voltage. When sensed voltage on the high-side MOSFET valley current rises above the voltage of COMP, the device turns off Q1 and the low-side MOSFET (Q2) turns on. After dead time duration, the device turns on low-side MOSFET Q2 and the inductor current decreases. Based on Vin and Vout voltage, the device predicts required off-time and turns off low-side MOSFET Q2. This repeats on cycle-by-cycle based.

Enable and Under Voltage Lockout Threshold

The SCT2A10 is enabled when the VIN pin voltage rises about 4.2V and the EN pin voltage exceeds the enable threshold of 1.21V. The device is disabled when the VIN pin voltage falls below 3.8V or when the EN pin voltage is below 1.05V. An internal 1uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R3 and R4) shown in Figure 15 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$R3 = \frac{1.13 * V_{rise} - 1.19 * V_{fall}}{3.63} \quad (1)$$

$$R4 = \frac{1.13 * V_{rise} - 1.19 * V_{fall}}{4 * V_{rise} - V_{fall} - 3.63} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO
- R3 R4 is with unite of MΩ

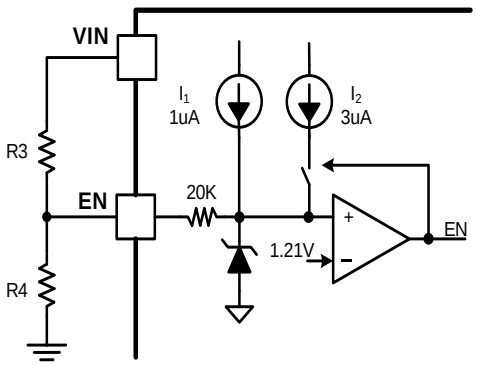


Figure 7. System UVLO by enable divide

Output Voltage

The SCT2A10 regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB\_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB\_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2A10 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 4ms. If the EN pin is pulled below 1.03V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Switching Frequency

The switching frequency of the SCT2A10 is set by placing a resistor between RT pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT pin to the ground sets the switching frequency over a wide range from 300KHz to 800KHz. The RT/CLK pin voltage is typical 0.5V. RT pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot in Figure 16. to determine the resistance for a switching frequency needed.

$$RT(K\Omega) = \frac{100000}{fsw(KHz)} \quad (4)$$

where,

fsw is switching clock frequency

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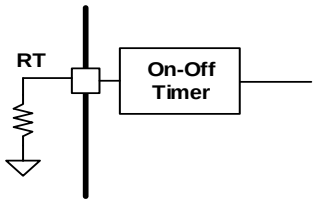


Figure 8. Setting Frequency

Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.7V and hysteresis of 350mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.35V, BOOT UVLO occurs. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

Over Current Limit and Hiccup Mode

The inductor current is monitored during low-side MOSFET Q2 on. The SCT2A10 implements over current protection with cycle-by-cycle limiting low-side MOSFET valley current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

Over voltage Protection

The SCT2A10 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The SCT2A10 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 170C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 145C, the device restarts with internal soft start phase.

APPLICATION INFORMATION

Typical Application

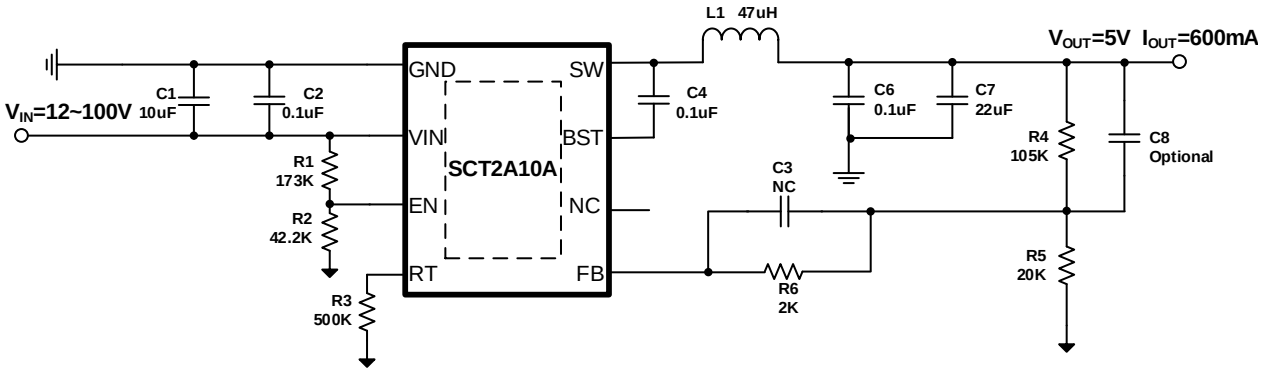


Figure 9. SCT2A10 Design Example, 5V Output with Programmable UVLO

Design Parameters

Design Parameters	Example Value
Input Voltage	48V Normal 48V to 100V
Output Voltage	5V
Maximum Output Current	600mA
Switching Frequency	500 KHz
Output voltage ripple (peak to peak)	50mV
Transient Response 60mA to 540mA load step	ΔVout = 250mV

Output Voltage

The output voltage is set by an external resistor divider R5 and R6 in typical application schematic. Recommended R6 resistance is 10.2KΩ. Use equation 5 to calculate R5.

$$R_5 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_6 \quad (5)$$

where:

- V_{REF} is the feedback reference voltage, typical 0.8V

Table 1. R_5, R_6Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_5	R_6
3.3 V	63.5 KΩ	20 KΩ
5 V	105 KΩ	20 KΩ
12 V	280 KΩ	20 KΩ
24 V	580 KΩ	20 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 32.7V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 26.5 V (stop or disable). Use Equation 7 and Equation 8 to calculate the values 115 kΩ and 42.2 kΩ of R_1 and R_2 resistors.

$$\mathrm{V_{rise}} = 1.19 * \left(1 + \frac{R_1}{R_2}\right) - 1\mathrm{uA} * \mathrm{R_1} \quad (7)$$

$$\mathrm{V_{fall}} = 1.15 * \left(1 + \frac{R_1}{R_2}\right) - 3\mathrm{uA} * R_1 \quad (8)$$

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~50% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 9.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (9)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 10 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (10)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 11 and equation 12.

$$I_{LVALLEY} = I_{OUT} - \frac{I_{LPP}}{2} \quad (11)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (12)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor valley current can increase up to the switch current limit of the device which is typically 0.8A. The most conservative approach is to choose an inductor with a saturation current rating greater than 0.8A. Because of the maximum $I_{LVALLEY}$ limited by device, the maximum output current that the SCT2A10 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a higher maximum output current.

For this design, use LIR=0.2 or 0.3, and the inductor value is calculated to be 33uH. The RMS inductor current is 600mA, and the and peak and valley inductor current is 860mA and 340mA respectively. The chosen inductor is a WE 7447714330, which has a saturation current rating of 2.9A

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0805) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 13.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (13)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (14)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increases.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

For this example, three 2.2μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 25V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 16 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (16)$$

Where

- $\Delta V_{OUT}$is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- $V_{IN}$is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, one 22μF ceramic output capacitors work for most applications.

Typical Application Circuit

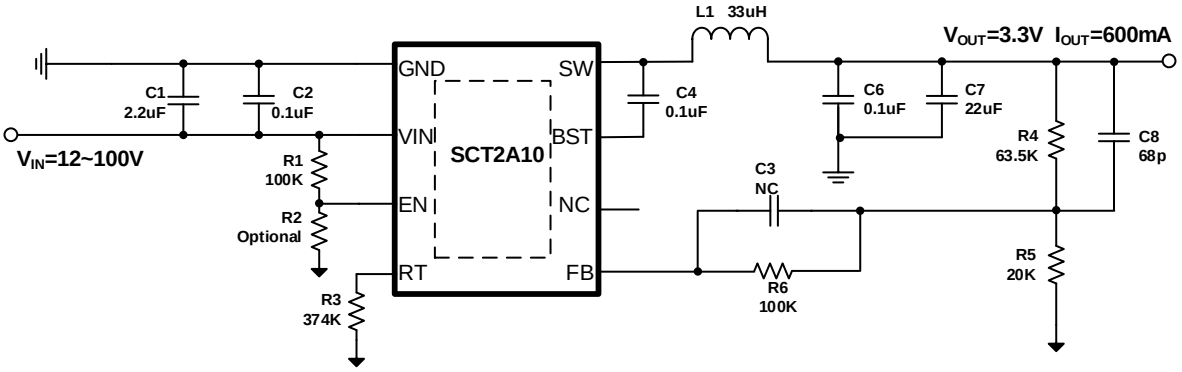


Figure 10. VOUT=3.3V, IOUT=0.6A Application Circuit

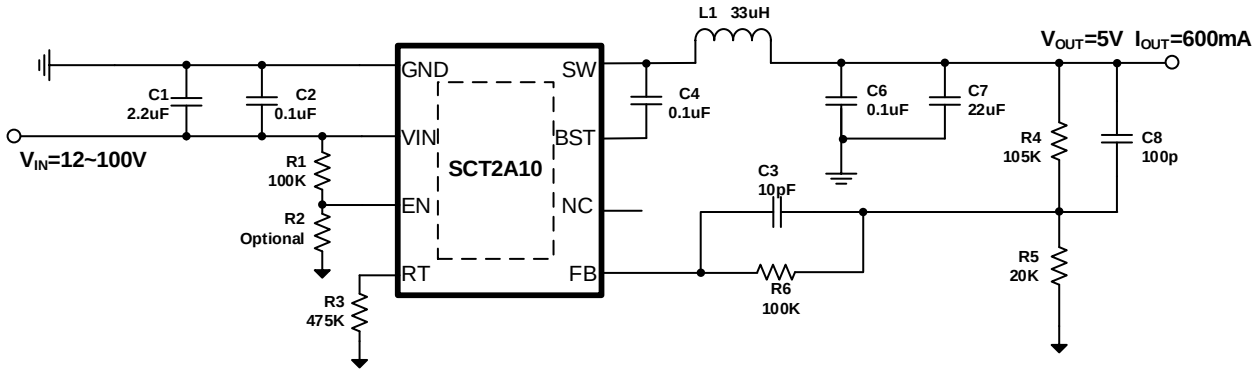


Figure 11. VOUT=5V, IOUT=0.6A Application Circuit

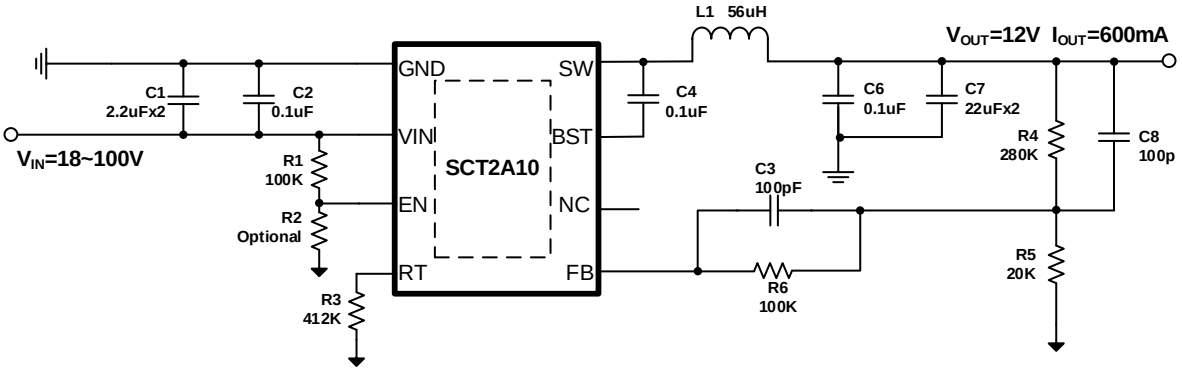


Figure 12. VOUT=12V, IOUT=0.6A Application Circuit

Layout Guideline

Proper PCB layout is a critical for SCT2A10's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. The RT terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
7. UVLO adjust and RT resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
8. Route BST capacitor trace on the top top layer to provide wide path for topside ground.
9. For achieving better thermal performance, a four-layer layout is strongly recommended.

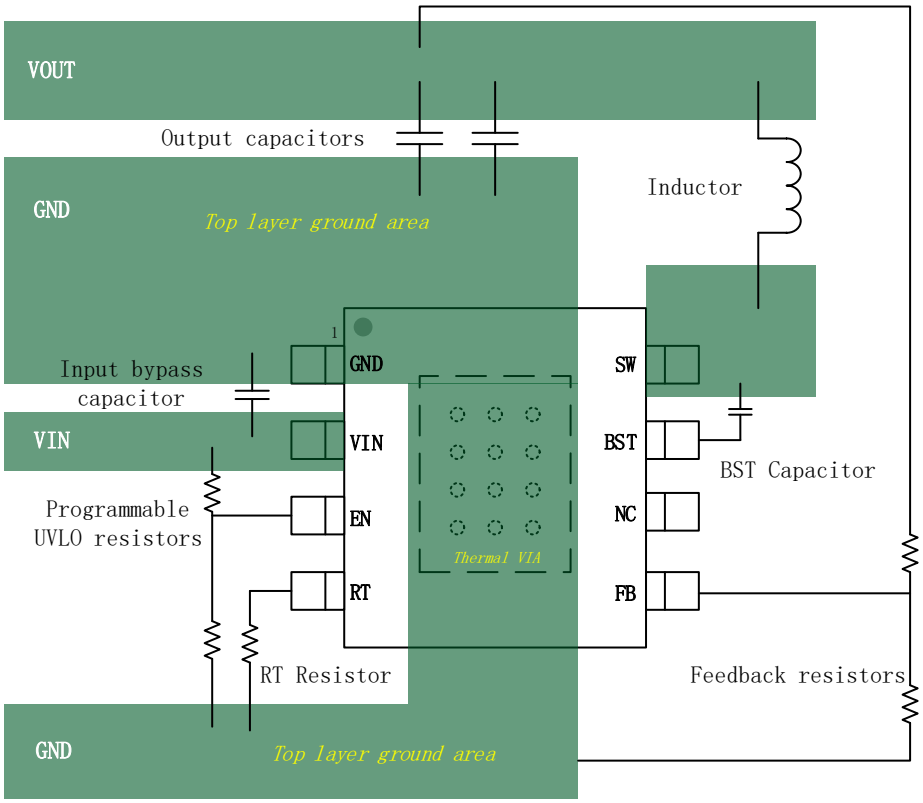
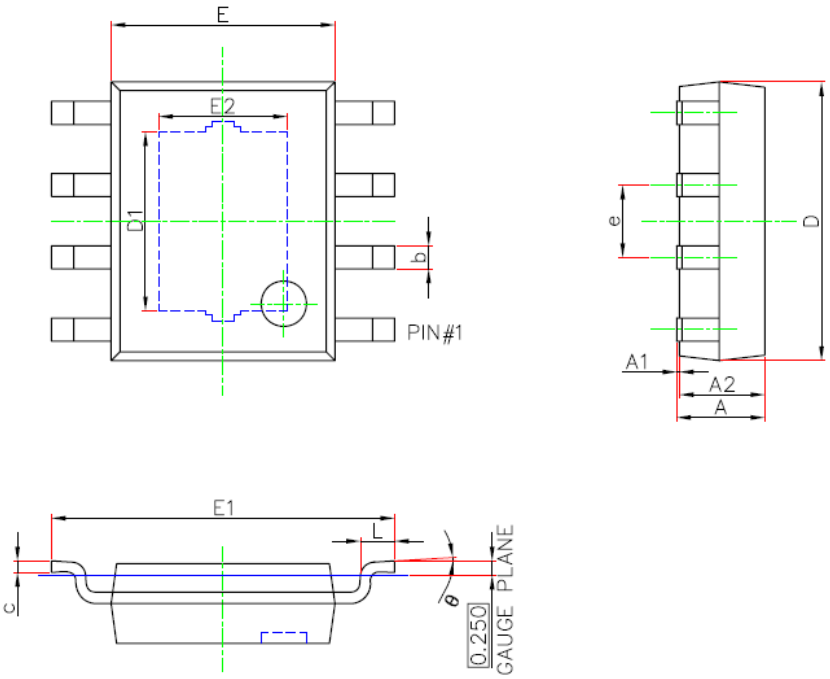


Figure 26. PCB Layout Example

PACKAGE INFORMATION



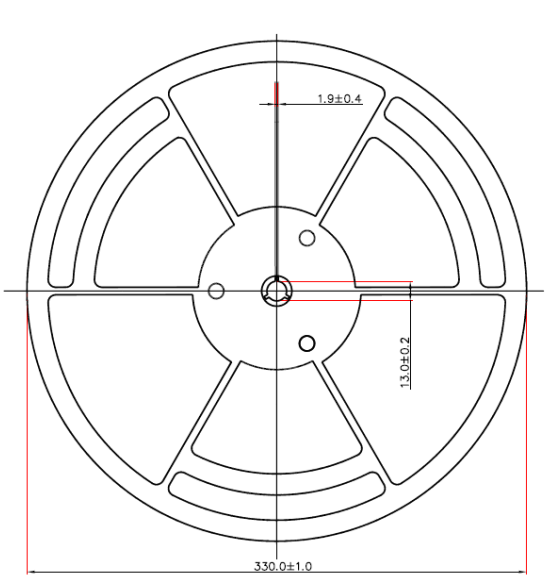
ESOP8/PP(95x130) Package Outline Dimensions

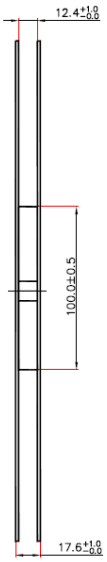
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

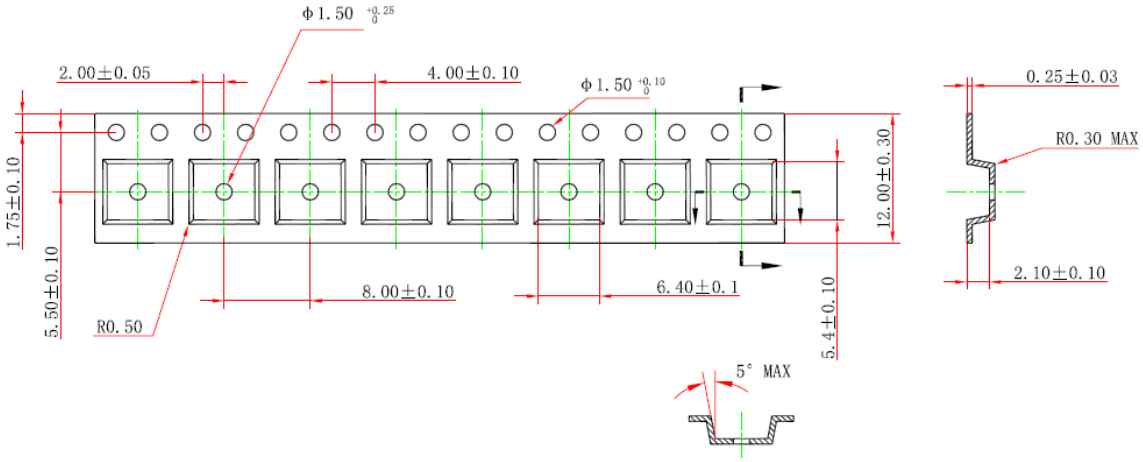
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

TAPE AND REEL INFORMATION







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