SGM42560
18V, 2A Three-Phase Integrated FET Motor Driver

GENERAL DESCRIPTION

The SGM42560 provides three integrated half-bridge MOSFET drivers for driving a three-phase brushless DC (BLDC) motor. This device integrates three current sense amplifiers (CSA) for sensing the three phase currents of BLDC motor. The SGM42560 has ENx and PWMx control inputs for each half-bridge. It uses an internal charge pump to generate the gate drive supply voltage for the HS FETs, and a trickle charge circuit that maintains sufficient gate drive voltage to operate at 100% duty cycle.

Internal protection functions are provided for under-voltage lockout (UVLO), over-current protection (OCP) and thermal shutdown (TSD). Fault conditions are indicated by the nFAULT pin. The SGM42560 is available in a Green TQFN-3×4-24L package.

FEATURES

- **3V to 18V Operating Supply Voltage**
- **Three Integrated Half-Bridge Drivers**
- **High Output Current Capability**
  - **2A Continuous Current**
  - **6A Peak Current**
- **On-Resistance: 170mΩ (HS + LS) at +25℃**
- **ENx and PWMx Control Inputs**
- **Integrated Bidirectional Current Sense Amplifiers**
- **Built-in 3.3V, 50mA LDO Regulator**
- **Internal Charge Pump Supports 100% Duty Cycle**
- **Automatic Synchronous Rectification**
- **Integrated Protection Features**
  - **Under-Voltage Lockout (UVLO)**
  - **Over-Current Protection (OCP) with Adjustable Threshold**
  - **Thermal Shutdown (TSD)**
- **Available in a Green TQFN-3×4-24L Package**

APPLICATIONS

Three-Phase BLDC Motor Drivers

TYPICAL APPLICATION

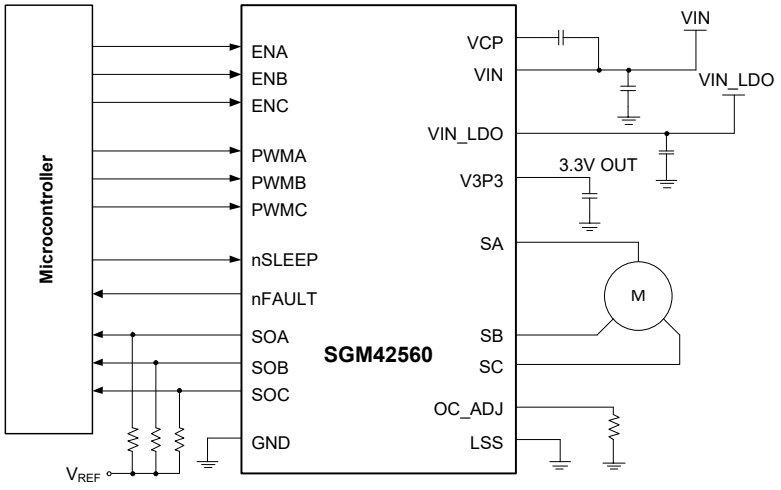


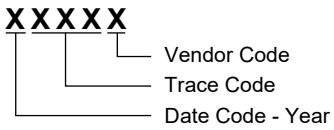
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42560	TQFN-3×4-24L	-40℃ to +125℃	SGM42560XTRR24G/TR	SGM 42560TRR XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN}, V_{IN_LDO} ..... -0.3V to 20V
V_{Sx} ..... -0.3V to V_{IN} + 0.3V
V_{CP} ..... -0.3V to V_{IN} + 5V
GND to LSS ..... -0.3V to 0.3V
Voltage at All Other Pins ..... -0.3V to 5V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN}, V_{IN_LDO} ..... 3V to 18V
Operating Junction Temperature Range ..... -40℃ to +150℃
Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

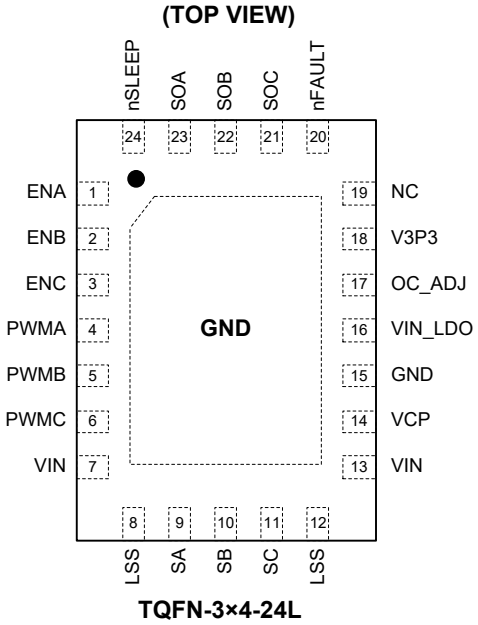
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	ENA	Enable Input for Phase A.
2	ENB	Enable Input for Phase B.
3	ENC	Enable Input for Phase C.
4	PWMA	PWM Input for Phase A.
5	PWMB	PWM Input for Phase B.
6	PWMC	PWM Input for Phase C.
7, 13	VIN	Input Power.
8, 12	LSS	Low-side Source Connection for Phase A, B, C. Must be connected directly to GND.
9	SA	Phase A Output.
10	SB	Phase B Output.
11	SC	Phase C Output.
14	VCP	Charge Pump Output. Connect a 1μF ceramic capacitor to VIN pin.
15	GND	Ground.
16	VIN_LDO	V3P3 LDO Input Power.
17	OC_ADJ	Over-Current Threshold Programming Pin.
18	V3P3	3.3V Regulator Output. Low-side gate drive supply voltage. Bypass to GND with a 4.7μF ceramic capacitor.
19	NC	No Connection.
20	nFAULT	Fault Indication. Open-drain output type, logic low when in fault conditions.
21	SOC	Current Sense Output for Phase C.
22	SOB	Current Sense Output for Phase B.
23	SOA	Current Sense Output for Phase A.
24	nSLEEP	Sleep Mode Input. Logic low to enter low power sleep mode. Internal pull-down.
Exposed Pad	GND	Ground.

ELECTRICAL CHARACTERISTICS

(T_J = +25℃, V_{IN} = 10V, LSS = GND = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Input Supply Voltage	V_{IN}, V_{IN_LDO}		3		18	V
Quiescent Current	I_Q	nSLEEP = 1, ENx = 0		2.9		mA
	I_{nSLEEP}	nSLEEP = 0		45		μA
Control Logic						
Input Low Threshold	V_{IL}			0.81		V
Input High Threshold	V_{IH}			1.27		V
Logic Input Current	I_{INH}	V_{IN} = 5V		10		μA
	I_{INL}	V_{IN} = 0V		0		μA
Power-Up Delay	t_{PUD}	At V_{IN} rising or nSLEEP rising		0.8		ms
Internal Pull-Down Resistance	R_{PD}	All logic inputs		500		kΩ
nFAULT Pull-Down R_{ON}	R_{ON_nFAULT}			5		Ω
V3P3 Regulator						
V3P3 Pin Voltage	V_{V3P3}	I_{OUT} = 0mA to 50mA		3.45		V
Protection Circuits						
UVLO Threshold	V_{UVLO}	V_{IN} rising		2.81		V
UVLO Hysteresis	ΔV_{UVLO}			200		mV
OCP Threshold	I_{OCP}	R_{OCP} = 0Ω		3.2		A
		R_{OCP} = Floating		6		A
OCP Deglitch Time	t_{OCD}			1		μs
Thermal Shutdown Threshold	T_{TSD}	T_J rising		170		℃
Thermal Shutdown Hysteresis	T_{HYS}			30		℃
Current Sense						
Current Sense Ratio				1/4000		A/A
Current Sense Output Current		LS FET current = 1A		250		μA
		LS FET current = -1A		-250		μA
		LS FET current = 100mA		25		μA
		LS FET current = -100mA		-25		μA
Positive and Negative Matching (Ratio of Positive-to-Negative)		LS FET current = ±1A, ±100mA		95%		
Phase Matching (Ratio of Phase-to-Phase)		LS FET current = ±1A, ±100mA		95%		
Current Sense Output Voltage Swing		LS FET current = ±0.25A		4		V
Output						
HS FET On-Resistance	R_{DSON}	I_{OUT} = 1A		80		mΩ
LS FET On-Resistance		I_{OUT} = 1A		91		
Output Rise Time	t_R	R_{LOAD} = 50Ω		25		ns
Output Fall Time	t_F	R_{LOAD} = 50Ω		25		ns
Dead Time	t_D	R_{LOAD} = 50Ω		40		ns
PWMx to Sx Delay Time Rising	t_{DLY_R}			70		ns
PWMx to Sx Delay Time Falling	t_{DLY_F}			90		ns
Charge Pump						
Charge Pump Output Voltage	V_{CP}			V_{IN} + 3.75		V

FUNCTIONAL BLOCK DIAGRAM

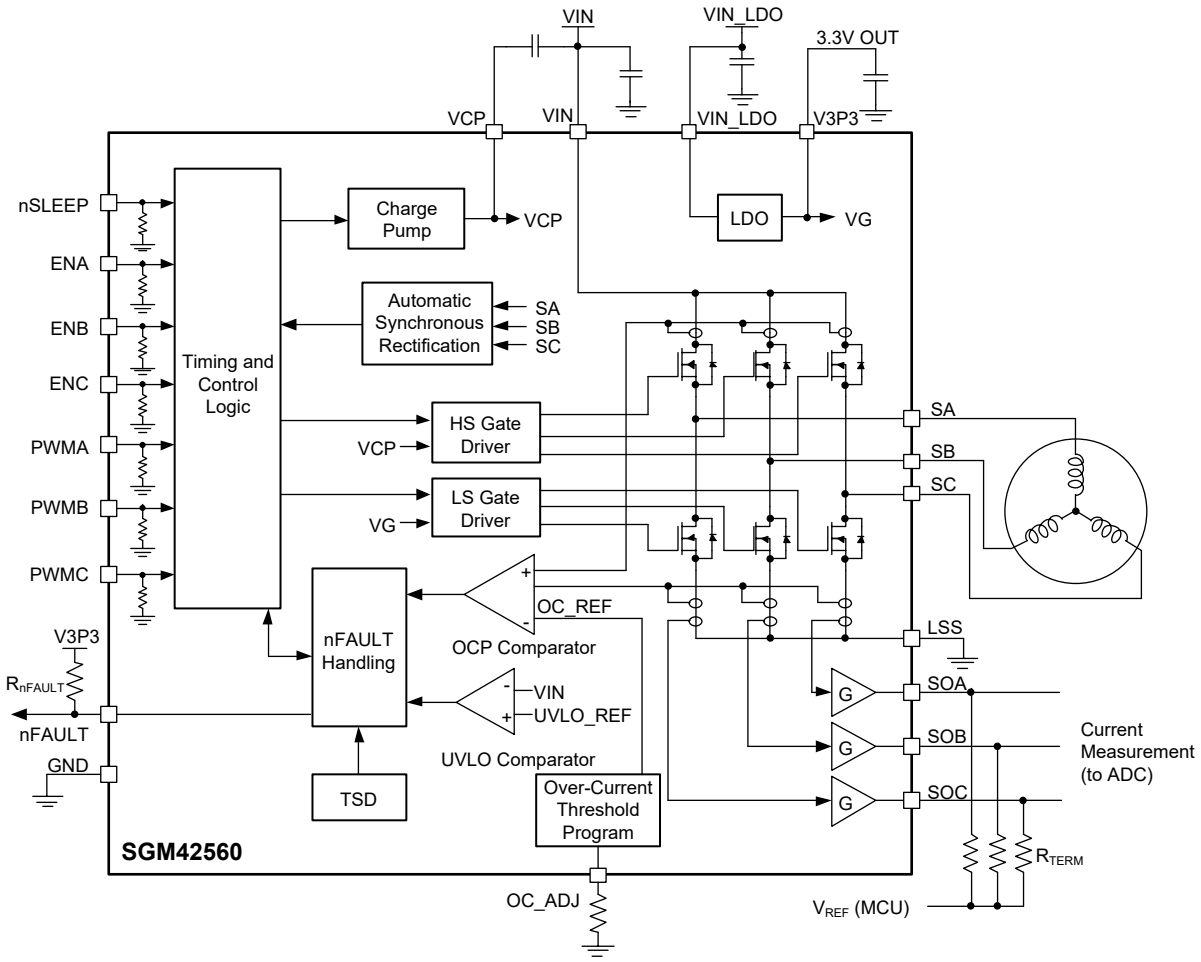


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM42560 device is an integrated 170mΩ (combination of HS and LS FETs on-resistance) driver for three-phase BLDC motor drive applications. The device reduces system component counts, cost and complexity by integrating three half-bridge FETs, gate drivers, charge pump and current sense amplifiers.

Input Logic

The SGM42560 has logic input pins (ENA, ENB and ENC), which enable the outputs (SA, SB and SC). When ENx is low, the corresponding output is disabled (output is in high-impedance (Hi-Z) state), and the PWMx input on that phase is ignored. When ENx is high, the corresponding output is enabled, and the PWMx input controls the state of the output. Table 1 shows the logic truth table.

Table 1. Input Logic Truth Table of SGM42560

ENx	PWMx	Sx
H	H	VIN
H	L	GND
L	X	Hi-Z

nSLEEP Operation

When the nSLEEP pin is low, the device goes to a low power sleep mode. In sleep mode, all the internal circuits are disabled and all inputs are ignored. When waking up from the sleep mode, if the charge pump output capacitor is fully discharged, approximately 0.8ms must pass before the device responds to inputs. The nSLEEP input has a weak pull-down resistor.

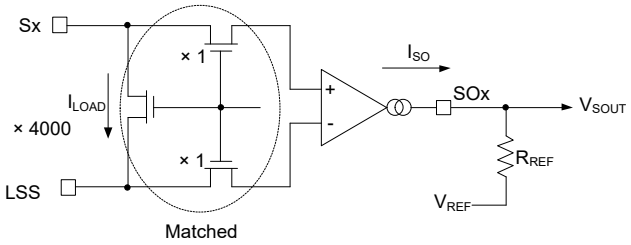
Current Sense Amplifiers

The SGM42560 integrates three high performance LS current sense amplifiers for current measurements using built-in current sensing. LS current measurements are commonly used to implement over-current protection, external torque control, or brushless DC commutation with an external controller. All three amplifiers can be used to sense the current in each of the half-bridge legs (LS FETs).

The current flowing in each of the three outputs is sensed by internal current sensing circuits. An output pin for each phase sources or sinks a current that is proportional to the current flowing in each phase. Note that only current flowing in the LS FET is sensed, and that it is sensed in both the forward and reverse directions. To convert this current into a voltage (e.g. to input to an ADC), a termination resistor (R_{REF}) is used as a reference voltage. When there is no current flowing, the resultant output will be equal to the reference voltage. When current is flowing, the voltage is above or below the reference voltage, determined with Equation 1:

$$V_{SOUT} = V_{REF} + (R_{REF} \times I_{LOAD})/4000 \quad (1)$$

To terminate the outputs when using an ADC with inputs that are ratio-metric to its supply voltage, use two equal value resistors to connect to the ADC supply and ground. The resulting ADC code will be half-scale at zero current. Figure 3 shows a simplified drawing of the current measurement circuit.



$I_{SO} = I_{LOAD}/4000$

$V_{SOUT} = V_{REF} + (I_{SO} \times R_{REF}) = V_{REF} + ((I_{LOAD} \times R_{REF})/4000)$

Figure 3. Current Measurement Circuit Diagram

Automatic Synchronous Rectification

The SGM42560 has automatic synchronous rectification feature (active demagnetization) which reduces power losses in device by reducing body-diode conduction losses. If a half-bridge power FETs are both turned off, and the recirculation current must continue to flow, then the automatic synchronous rectification applies.

The SGM42560 includes a HS output comparator and a LS output comparator for each half-bridge channel, which detect the respective body-diodes' current flow. The HS output comparator compares the half-bridge output voltage with respect to V_{IN}. The LS output comparator compares the half-bridge output voltage with respect to LSS. When both HS and LS FETs of a channel are turned off, upon the flow of the recirculation current: if the LS body-diode conducts, the half-bridge output voltage is driven below LSS, the LS output comparator trips, then the LS FET is turned on until the current flowing through it reduces to zero; similarly, if the HS body-diode conducts, the half-bridge output voltage is driven above V_{IN}, the HS output comparator trips, then the HS FET is turned on until the current flowing through it reduces to zero.

DETAILED DESCRIPTION (continued)

nFAULT Output

The SGM42560 provides an nFAULT output pin, which is driven active low in a fault condition, such as over-current protection (OCP) or thermal shutdown (TSD). This pin is an open-drain output, and must be pulled up by an external pull-up resistor.

Input UVLO Protection

If at any time the input supply voltage on the VIN pin falls lower than the V_{UVLO} threshold (V_{IN} falling threshold), all of the integrated FETs, driver charge pump and digital logic controller are disabled the internal logic is reset. Normal operation resumes when V_{IN} rises above the V_{UVLO} threshold.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT is driven low. Normal operation resumes when the die temperature has fallen to a safe level.

Over-Current Protection

A MOSFET over-current event is sensed by monitoring the current flowing through the FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the t_{OCD} deglitch time, the OCP circuit limits the current through each FET by disabling its gate driver. And all six output FETs are disabled (outputs become high-impedance) and nFAULT is driven low. The current is then recirculated through the body diodes. The over-current shutdown is latched until either nSLEEP is reset or VIN is power-cycled.

Over-current conditions on both high-side and low-side devices (e.g. a short to ground, supply, or across the motor winding) all result in an over-current shutdown.

Figure 4 shows a simplified diagram of the OCP circuit for one output.

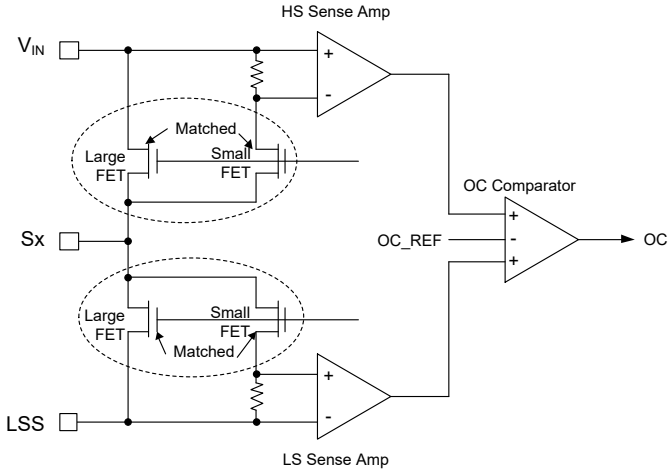


Figure 4. OCP Circuit

Table 2. Over-Current Threshold

OC_ADJ Resistor Value	OCP Threshold (TYP)
0Ω	3.2A
100kΩ	4.8A
Floating	6.0A

3.3V LDO Output

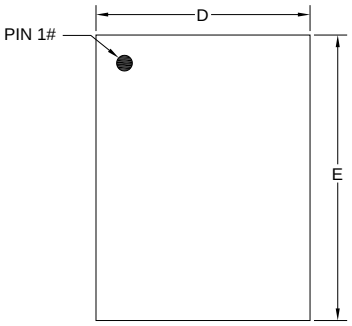
An internal LDO regulator generates a 3.3V voltage with 50mA capacity, which can be used to power a microcontroller. A bypass capacitor between 4.7μF to 10μF is required from the V3P3 pin to ground.

Charge Pump

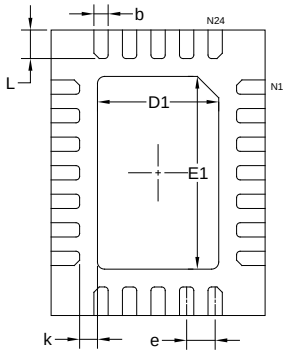
A charge pump is used to generate the gate drive for the HS FETs. The charge pump requires one external, 1μF ceramic capacitor rated for at least 10V between VIN pin and VCP pin.

PACKAGE OUTLINE DIMENSIONS

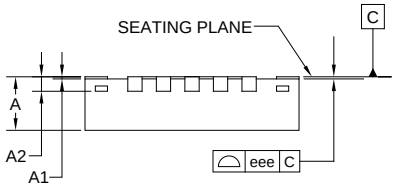
TQFN-3×4-24L



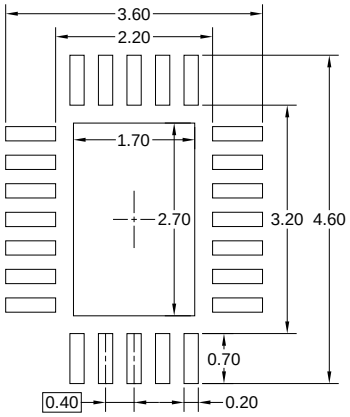
TOP VIEW



BOTTOM VIEW



SIDE VIEW



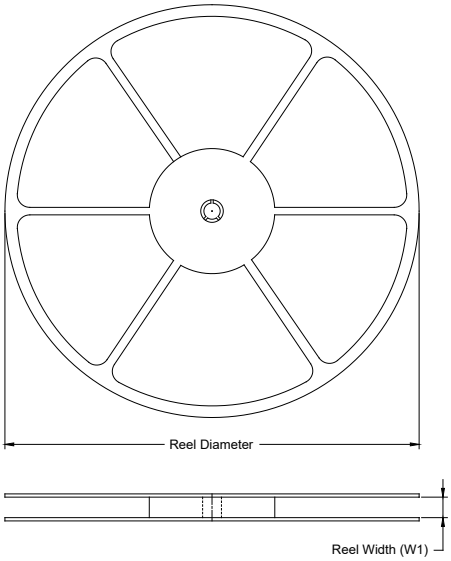
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.150	0.200	0.250
D	2.900	3.000	3.100
E	3.900	4.000	4.100
D1	1.600	1.700	1.800
E1	2.600	2.700	2.800
k	0.250 REF		
L	0.300	0.400	0.500
e	0.400 BSC		
eee	0.080		

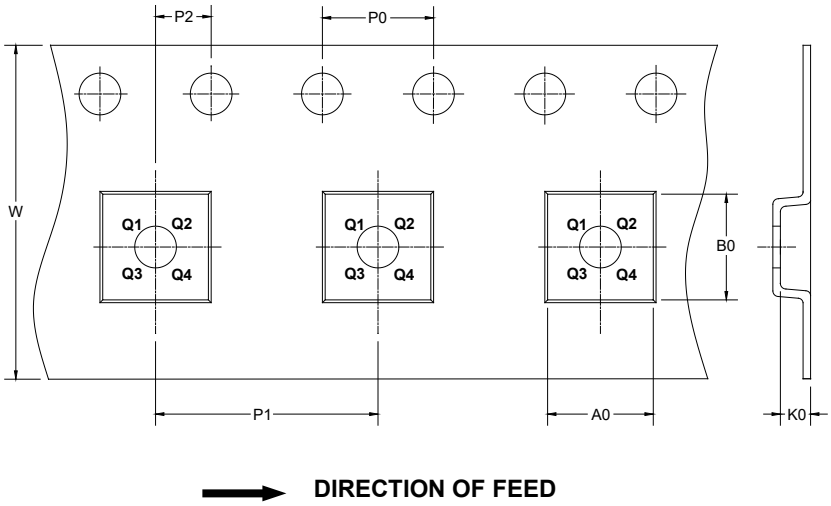
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



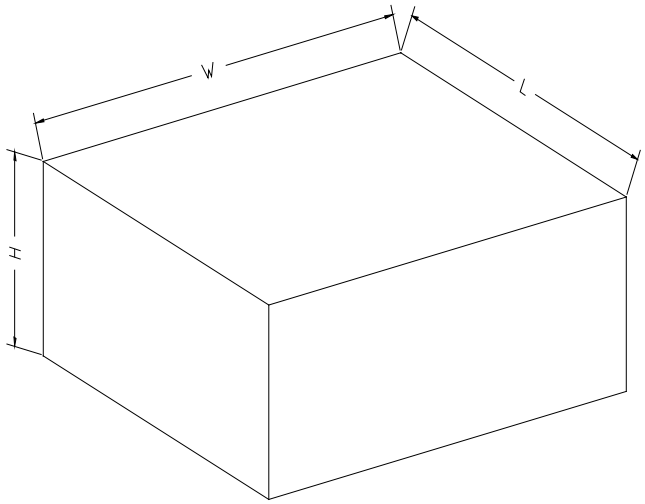
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×4-24L	13″	12.4	3.40	4.40	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002