

# 74LVC16373A; 74LVCH16373A

16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

Rev. 10 — 1 October 2021

Product data sheet

## 1. General description

The 74LVC16373A and 74LVCH16373A are 16-bit D-type transparent latches with 3-state outputs. The devices can be used as two 8-bit transparent latches or a single 16-bit transparent latch. The devices feature two latch enables (1LE and 2LE) and two output enables (1OE and 2OE), each controlling 8-bits. When nLE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When nLE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of nLE. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. Operation of the nOE input does not affect the state of the latches. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

Bus hold on the data inputs eliminates the need for external pull-up resistors to hold unused inputs.

## 2. Features and benefits

- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power dissipation
- MULTIBYTE flow-through standard pinout architecture
- Multiple low inductance supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16373A only)
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Complies with JEDEC standards:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM ANSI/ESDA/Jedec JS-002 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

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## 3. Ordering information

Table 1. Ordering information

| Type number     | Package           |         |   | Version  |
|-----------------|-------------------|---------|---|----------|
|                 | Temperature range | Name    | Description   |          |
| 74LVC16373ADGG  | -40 °C to +125 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm                    | SOT362-1 |
| 74LVCH16373ADGG |                   |         |   |          |
| 74LVC16373ADGV  | -40 °C to +125 °C | TVSOP48 | plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm | SOT480-1 |
| 74LVCH16373ADGV |                   |         |   |          |

## 4. Functional diagram

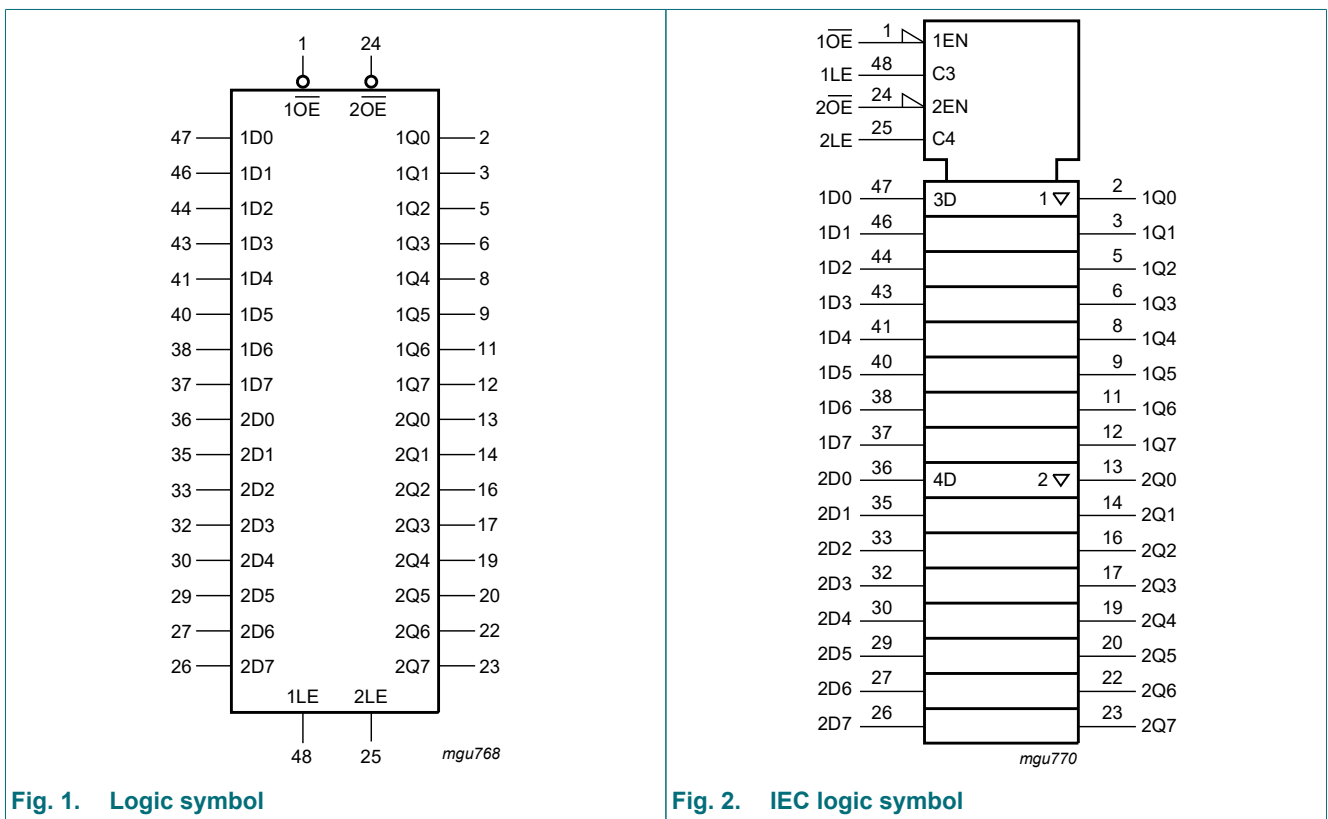


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

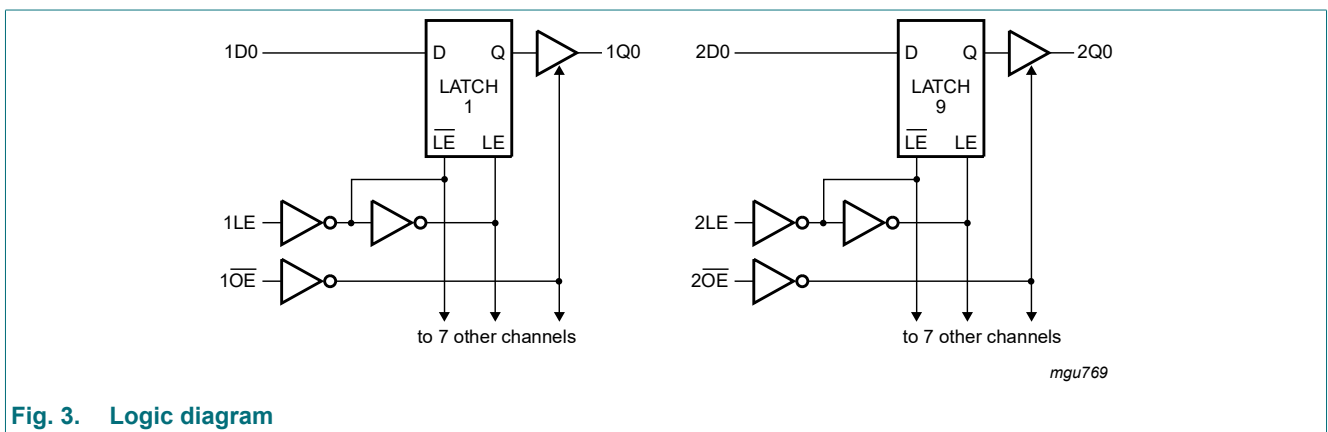


Fig. 3. Logic diagram

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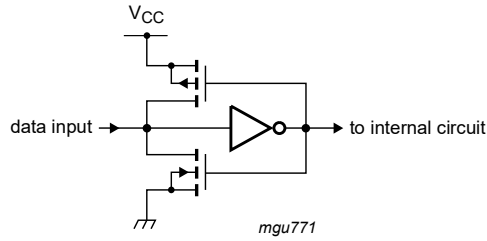


Fig. 4. Bus hold circuit

## 5. Pinning information

### 5.1. Pinning

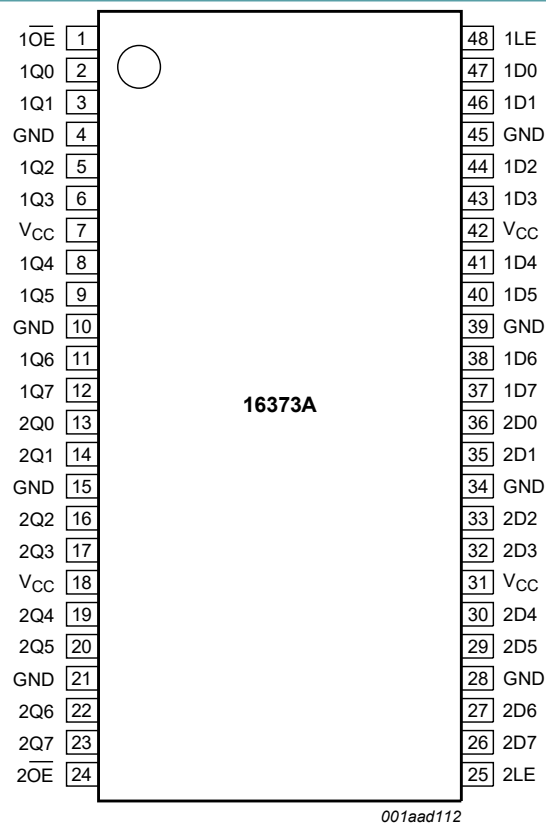


Fig. 5. Pin configuration SOT362-1 (TSSOP48) and SOT480-1 (TSSOP48)

## 5.2. Pin description

Table 2. Pin description

| Symbol          | Pin                            | Description                      |
|-----------------|--------------------------------|----------------------------------|
| 1OE, 2OE        | 1, 24                          | output enable input (active LOW) |
| 1LE, 2LE        | 48, 25                         | latch enable input (active HIGH) |
| GND             | 4, 10, 15, 21, 28, 34, 39, 45  | ground (0 V)                     |
| V <sub>CC</sub> | 7, 18, 31, 42                  | supply voltage                   |
| 1Q0 to 1Q7      | 2, 3, 5, 6, 8, 9, 11, 12       | data output                      |
| 2Q0 to 2Q7      | 13, 14, 16, 17, 19, 20, 22, 23 | data output                      |
| 1D0 to 1D7      | 47, 46, 44, 43, 41, 40, 38, 37 | data input                       |
| 2D0 to 2D7      | 36, 35, 33, 32, 30, 29, 27, 26 | data input                       |

## 6. Functional description

Table 3. Function table

Per section of eight bits.

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH to LOW LE transition

L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH to LOW LE transition

Z = high-impedance OFF-state

| Operating modes                                | Input |     |     | Internal latch | Output<br>nQ0 to nQ7 |
|--|-------|-----|-----|----------------|----------------------|
|  | nOE   | nLE | nDn |                |                      |
| Enable and read register<br>(transparent mode) | L     | H   | L   | L              | L                    |
|  | L     | H   | H   | H              | H                    |
| Latch and read register                        | L     | L   | l   | L              | L                    |
|  | L     | L   | h   | H              | H                    |
| Latch register and disable outputs             | H     | L   | l   | L              | Z                    |
|  | H     | L   | h   | H              | Z                    |

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol    | Parameter               | Conditions                    | Min      | Max            | Unit |
|-----------|-------------------------|-------------------------------|----------|----------------|------|
| $V_{CC}$  | supply voltage          |                               | -0.5     | +6.5           | V    |
| $I_{IK}$  | input clamping current  | $V_I < 0$                     | -50      | -              | mA   |
| $V_I$     | input voltage           |                               | [1] -0.5 | +6.5           | V    |
| $I_{OK}$  | output clamping current | $V_O > V_{CC}$ or $V_O < 0$   | -        | ±50            | mA   |
| $V_O$     | output voltage          | output HIGH or LOW state      | [2] -0.5 | $V_{CC} + 0.5$ | V    |
|           |                         | output 3-state                | [2] -0.5 | +6.5           | V    |
| $I_O$     | output current          | $V_O = 0$ V to $V_{CC}$       | -        | ±50            | mA   |
| $I_{CC}$  | supply current          |                               | -        | 100            | mA   |
| $I_{GND}$ | ground current          |                               | -100     | -              | mA   |
| $T_{stg}$ | storage temperature     |                               | -65      | +150           | °C   |
| $P_{tot}$ | total power dissipation | $T_{amb} = -40$ °C to +125 °C | [3] -    | 500            | mW   |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT362-1 (TSSOP48) packages:  $P_{tot}$  derates linearly with 12.2 mW/K above 109 °C.

For SOT480-1 (TVSOP48) packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol              | Parameter                           | Conditions                | Min  | Typ | Max      | Unit |
|---------------------|-------------------------------------|---------------------------|------|-----|----------|------|
| $V_{CC}$            | supply voltage                      |                           | 1.65 | -   | 3.6      | V    |
|                     |                                     | functional                | 1.2  | -   | 3.6      | V    |
| $V_I$               | input voltage                       |                           | 0    | -   | 5.5      | V    |
| $V_O$               | output voltage                      | output HIGH or LOW state  | 0    | -   | $V_{CC}$ | V    |
|                     |                                     | output 3-state            | 0    | -   | 5.5      | V    |
| $T_{amb}$           | ambient temperature                 | in free air               | -40  | -   | +125     | °C   |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.2$ V to 2.7 V | 0    | -   | 20       | ns/V |
|                     |                                     | $V_{CC} = 2.7$ V to 3.6 V | 0    | -   | 10       | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol           | Parameter                 | Conditions   | -40 °C to +85 °C      |         |                     | -40 °C to +125 °C     |                     | Unit |
|------------------|---------------------------|--|-----------------------|---------|---------------------|-----------------------|---------------------|------|
|                  |                           |  | Min                   | Typ [1] | Max                 | Min                   | Max                 |      |
| V <sub>IH</sub>  | HIGH-level input voltage  | V <sub>CC</sub> = 1.2 V  | 1.08                  | -       | -                   | 1.08                  | -                   | V    |
|                  |                           | V <sub>CC</sub> = 1.65 V to 1.95 V   | 0.65V <sub>CC</sub>   | -       | -                   | 0.65V <sub>CC</sub>   | -                   | V    |
|                  |                           | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.7                   | -       | -                   | 1.7                   | -                   | V    |
|                  |                           | V <sub>CC</sub> = 2.7 V to 3.6 V   | 2.0                   | -       | -                   | 2.0                   | -                   | V    |
| V <sub>IL</sub>  | LOW-level input voltage   | V <sub>CC</sub> = 1.2 V  | -                     | -       | 0.12                | -                     | 0.12                | V    |
|                  |                           | V <sub>CC</sub> = 1.65 V to 1.95 V   | -                     | -       | 0.35V <sub>CC</sub> | -                     | 0.35V <sub>CC</sub> | V    |
|                  |                           | V <sub>CC</sub> = 2.3 V to 2.7 V   | -                     | -       | 0.7                 | -                     | 0.7                 | V    |
|                  |                           | V <sub>CC</sub> = 2.7 V to 3.6 V   | -                     | -       | 0.8                 | -                     | 0.8                 | V    |
| V <sub>OH</sub>  | HIGH-level output voltage | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>  |                       |         |                     |                       |                     |      |
|                  |                           | I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 1.65 V to 3.6 V  | V <sub>CC</sub> - 0.2 | -       | -                   | V <sub>CC</sub> - 0.3 | -                   | V    |
|                  |                           | I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V   | 1.2                   | -       | -                   | 1.05                  | -                   | V    |
|                  |                           | I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V  | 1.8                   | -       | -                   | 1.65                  | -                   | V    |
|                  |                           | I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V   | 2.2                   | -       | -                   | 2.05                  | -                   | V    |
|                  |                           | I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V   | 2.4                   | -       | -                   | 2.25                  | -                   | V    |
| V <sub>OL</sub>  | LOW-level output voltage  | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>  |                       |         |                     |                       |                     |      |
|                  |                           | I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 1.65 V to 3.6 V   | -                     | -       | 0.2                 | -                     | 0.3                 | V    |
|                  |                           | I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V  | -                     | -       | 0.45                | -                     | 0.65                | V    |
|                  |                           | I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V   | -                     | -       | 0.6                 | -                     | 0.8                 | V    |
|                  |                           | I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V  | -                     | -       | 0.4                 | -                     | 0.6                 | V    |
|                  |                           | I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V  | -                     | -       | 0.55                | -                     | 0.8                 | V    |
| I <sub>I</sub>   | input leakage current     | V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND [2]   | -                     | ±0.1    | ±5                  | -                     | ±20                 | µA   |
| I <sub>OZ</sub>  | OFF-state output current  | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 5.5 V or GND [2] | -                     | ±0.1    | ±5                  | -                     | ±20                 | µA   |
| I <sub>OFF</sub> | power-off leakage current | V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V  | -                     | ±0.1    | ±10                 | -                     | ±20                 | µA   |
| I <sub>CC</sub>  | supply current            | V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A                           | -                     | 0.1     | 20                  | -                     | 80                  | µA   |
| ΔI <sub>CC</sub> | additional supply current | per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A  | -                     | 5       | 500                 | -                     | 5000                | µA   |
| C <sub>I</sub>   | input capacitance         | V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>  | -                     | 5.0     | -                   | -                     | -                   | pF   |

| Symbol            | Parameter                       | Conditions   | -40 °C to +85 °C |         |     | -40 °C to +125 °C |     | Unit |
|-------------------|---------------------------------|--|------------------|---------|-----|-------------------|-----|------|
|                   |                                 |  | Min              | Typ [1] | Max | Min               | Max |      |
| I <sub>BHL</sub>  | bus hold LOW current            | V <sub>CC</sub> = 1.65; V <sub>I</sub> = 0.58 V [3][4] | 10               | -       | -   | 10                | -   | μA   |
|                   |                                 | V <sub>CC</sub> = 2.3; V <sub>I</sub> = 0.7 V          | 30               | -       | -   | 25                | -   | μA   |
|                   |                                 | V <sub>CC</sub> = 3.0; V <sub>I</sub> = 0.8 V          | 75               | -       | -   | 60                | -   | μA   |
| I <sub>BHH</sub>  | bus hold HIGH current           | V <sub>CC</sub> = 1.65; V <sub>I</sub> = 1.07 V [3][4] | -10              | -       | -   | -10               | -   | μA   |
|                   |                                 | V <sub>CC</sub> = 2.3; V <sub>I</sub> = 1.7 V          | -30              | -       | -   | -25               | -   | μA   |
|                   |                                 | V <sub>CC</sub> = 3.0; V <sub>I</sub> = 2.0 V          | -75              | -       | -   | -60               | -   | μA   |
| I <sub>BHLO</sub> | bus hold LOW overdrive current  | V <sub>CC</sub> = 1.95 V [3][5]                        | 200              | -       | -   | 200               | -   | μA   |
|                   |                                 | V <sub>CC</sub> = 2.7 V                                | 300              | -       | -   | 300               | -   | μA   |
|                   |                                 | V <sub>CC</sub> = 3.6 V                                | 500              | -       | -   | 500               | -   | μA   |
| I <sub>BHHO</sub> | bus hold HIGH overdrive current | V <sub>CC</sub> = 1.95 V [3][5]                        | -200             | -       | -   | -200              | -   | μA   |
|                   |                                 | V <sub>CC</sub> = 2.7 V                                | -300             | -       | -   | -300              | -   | μA   |
|                   |                                 | V <sub>CC</sub> = 3.6 V                                | -500             | -       | -   | -500              | -   | μA   |

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

[2] The bus hold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input pin.

[3] Valid for data inputs (74LVCH16373A) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified V<sub>I</sub> level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 10.

| Symbol          | Parameter         | Conditions                         | -40 °C to +85 °C |         |      | -40 °C to +125 °C |      | Unit |
|-----------------|-------------------|------------------------------------|------------------|---------|------|-------------------|------|------|
|                 |                   |                                    | Min              | Typ [1] | Max  | Min               | Max  |      |
| t <sub>pd</sub> | propagation delay | Dn to Qn; see Fig. 6 [2]           |                  |         |      |                   |      |      |
|                 |                   | V <sub>CC</sub> = 1.2 V            | -                | 12      | -    | -                 | -    | ns   |
|                 |                   | V <sub>CC</sub> = 1.65 V to 1.95 V | 1.5              | 5.4     | 11.4 | 1.5               | 13.2 | ns   |
|                 |                   | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.0              | 2.9     | 5.7  | 1.0               | 6.6  | ns   |
|                 |                   | V <sub>CC</sub> = 2.7 V            | 1.5              | 2.9     | 4.9  | 1.5               | 6.5  | ns   |
|                 |                   | V <sub>CC</sub> = 3.0 V to 3.6 V   | 1.0              | 2.4     | 4.4  | 1.0               | 5.5  | ns   |
|                 |                   | LE to Qn; see Fig. 7               |                  |         |      |                   |      |      |
|                 |                   | V <sub>CC</sub> = 1.2 V            | -                | 14      | -    | -                 | -    | ns   |
|                 |                   | V <sub>CC</sub> = 1.65 V to 1.95 V | 2.0              | 6.4     | 12.4 | 2.0               | 14.4 | ns   |
|                 |                   | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.5              | 3.4     | 6.1  | 1.5               | 7.1  | ns   |
|                 |                   | V <sub>CC</sub> = 2.7 V            | 1.5              | 3.0     | 5.3  | 1.5               | 7.0  | ns   |
|                 |                   | V <sub>CC</sub> = 3.0 V to 3.6 V   | 1.5              | 2.9     | 4.8  | 1.5               | 6.0  | ns   |
| t <sub>en</sub> | enable time       | OE to Qn; see Fig. 8 [2]           |                  |         |      |                   |      |      |
|                 |                   | V <sub>CC</sub> = 1.2 V            | -                | 18      | -    | -                 | -    | ns   |
|                 |                   | V <sub>CC</sub> = 1.65 V to 1.95 V | 1.5              | 5.5     | 12.4 | 1.5               | 14.3 | ns   |
|                 |                   | V <sub>CC</sub> = 2.3 V to 2.7 V   | 1.0              | 3.1     | 6.6  | 1.0               | 7.6  | ns   |
|                 |                   | V <sub>CC</sub> = 2.7 V            | 1.5              | 3.3     | 5.7  | 1.5               | 7.5  | ns   |
|                 |                   | V <sub>CC</sub> = 3.0 V to 3.6 V   | 1.0              | 2.5     | 4.9  | 1.0               | 6.5  | ns   |

# 74LVC16373A; 74LVCH16373A

## 16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

| Symbol             | Parameter                     | Conditions   | -40 °C to +85 °C |         |     | -40 °C to +125 °C |      | Unit |
|--------------------|-------------------------------|--|------------------|---------|-----|-------------------|------|------|
|                    |                               |  | Min              | Typ [1] | Max | Min               | Max  |      |
| t <sub>dis</sub>   | disable time                  | OE to Qn; see Fig. 8 [2]                               |                  |         |     |                   |      |      |
|                    |                               | V <sub>CC</sub> = 1.2 V                                | -                | 11      | -   | -                 | -    | ns   |
|                    |                               | V <sub>CC</sub> = 1.65 V to 1.95 V                     | 2.8              | 4.5     | 9.1 | 2.8               | 10.5 | ns   |
|                    |                               | V <sub>CC</sub> = 2.3 V to 2.7 V                       | 1.0              | 2.5     | 5.1 | 1.0               | 6.0  | ns   |
|                    |                               | V <sub>CC</sub> = 2.7 V                                | 1.5              | 3.3     | 6.3 | 1.5               | 8.0  | ns   |
|                    |                               | V <sub>CC</sub> = 3.0 V to 3.6 V                       | 1.5              | 3.1     | 5.4 | 1.5               | 7.0  | ns   |
| t <sub>w</sub>     | pulse width                   | LE HIGH; see Fig. 7                                    |                  |         |     |                   |      |      |
|                    |                               | V <sub>CC</sub> = 1.65 V to 1.95 V                     | 5.0              | -       | -   | 5.0               | -    | ns   |
|                    |                               | V <sub>CC</sub> = 2.3 V to 2.7 V                       | 4.0              | -       | -   | 4.0               | -    | ns   |
|                    |                               | V <sub>CC</sub> = 2.7 V                                | 3.0              | -       | -   | 3.0               | -    | ns   |
|                    |                               | V <sub>CC</sub> = 3.0 V to 3.6 V                       | 3.0              | 2.0     | -   | 3.0               | -    | ns   |
| t <sub>su</sub>    | set-up time                   | Dn to LE; see Fig. 9                                   |                  |         |     |                   |      |      |
|                    |                               | V <sub>CC</sub> = 1.65 V to 1.95 V                     | 3.0              | -       | -   | 3.0               | -    | ns   |
|                    |                               | V <sub>CC</sub> = 2.3 V to 2.7 V                       | 2.5              | -       | -   | 2.5               | -    | ns   |
|                    |                               | V <sub>CC</sub> = 2.7 V                                | 2.0              | -       | -   | 2.0               | -    | ns   |
|                    |                               | V <sub>CC</sub> = 3.0 V to 3.6 V                       | 2.0              | 1.0     | -   | 2.0               | -    | ns   |
| t <sub>h</sub>     | hold time                     | Dn to LE; see Fig. 9                                   |                  |         |     |                   |      |      |
|                    |                               | V <sub>CC</sub> = 1.65 V to 1.95 V                     | 2.5              | -       | -   | 2.5               | -    | ns   |
|                    |                               | V <sub>CC</sub> = 2.3 V to 2.7 V                       | 2.0              | -       | -   | 2.0               | -    | ns   |
|                    |                               | V <sub>CC</sub> = 2.7 V                                | 0.9              | -       | -   | 0.9               | -    | ns   |
|                    |                               | V <sub>CC</sub> = 3.0 V to 3.6 V                       | +0.9             | -1.0    | -   | +0.9              | -    | ns   |
| t <sub>sk(o)</sub> | output skew time              | V <sub>CC</sub> = 3.0 V to 3.6 V [3]                   | -                | -       | 1.0 | -                 | 1.5  | ns   |
| C <sub>PD</sub>    | power dissipation capacitance | per input; V <sub>I</sub> = GND to V <sub>CC</sub> [4] |                  |         |     |                   |      |      |
|                    |                               | V <sub>CC</sub> = 1.65 V to 1.95 V                     | -                | 10.8    | -   | -                 | -    | pF   |
|                    |                               | V <sub>CC</sub> = 2.3 V to 2.7 V                       | -                | 13.0    | -   | -                 | -    | pF   |
|                    |                               | V <sub>CC</sub> = 3.0 V to 3.6 V                       | -                | 15.0    | -   | -                 | -    | pF   |

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

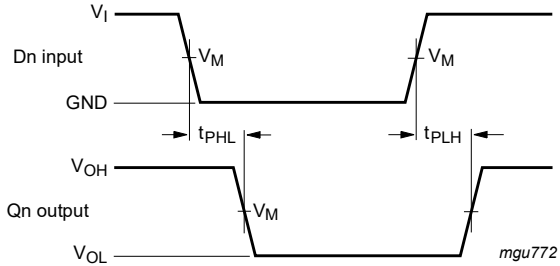
V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

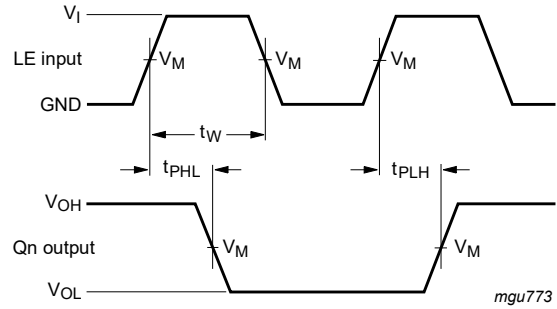


### 10.1. Waveforms and test circuit



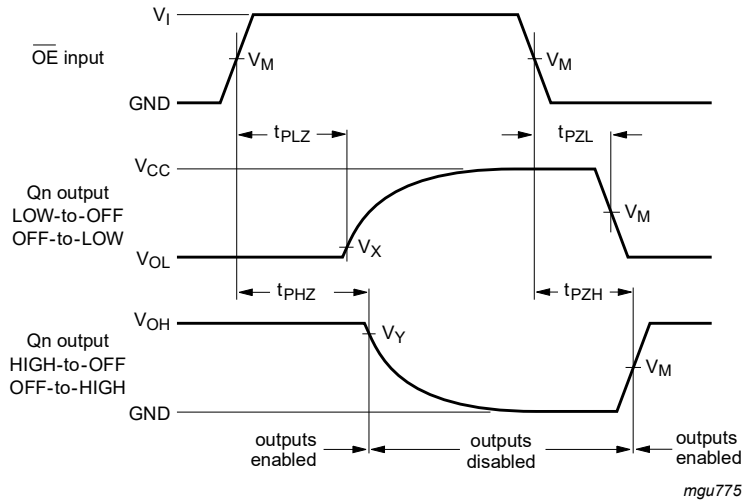
Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 6. Input (Dn) to output (Qn) propagation delays**



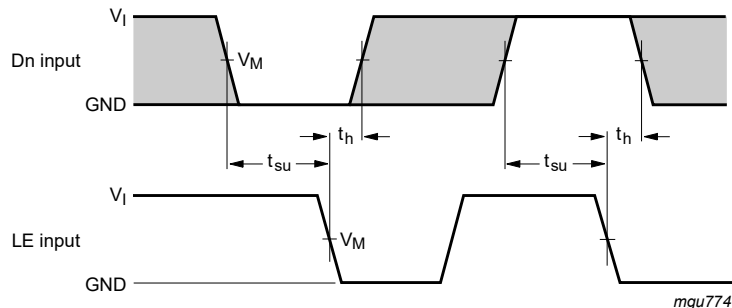
Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 7. Latch enable input (LE) pulse width, and the latch enable input to output (Qn) propagation delays**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 8. 3-state enable and disable times**

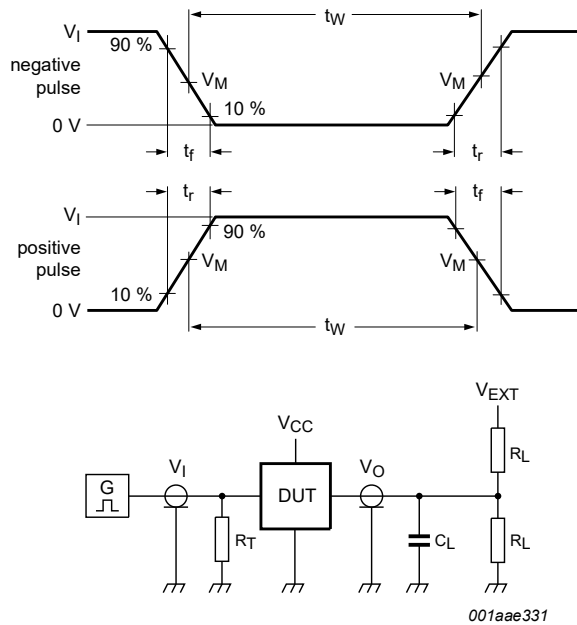


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.  
 The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 9. Data set-up and hold times for the Dn input to the LE input**

**Table 8. Measurement points**

| Supply voltage   | Input    |                     | Output              |                           |                           |
|------------------|----------|---------------------|---------------------|---------------------------|---------------------------|
| $V_{CC}$         | $V_I$    | $V_M$               | $V_M$               | $V_X$                     | $V_Y$                     |
| 1.2 V            | $V_{CC}$ | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |
| 2.3 V to 2.7 V   | $V_{CC}$ | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |
| 2.7 V            | 2.7 V    | 1.5 V               | 1.5 V               | $V_{OL} + 0.3 \text{ V}$  | $V_{OH} - 0.3 \text{ V}$  |
| 3.0 V to 3.6 V   | 2.7 V    | 1.5 V               | 1.5 V               | $V_{OL} + 0.3 \text{ V}$  | $V_{OH} - 0.3 \text{ V}$  |



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 10. Test circuit for measuring switching times**

**Table 9. Test data**

| Supply voltage   | Input    |                       | Load  |              | $V_{EXT}$          |                    |                    |
|------------------|----------|-----------------------|-------|--------------|--------------------|--------------------|--------------------|
| $V_{CC}$         | $V_I$    | $t_r, t_f$            | $C_L$ | $R_L$        | $t_{PLH}, t_{PHL}$ | $t_{PLZ}, t_{PZL}$ | $t_{PHZ}, t_{PZH}$ |
| 1.2 V            | $V_{CC}$ | $\leq 2 \text{ ns}$   | 30 pF | 1 k $\Omega$ | open               | $2 \times V_{CC}$  | GND                |
| 1.65 V to 1.95 V | $V_{CC}$ | $\leq 2 \text{ ns}$   | 30 pF | 1 k $\Omega$ | open               | $2 \times V_{CC}$  | GND                |
| 2.3 V to 2.7 V   | $V_{CC}$ | $\leq 2 \text{ ns}$   | 30 pF | 500 $\Omega$ | open               | $2 \times V_{CC}$  | GND                |
| 2.7 V            | 2.7 V    | $\leq 2.5 \text{ ns}$ | 50 pF | 500 $\Omega$ | open               | $2 \times V_{CC}$  | GND                |
| 3.0 V to 3.6 V   | 2.7 V    | $\leq 2.5 \text{ ns}$ | 50 pF | 500 $\Omega$ | open               | $2 \times V_{CC}$  | GND                |

### 11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

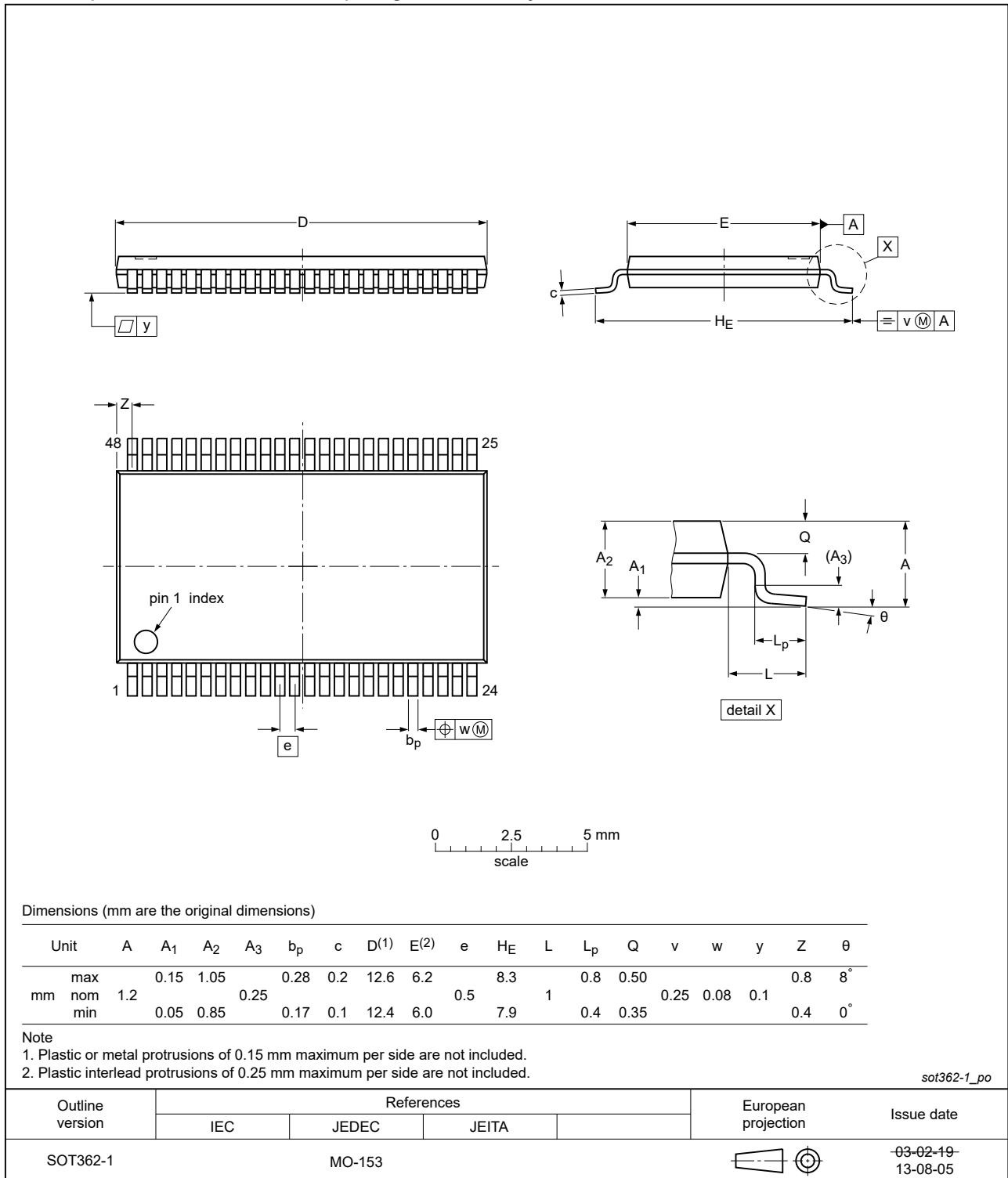


Fig. 11. Package outline SOT362-1 (TSSOP48)

# 74LVC16373A; 74LVCH16373A

16-bit D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

TVSOP48: plastic thin shrink small outline package; 48 leads;  
body width 4.4 mm; lead pitch 0.4 mm

SOT480-1

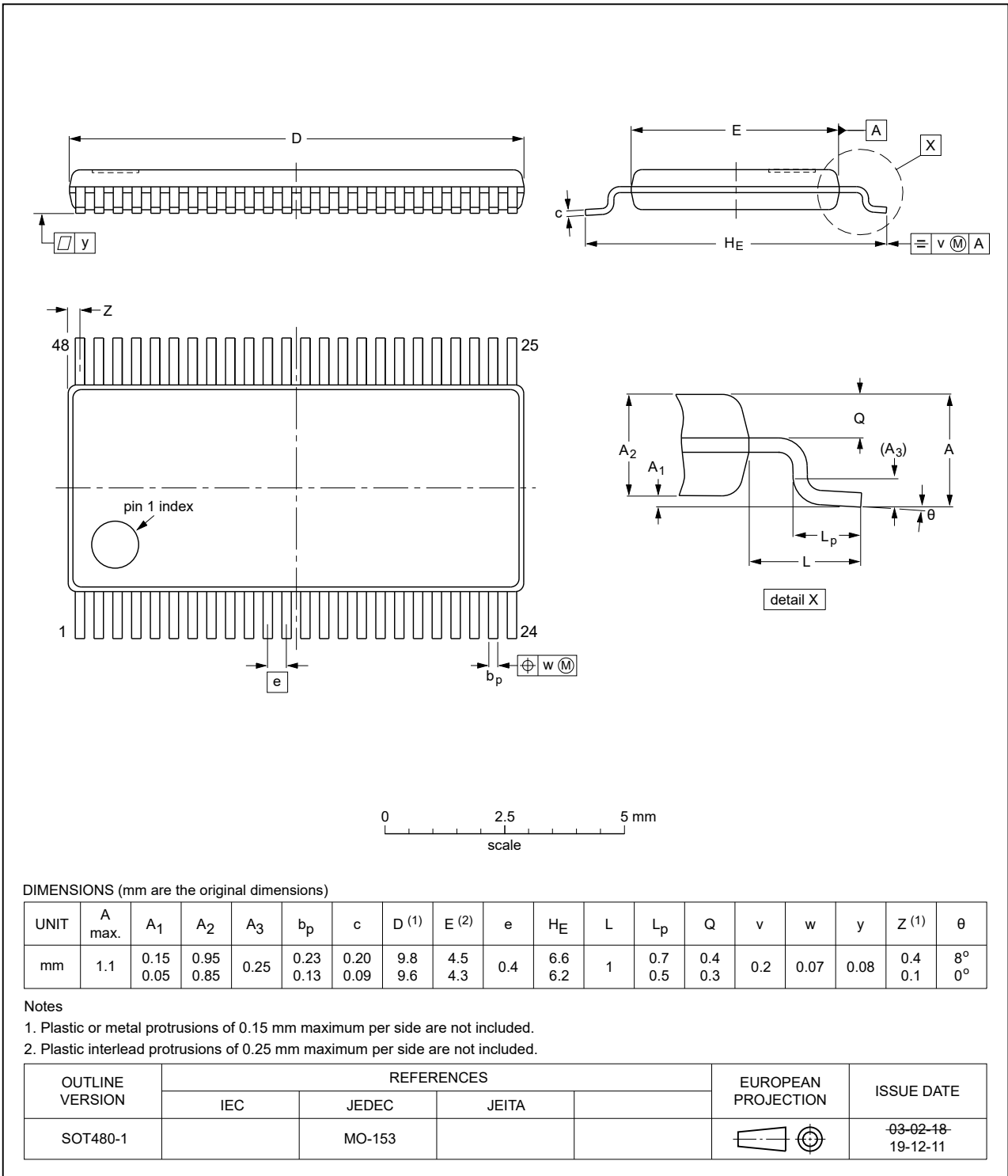


Fig. 12. Package outline SOT480-1 (TVSOP48)

## 12. Abbreviations

Table 10. Abbreviations

| Acronym | Description                             |
|---------|---|
| CDM     | Charged Device Model                    |
| CMOS    | Complementary Metal-Oxide Semiconductor |
| DUT     | Device Under Test                       |
| ESD     | ElectroStatic Discharge                 |
| HBM     | Human Body Model                        |
| MM      | Machine Model                           |
| TTL     | Transistor-Transistor Logic             |

## 13. Revision history

Table 11. Revision history

| Document ID                      | Release date  | Data sheet status     | Change notice | Supersedes                       |
|----------------------------------|---|-----------------------|---------------|----------------------------------|
| 74LVC_LVCH16373A v.10            | 20211001  | Product data sheet    | -             | 74LVC_LVCH16373A v.9             |
| Modifications:                   | <ul style="list-style-type: none"> <li>Type number 74LVC16373ADL (SOT370-1/SSOP48) removed.</li> <li>Package outline drawing <a href="#">SOT480-1</a> updated.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>   |                       |               |                                  |
| 74LVC_LVCH16373A v.9             | 20190215  | Product data sheet    | -             | 74LVC_LVCH16373A v.8             |
| Modifications:                   | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74LVCH16373ADL (SOT370-1) removed.</li> <li>Type numbers 74LVC16373ADGV and 74LVCH16373ADGV (SOT480-1) added.</li> </ul>   |                       |               |                                  |
| 74LVC_LVCH16373A v.8             | 20140106  | Product data sheet    | -             | 74LVC_LVCH16373A v.7             |
| Modifications:                   | <ul style="list-style-type: none"> <li>General description corrected (errata).</li> </ul>   |                       |               |                                  |
| 74LVC_LVCH16373A v.7             | 20130118  | Product data sheet    | -             | 74LVC_LVCH16373A v.6             |
| Modifications:                   | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, <a href="#">Table 8</a> and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul> |                       |               |                                  |
| 74LVC_LVCH16373A v.6             | 20031208  | Product specification | -             | 74LVC_LVCH16373A v.5             |
| 74LVC_LVCH16373A v.5             | 20021002  | Product specification | -             | 74LVC_H16373A v.4                |
| 74LVC_H16373A v.4                | 19980317  | Product specification | -             | 74LVC16373A_<br>74LVCH16373A v.3 |
| 74LVC16373A_<br>74LVCH16373A v.3 | 19980317  | Product specification | -             | 74LVC16373A v.2                  |
| 74LVC16373A v.2                  | 19970822  | Product specification | -             | 74LVC16373A v.1                  |
| 74LVC16373A v.1                  | 19960108  | -                     | -             | -                                |

## 14. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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