SGM41570

SMBus NVDC Buck-Boost Battery Charge Controller with System Power Monitor and Processor Hot Monitor

FEATURES

- 1- to 4-Cell Charging from a Variety of Input Types
  - 3.58V to 24V Input Operating Voltage Range
  - USB 2.0/3.0/3.1 (Type C)/USB-PD Input Current Support
  - Seamless Buck ↔ Buck-Boost ↔ Boost Transitions
  - Input Overload Protection (IDPM and VDPM Regulation)
- CPU Throttling, Power and Current Monitoring
  - Full nPROCHOT Profile IMVP8/IMVP9 Compliant
  - Input Current Monitoring
  - Battery Charge/Discharge Current Monitoring
  - System Power Monitoring, IMVP8/IMVP9 Compliant
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with Depleted or No Battery
  - Battery Supplementation if Adapter is Fully Loaded
  - BATFET Ideal Diode Emulation in Supplement Mode
- Power-Up USB Port from Battery (USB OTG)
  - 3V to 20.56V Adjustable OTG Voltage with 8mV Resolution
  - Up to 6.35A Output Current Limit with 50mA Resolution
- Pass Through Mode (PTM) to Improve Efficiency
- V_{MIN} Active Protection (VAP) Mode
- VAP Supplements Battery from Input Caps for System Power Spikes (Battery-Only Conditions)
- Input Current Optimizer Maximizes Power Extraction
- 800kHz or 1.2MHz Selectable Switching Frequency
- SMBus Interface for Flexible System Configuration
- Input Current Limit Setting Pin (without SMBus)
- Integrated ADC for Voltage/Current/Power Monitoring
- Low Battery Quiescent Current
- High Accuracy
  - TBD% for Charge Voltage Regulation
  - TBD% for Input/Charge Current Regulation
  - TBD% for Input/Charge Current Monitor
  - TBD% for Power Monitor
- Safety
  - Thermal Shutdown
  - Input/System/Battery Over-Voltage Protection
  - Input/MOSFET/Inductor Over-Current Protection
- Available in a Green TQFN-4×4-32AL Package

APPLICATIONS

Bluetooth Speakers, Drones, IP Cameras, Detachable Power Supply

Portable Internet Devices and Accessory

Industrial and Medical Equipment

TYPICAL APPLICATION

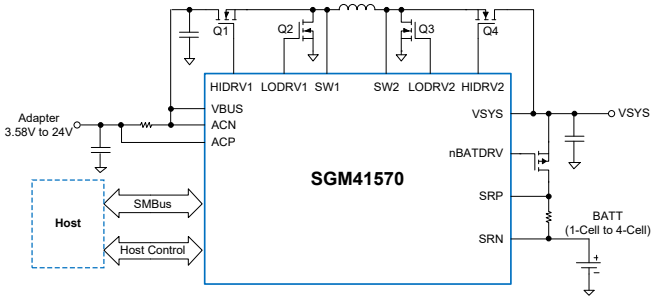


Figure 1. Typical Application Circuit

GENERAL DESCRIPTION

The SGM41570 is a synchronous Buck-Boost battery charge controller with NVDC power path management. It can provide high efficiency and low component count solution for 1-cell to 4-cell battery charging applications.

The system is regulated slightly above battery voltage and not below the programmable system minimum voltage. Therefore, system power is maintained even if the battery is completely depleted or removed. Dynamic power management (DPM) feature is also included that automatically reduces the charge current if the input current or voltage limit is reached. If the system load continues to increase after reduction of charge current down to zero, the battery goes into supplement mode and both adapter and battery power the system.

A wide range of input sources are supported for SGM41570, including traditional adapters, USB adapter and high voltage USB PD sources. Depending on the input source and battery conditions, the converter is configured as Buck, Boost or Buck-Boost during power-up. The charger automatically transition among Buck, Boost and Buck-Boost and requires no host control.

When input source is absent, SGM41570 can work in USB On-The-Go (OTG) mode to supply VBUS from battery. The OTG output voltage can be programmed from 3V to 20.56V with 8mV resolution, and the output voltage transition slew rate can be configurable, which is complied with the USB PD 3.0 PPS specifications.

If there is no external load on the USB OTG port and the system is powered by battery only, the V_{MIN} Active Protection (VAP) feature is supported. In VAP, the VBUS voltage is charged up by the battery and the energy is stored in the input decoupling capacitors. When the system demands power spike, the stored energy will supplement the system to prevent the system voltage from dropping below the minimum system voltage.

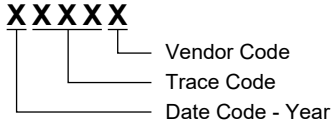
Adapter current, battery current and system power are monitored in SGM41570. When system power is too high and exceeds available power from adapter and battery together, a flexibly programmed nPROCHOT pulse is asserted to inform CPU for throttle back.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41570	TQFN-4×4-32AL	-40℃ to +125℃	SGM41570XTSE32G/TR	SGM41570 XTSE32 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- SRN, SRP, ACN, ACP, VBUS, VSYS ..... -0.3V to 30V
- SW1, SW2 ..... -2V to 30V
- BTST1, BTST2, HIDRV1, HIDRV2, nBATDRV ..... -0.3V to 36V
- LODRV1, LODRV2 (25ns) ..... -4V to 7V
- HIDRV1, HIDRV2 (25ns) ..... -4V to 36V
- SW1, SW2 (25ns) ..... -4V to 30V
- SDA, SCL, REGN, PSYS, CHRG_OK, OTG/VAP, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, nPROCHOT, CMPIN, CMPOUT ..... -0.3V to 7V
- COMP1, COMP2 ..... -0.3V to 5.5V
- IADPT, IBAT, PSYS ..... -0.3V to 3.6V

Differential Voltage
- BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2 ..... -0.3V to 7V
- SRP-SRN, ACP-ACN ..... -0.5V to 0.5V

Package Thermal Resistance
- TQFN-4×4-32AL, θ_{JA} ..... TBD℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

RECOMMENDED OPERATING CONDITIONS

Voltage Range (with Respect to GND)
- ACN, ACP, VBUS ..... 0V to 24V
- SRN, SRP, VSYS ..... 0V to 19.2V
- SW1, SW2 ..... -2V to 24V
- BTST1, BTST2, HIDRV1, HIDRV2, nBATDRV ..... 0V to 30V
- SDA, SCL, REGN, PSYS, CHRG_OK, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP1, COMP2, CMPIN, CMPOUT ..... 0V to 6.5V
- nPROCHOT ..... 0V to 5.3V
- IADPT, IBAT, PSYS ..... 0V to 3.3V

Differential Voltage Range (with Respect to GND)
- BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2 ..... 0V to 6.5V
- SRP-SRN, ACP-ACN ..... -0.5V to 0.5V

Operating Junction Temperature Range ..... -40℃ to +85℃

ESD SENSITIVITY CAUTION

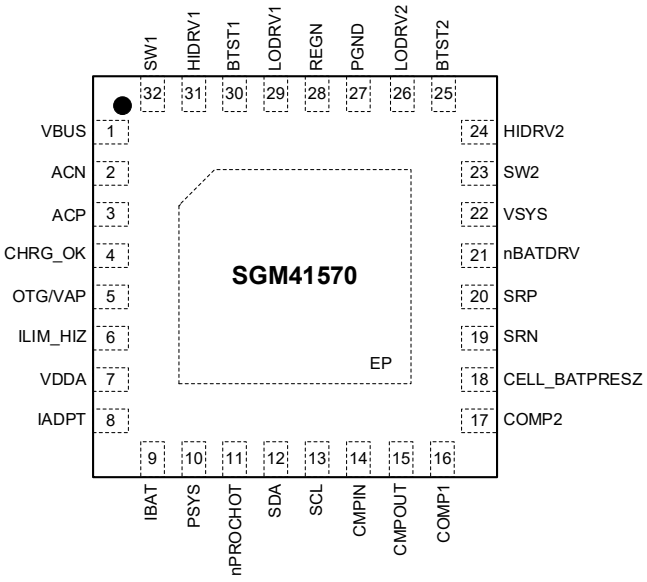
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-32AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	VBUS	PWR	Charger Input. Place an RC low pass filter on this pin (R = 1Ω and C ≥ 0.47μF).
2	ACN	PWR	Negative Terminal of the Input Current Sense Resistor. Place an RC low pass filter between this pin and the sense resistor. The leakage current on ACN and ACP are matched.
3	ACP	PWR	Positive Terminal of the Input Current Sense Resistor. Place an RC low pass filter between this pin and the sense resistor. The leakage current on ACN and ACP are matched.
4	CHRG_OK	O	Active High Open-Drain Good Power Source Status Output. Place a 10kΩ resistor between this pin and pull-up rail. CHRG_OK goes high after 50ms deglitch time when VBUS rises above 3.58V or falls below 23.9V. CHRG_OK goes low when VBUS falls below 3.21V or rises above 25.8V.
5	OTG/VAP	I	OTG or VAP Modes Enable Input (Active High). OTG mode enable: OTG_VAP_MODE bit = 1, EN_OTG bit = 1 and pull this pin to high. VAP mode enable: OTG_VAP_MODE bit = 0, and pull this pin to high.
6	ILIM_HIZ	I	Input Current Limit Setting Input. Connect this pin to a resistor divider between supply and ground to set the target input current limit I_{DPM} using the following equation: $V_{ILIM\_HIZ} = 1V + 40 \times I_{DPM} \times R_{AC}$ The actual input current limit is the lower setting of ILIM_HIZ pin and IIN_HOST register. The device enters HIZ mode when $V_{ILIM\_HIZ} < V_{HIZ\_LOW}$, and exits HIZ mode when $V_{ILIM\_HIZ} > V_{HIZ\_HIGH}$.
7	VDDA	PWR	Internal Reference Bias. Place a 10Ω resistor from REGN to this pin, and place a 1μF ceramic capacitor from this pin to ground.
8	IADPT	O	Adapter Current Monitoring Output. V_{IADPT} = 20 or 40 × (V_{ACP} - V_{ACN}) and 20 or 40 can be selected in the IADPT_GAIN bit. Place a resistor corresponding to the inductance in use from this pin to ground. The resistor is 137kΩ when L = 2.2μH. Connect a 100pF or less ceramic decoupling capacitor from this pin to ground. IADPT output voltage is clamped below V_{IADPT_CLAMP}.
9	IBAT	O	Battery Current Monitoring Output. The charge current is monitored as V_{IBAT} = 8 or 16 × (V_{SRP} - V_{SRN}), and discharge current is monitored as V_{IBAT} = 8 or 16 × (V_{SRN} - V_{SRP}), 8 or 16 can be selected in the IBAT_GAIN bit. Connect a 100pF or less ceramic decoupling capacitor from this pin to ground. IBAT pin can be left floating if not in use and its output voltage is clamped below V_{IBAT_CLAMP}.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
10	PSYS	O	System Power Monitoring Output (Current Mode). The output current of this pin is proportional to the total power from the adapter and the battery. The gain is selectable through SMBus. Place a resistor from this pin to ground to generate output voltage. PSYS pin can be left floating if not in use and its output voltage is clamped below V_{PSYS_CLAMP}.
11	nPROCHOT	O	Active Low Open-Drain Processor Hot Indicator Output. The adapter input current, battery discharge current and system voltage are monitored, and a pulse is asserted if any event in the nPROCHOT profile is triggered. The minimum pulse width is adjustable in PROCHOT_WIDTH[1:0] bits.
12	SDA	I/O	SMBus Data Signal. Use a 10kΩ pull-up to the logic high rail.
13	SCL	I	SMBus Clock Signal. Use a 10kΩ pull-up to the logic high rail.
14	CMPIN	I	Independent Comparator Input. The voltage sensed on this pin is compared with internal reference by the independent comparator, and the output of comparator is on CMPOUT pin. The Internal reference, output polarity and deglitch time are all selectable in the SMBus host. When CMP_POL bit = 1, the internal hysteresis is determined by the resistor between CMPIN and CMPOUT. When CMP_POL bit = 0, the internal hysteresis is 103mV. Connect this pin to ground if the independent comparator is not in use.
15	CMPOUT	O	Open-Drain Independent Comparator Output. Place a resistor between this pin and pull-up supply rail.
16	COMP1	I	Buck Boost Compensation Pin 1. Refer to Figure 2 for the compensation network.
17	COMP2	I	Buck Boost Compensation Pin 2. Refer to Figure 2 for the compensation network.
18	CELL_BATPRESZ	I	Battery Cell Selection Input. This pin is biased from VDDA, and sets the SYSOVP thresholds (5V for 1-cell, 12V for 2-cell, and 19.4V for 3-cell/4-cell). When the voltage on this pin is pulled below $V_{CELL\_BATPRESZ\_FALL}$, it indicates battery removal. The device exits LEARN mode, charge is disabled, and the charge voltage register MaxChargeVoltage goes to default.
19	SRN	PWR	Negative Input of the Charge Current Sense Resistor. This pin also senses the battery voltage. Place an optional 0.1μF ceramic capacitor from this pin to GND for common-mode noise filtering. Place a 0.1μF ceramic capacitor from SRP to SRN for differential mode noise filtering. The leakage current on SRP and SRN are matched.
20	SRP	PWR	Positive Input of the Charge Current Sense Resistor. Place an optional 0.1μF ceramic capacitor from this pin to GND for common-mode noise filtering. Place a 0.1μF ceramic capacitor from SRP to SRN for differential mode noise filtering. The leakage current on SRP and SRN are matched.
21	nBATDRV	O	P-Channel BATFET Gate Driver Output. It is shorted to VSYS for turning off the BATFET and goes 10V below VSYS for fully on.
22	VSYS	PWR	System Voltage. The system voltage regulation limit is programmed in MaxChargeVoltage registers.
23	SW2	PWR	Boost Mode Switching Node. Connect it to the source of the Boost mode high-side N-channel MOSFET (Q4).
24	HIDRV2	O	Boost Mode High-side N-Channel MOSFET (Q4) Driver. Connect to the gate of Q4.
25	BTST2	PWR	Boost Mode High-side N-Channel MOSFET (Q4) Driver Power Supply. Place a 47nF capacitor between SW2 and BTST2. The bootstrap diode between REGN and BTST2 is integrated.
26	LODRV2	O	Boost Mode Low-side N-Channel MOSFET (Q3) Driver. Connect to the gate of Q3.
27	PGND	GND	Power Ground.
28	REGN	PWR	6V LDO Output. It's supplied from VBUS or VSYS and the LDO is active when VBUS voltage is above V_{VBUS_CONVEN}. A 2.2μF or 3.3μF ceramic capacitor is recommended between this pin and PGND.
29	LODRV1	O	Buck Mode Low-side N-Channel MOSFET (Q2) Driver. Connect to the gate of Q2.
30	BTST1	PWR	Buck Mode High-side N-Channel MOSFET (Q1) Driver Power Supply. Place a 47nF capacitor between SW1 and BTST1. The bootstrap diode between REGN and BTST1 is integrated.
31	HIDRV1	O	Buck Mode High-side N-Channel MOSFET (Q1) driver. Connect to the gate of Q1.
32	SW1	PWR	Buck Mode Switching Node. Connect it to the source of the Buck mode high-side N-channel MOSFET (Q1).
Exposed Pad	EP		Thermal Pad. It's the thermal pad to conduct heat from the device. Tie externally to the PCB power ground plane. Thermal vias under the pad are needed to conduct the heat to the PCB power ground planes.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Operating Range	V_{INPUT_OP}			3.58		24	V
Regulation Accuracy							
Max System Voltage Regulation							
System Voltage Regulation	V_{SYSMAX_RNG}	Charge disabled, measured on V_{SYS}		1.024		19.2	V
System Voltage Regulation Accuracy	V_{SYSMAX_ACC}	Charge disabled	MaxChargeVoltage register = 0x41A0 (16.800V)		17.02		V
				TBD		TBD	%
			MaxChargeVoltage register = 0x3138 (12.600V)		12.82		V
				TBD		TBD	%
			MaxChargeVoltage register = 0x20D0 (8.400V)		8.61		V
				TBD		TBD	%
			MaxChargeVoltage register = 0x1068 (4.200V)		4.41		V
				TBD		TBD	%
Minimum System Voltage Regulation							
System Voltage Regulation	V_{SYSMIN_RNG}	Measured on V_{SYS}		1.024		16.128	V
Minimum System Voltage Regulation Accuracy	$V_{SYSMIN\_REG\_ACC}$	VBAT below MinSystemVoltage register setting	MinSystemVoltage register = 0x3000		12.27		V
				TBD		TBD	%
			MinSystemVoltage register = 0x2400		9.22		V
				TBD		TBD	%
			MinSystemVoltage register = 0x1800		6.16		V
				TBD		TBD	%
			MinSystemVoltage register = 0x0E00		3.61		V
				TBD		TBD	%
Charge Voltage Regulation							
Battery Voltage Regulation	V_{BAT_RNG}			1.024		19.2	V
Battery Voltage Regulation Accuracy	$V_{BAT\_REG\_ACC}$	Charge enable (0℃ to +85℃)	MaxChargeVoltage register = 0x41A0		16.788		V
				TBD		TBD	%
			MaxChargeVoltage register = 0x3138		12.6		V
				TBD		TBD	%
			MaxChargeVoltage register = 0x20D0		8.407		V
				TBD		TBD	%
			MaxChargeVoltage register = 0x1068		4.206		V
				TBD		TBD	%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Current Regulation in Fast Charge							
Charge Current Regulation Differential Voltage Range	$V_{IREG\_CHG\_RNG}$	V_{IREG_CHG} = V_{SRP} - V_{SRN}		0		81.28	mV
Charge Current Regulation Accuracy with 10mΩ Sensing Resistor	$I_{CHRG\_REG\_ACC}$	VBAT above MinSystemVoltage register setting (0℃ to +85℃)	ChargeCurrent register = 0x1000		4053		mA
				TBD		TBD	%
			ChargeCurrent register = 0x0800		2019		mA
				TBD		TBD	%
			ChargeCurrent register = 0x0400		999		mA
				TBD		TBD	%
			ChargeCurrent register = 0x0200		490		mA
				TBD		TBD	%
Charge Current Regulation in LDO Mode							
Pre-Charge Current Clamp	I_{CLAMP}	2-cell to 4-cell			384		mA
		1-cell, V_{SRN} < 3V			384		mA
		1-cell, 3V < V_{SRN} < V_{SYSMIN}			2		A
Pre-Charge Current Regulation Accuracy with 10mΩ SRP/SRN Series Resistor	$I_{PRECHRG\_REG\_ACC}$	VBAT below MinSystemVoltage register setting (0℃ to +85℃)	ChargeCurrent register = 0x0180		384		mA
			2-cell to 4-cell	TBD		TBD	%
			1-cell	TBD		TBD	%
			ChargeCurrent register = 0x0100		256		mA
			2-cell to 4-cell	TBD		TBD	%
			1-cell	TBD		TBD	%
			ChargeCurrent register = 0x00C0		192		mA
			2-cell to 4-cell	TBD		TBD	%
			1-cell	TBD		TBD	%
			ChargeCurrent register = 0x0080		128		mA
			2-cell to 4-cell	TBD		TBD	%
SRP, SRN Leakage Current Mismatch	$I_{LEAK\_SRP\_SRN}$	0℃ to +85℃		-12		10	μA
Input Current Regulation							
Input Current Regulation Differential Voltage Range	$V_{IREG\_DPM\_RNG}$	V_{IREG_DPM} = V_{ACP} - V_{ACN}		0.5		63.5	mV
Input Current Regulation Accuracy with 10mΩ ACP/ACN Series Resistor	$I_{DPM\_REG\_ACC}$	-40℃ to +105℃	IIN_HOST register = 0x5000	TBD	3850	TBD	mA
			IIN_HOST register = 0x3C00	TBD	2853	TBD	
			IIN_HOST register = 0x1E00	TBD	1405	TBD	
			IIN_HOST register = 0x0A00	TBD	448	TBD	
ACP, ACN Leakage Current Mismatch	$I_{LEAK\_ACP\_\_ACN}$	-40℃ to +105℃		-16		10	μA
Voltage Range for Input Current Regulation (ILIM_HIZ Pin)	$V_{IREG\_DPM\_RNG\_ILIM}$			1.15		4	V
Input Current Regulation Accuracy on ILIM_HIZ Pin with 10mΩ ACP/ACN Series Resistor	$I_{DPM\_REG\_ACC\_ILIM}$	V_{ILIM_HIZ} = 1V + 40 × I_{DPM} × R_{AC}	V_{ILIM_HIZ} = 2.6V	TBD	4023	TBD	mA
			V_{ILIM_HIZ} = 2.2V	TBD	3024	TBD	
			V_{ILIM_HIZ} = 1.6V	TBD	1522	TBD	
			V_{ILIM_HIZ} = 1.2V	TBD	524	TBD	
ILIM_HIZ Pin Leakage Current	I_{LEAK_ILIM}			TBD	0.01	TBD	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Regulation						
Input Voltage Regulation Range	$V_{IREG\_DPM\_RNG}$	Voltage on VBUS	3.2		19.52	V
Input Voltage Regulation Accuracy	$V_{DPM\_REG\_ACC}$	InputVoltage register = 0x3C80		18607		mV
			TBD		TBD	%
		InputVoltage register = 0x1E00		10835		mV
			TBD		TBD	%
		InputVoltage register = 0x0500		4465		mV
			TBD		TBD	%
OTG Current Regulation						
OTG Output Current Regulation Differential Voltage Range	$V_{IOTG\_REG\_RNG}$	$V_{IOTG\_REG} = V_{ACP} - V_{ACN}$	0		63.5	mV
OTG Output Current Regulation Accuracy with 50mA LSB and 10mΩ ACP/ACN Series Resistor	I_{OTG_ACC}	OTGCurrent register = 0x3C00	TBD	2967	TBD	mA
		OTGCurrent register = 0x1E00	TBD	1474	TBD	
		OTGCurrent register = 0x0A00	TBD	478	TBD	
OTG Voltage Regulation						
OTG Voltage Regulation Range	$V_{OTG\_REG\_RNG}$	Voltage on VBUS	3		20.56	V
OTG Voltage Regulation Accuracy	$V_{OTG\_REG\_ACC}$	OTGVoltage register = 0x23F8, OTG_RANGE_LOW = 0		19.621		V
			TBD		TBD	%
		OTGVoltage register = 0x1710, OTG_RANGE_LOW = 1		11.779		V
			TBD		TBD	%
		OTGVoltage register = 0x099CH, OTG_RANGE_LOW = 1		4.928		V
			TBD		TBD	%
Reference and Buffer						
REGN Regulator						
REGN Regulator Voltage (0mA to 60mA)	V_{REGN_REG}	V_{VBUS} = 10V	TBD	6.15	TBD	V
REGN Voltage in Drop Out Mode	$V_{DROPOUT}$	V_{VBUS} = 5V, I_{LOAD} = 20mA	TBD	4.8	TBD	V
REGN Current Limit when Converter is Enabled	$I_{REGN\_LIM\_Charging}$	V_{VBUS} = 10V, force V_{REGN} = 4V	TBD	106		mA
REGN Output Capacitor Required for Stability	C_{REGN}	I_{LOAD} = 100μA to 50mA	2.2			μF
VDDA Input Capacitor Required for Stability	C_{VDDA}	I_{LOAD} = 100μA to 50mA	1			μF

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current							
System Powered by Battery, BATFET on, I_{SRN} + I_{SRP} + I_{SW2} + I_{BTST2} + I_{SW1} + I_{BTST1} + I_{ACP} + I_{ACN} + I_{VBUS} + I_{VSYS}	$I_{BAT\_BATFET\_ON}$	V_{BAT} = 18V, EN_LWPWR = 1, in low power mode			21.13	TBD	μA
		V_{BAT} = 18V, EN_LWPWR = 1, EN_PROCHOT_LPWR = 1, REGN off			186.41	TBD	
		V_{BAT} = 18V, EN_LWPWR = 0, EN_PSYS = 0, REGN on, DIS_PSYS			1146	TBD	
		V_{BAT} = 18V, EN_LWPWR = 0, EN_PSYS = 1, REGN on, EN_PSYS			1260	TBD	
Input Current during PFM in Buck Mode, No Load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	$I_{AC\_SW\_LIGHT\_buck}$	V_{IN} = 20V, V_{BAT} = 12.6V, 3-cell, EN_OOA = 0, MOSFET Qg = 4nC			2.5		mA
Input Current during PFM in Boost Mode, No Load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	$I_{AC\_SW\_LIGHT\_boost}$	V_{IN} = 5V, V_{BAT} = 8.4V, 2-cell, EN_OOA = 0, MOSFET Qg = 4nC			6.7		mA
Input Current during PFM in Buck Boost Mode, No Load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	$I_{AC\_SW\_LIGHT\_buckboost}$	V_{IN} = 12V, V_{BAT} = 12V, EN_OOA = 0, MOSFET Qg = 4nC			3.3		mA
Quiescent Current during PFM in OTG Mode, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	$I_{OTG\_STANDBY}$	V_{BAT} = 8.4V, 800kHz switching frequency, MOSFET Qg = 4nC	V_{VBUS} = 5V		3.3		mA
			V_{VBUS} = 12V		3.6		
			V_{VBUS} = 20V		4		
Input Common Mode Range	V_{ACP/N_OP}	Voltage on ACP/ACN		3.8		24	V
IADPT Output Clamp Voltage	V_{IADPT_CLAMP}			TBD	3.18	TBD	V
IADPT Output Current	I_{IADPT}					1	mA
Input Current Sensing Gain	A_{IADPT}	$V_{IADPT}/V_{(ACP-ACN)}$	IADPT_GAIN = 0		20		V/V
			IADPT_GAIN = 1		40		
Input Current Monitor Accuracy	V_{IADPT_ACC}	$V_{(ACP-ACN)}$ = 40.96mV		TBD	0.74	TBD	%
		$V_{(ACP-ACN)}$ = 20.48mV		TBD	1.39	TBD	
		$V_{(ACP-ACN)}$ =10.24mV		TBD	2.52	TBD	
		$V_{(ACP-ACN)}$ = 5.12mV		TBD	5.23	TBD	
Maximum Capacitance on IADPT Pin	C_{IADPT_MAX}					100	pF
Battery Common Mode Range	V_{SRP/N_OP}	Voltage on SRP/SRN		2.5		18	V
IBAT Output Clamp Voltage	V_{IBAT_CLAMP}			TBD	3.28	TBD	V
IBAT Output Current	I_{IBAT}					1	mA
Charge and Discharge Current Sensing Gain on IBAT Pin	A_{IBAT}	$V_{IBAT}/V_{(SRN-SRP)}$	IBAT_GAIN = 0		8		V/V
			IBAT_GAIN = 1		16		
Charge and Discharge Current Monitor Accuracy on IBAT Pin	$V_{IBAT\_CHG\_ACC}$	$V_{(SRN-SRP)}$ = 40.96mV		TBD	1.53	TBD	%
		$V_{(SRN-SRP)}$ = 20.48mV		TBD	2.32	TBD	
		$V_{(SRN-SRP)}$ =10.24mV		TBD	3.81	TBD	
		$V_{(SRN-SRP)}$ = 5.12mV		TBD	7.24	TBD	
Maximum Capacitance on IBAT Pin	C_{IBAT_MAX}					100	pF

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Power Sense Amplifier						
PSYS Output Voltage Range	V_{PSYS}		0		3.3	V
PSYS Output Current	I_{PSYS}		0		160	μA
PSYS System Gain	A_{PSYS}	$V_{PSYS}/(P_{IN}+P_{BAT})$, PSYS_RATIO = 1		1		μA/W
PSYS Gain Accuracy	V_{PSYS_ACC}	Adapter only with system power = 19.5V/45W, PSYS_RATIO = 1, T_A = -40°C to +85°C	TBD	1.7	TBD	%
		Battery only with system power = 11V/44W, PSYS_RATIO = 1, T_A = -40°C to +85°C	TBD	0.27	TBD	
PSYS Clamp Voltage	V_{PSYS_CLAMP}		TBD	3.3	TBD	V
Comparator						
VBUS Under-Voltage Lockout Comparator						
VBUS Under-Voltage Rising Threshold	V_{VBUS_UVLOZ}	VBUS rising	TBD	2.55	TBD	V
VBUS Under-Voltage Falling Threshold	V_{VBUS_UVLO}	VBUS falling	TBD	2.4	TBD	V
VBUS Under-Voltage Hysteresis	$V_{VBUS\_UVLO\_HYST}$			150		mV
VBUS Converter Enable Rising Threshold	V_{VBUS_CONVEN}	VBUS rising	TBD	3.58	TBD	V
VBUS Converter Enable Falling Threshold	$V_{VBUS\_CONVENZ}$	VBUS falling	TBD	3.21	TBD	V
VBUS Converter Enable Hysteresis	$V_{VBUS\_CONVEN\_HYST}$			377		mV
Battery Under-Voltage Lockout Comparator						
VBAT Under-Voltage Rising Threshold	V_{VBAT_UVLOZ}	VSRN rising	TBD	2.56	TBD	V
VBAT Under-Voltage Falling Threshold	V_{VBAT_UVLO}	VSRN falling	TBD	2.41	TBD	V
VBAT Under-Voltage Hysteresis	$V_{VBAT\_UVLO\_HYST}$			150		mV
VBAT OTG Enable Rising Threshold	V_{VBAT_OTGEN}	VSRN rising	TBD	3.57	TBD	V
VBAT OTG Enable Falling Threshold	V_{VBAT_OTGENZ}	VSRN falling	TBD	2.36	TBD	V
VBAT OTG Enable Hysteresis	$V_{VBAT\_OTGEN\_HYST}$			1208		mV
VBUS Under-Voltage Comparator (OTG Mode)						
VBUS Under-Voltage Falling Threshold	$V_{VBUS\_OTG\_UV}$	As percentage of OTGVoltage register		0.85		
VBUS Time Under-Voltage Deglitch	$t_{VBUS\_OTG\_UV}$			7		ms
VBUS Over-Voltage Comparator (OTG Mode)						
VBUS Over-Voltage Rising Threshold	$V_{VBUS\_OTG\_OV}$	As percentage of OTGVoltage register		1.1		
VBUS Time Over-Voltage Deglitch	$t_{VBUS\_OTG\_OV}$			10		ms
Pre-Charge to Fast Charge Transition						
LDO Mode to Fast Charge Mode Threshold	VSRN Rising	$V_{BAT\_SYSMIN\_RISE}$	As percentage of MinSystemVoltage register	TBD	99.51	TBD	%
	VSRN Falling	$V_{BAT\_SYSMIN\_FALL}$			97.88		
Fast Charge Mode to LDO Mode Threshold Hysteresis		$V_{BAT\_SYSMIN\_HYST}$	As percentage of MinSystemVoltage register		1.63		%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Battery LOWV Comparator (Pre-Charge to Fast Charge Threshold for 1-Cell)							
BATLOWV Falling Threshold	V_{BATLV_FALL}	1-cell			2.8		V
BATLOWV Rising Threshold	V_{BATLV_RISE}				3		V
BATLOWV Hysteresis	V_{BATLV_HYST}				193		mV
Input Over-Voltage Comparator (ACOVP)							
VBUS Over-Voltage Rising Threshold	V_{ACOV_RISE}	VBUS rising		TBD	25.8	TBD	V
VBUS Over-Voltage Falling Threshold	V_{ACOV_FALL}	VBUS falling		TBD	23.9	TBD	V
VBUS Over-Voltage Hysteresis	V_{ACOV_HYST}				1.9		V
VBUS Deglitch Over-Voltage Rising	$t_{ACOV\_RISE\_DEG}$	VBUS converter rising to stop converter			100		μs
VBUS Deglitch Over-Voltage Falling	$t_{ACOV\_FALL\_DEG}$	VBUS converter falling to start converter			1		ms
Input Over-Current Comparator (ACOC)							
ACP to ACN Rising Threshold, w.r.t. ILIM2 in ILIM2_VTH[4:0] Bits	V_{ACOC}	Voltage across input sense resistor rising, ACOC_VTH = 1		TBD	2	TBD	
Measure between ACP and ACN	V_{ACOC_FLOOR}	Set IDPM to minimum		TBD	50	TBD	mV
Measure between ACP and ACN	$V_{ACOC\_CEILING}$	Set IDPM to maximum		TBD	180	TBD	mV
Rising Deglitch Time	$t_{ACOC\_DEG\_RISE}$	Deglitch time to trigger ACOC			250		μs
Relax Time	t_{ACOC_RELAX}	Relax time before converter starts again			250		ms
System Over-Voltage Comparator (SYSOVP)							
System Over-Voltage Rising Threshold to Turn Off Converter	V_{SYSOVP_RISE}	1-cell		TBD	5	TBD	V
		2-cell		TBD	12	TBD	
		3-cell, 4-cell		TBD	19.4	TBD	
System Over-Voltage Falling Threshold	V_{SYSOVP_FALL}	1-cell			4.8		V
		2-cell			11.4		
		3-cell, 4-cell			18.8		
Discharge Current when SYSOVP Stop Switching is Triggered	I_{SYSOVP}	On VSYS pin			20		mA
BAT Over-Voltage Comparator (BATOVP)							
Over-Voltage Rising Threshold	V_{BATOVP_RISE}	As percentage of V_{BAT_REG} in MaxChargeVoltage register	1-cell, 4.2V	TBD	104.8	TBD	%
			2-cell to 4-cell	TBD	103.9	TBD	
Over-Voltage Falling Threshold	V_{BATOVP_FALL}	As percentage of V_{BAT_REG} in MaxChargeVoltage register	1-cell	TBD	101.6	TBD	%
			2-cell to 4-cell	TBD	101.5	TBD	
Over-Voltage Hysteresis	V_{BATOVP_HYST}	As percentage of V_{BAT_REG} in MaxChargeVoltage register	1-cell		3.1		%
			2-cell to 4-cell		2.4		
Discharge Current during BATOVP	I_{BATOVP}	On VSYS pin			20		mA
Over-Voltage Rising Deglitch to Turn Off Converter to Disable Charge	t_{BATOVP_RISE}				20		ms
Converter Over-Current Comparator (Q2)							
Converter Over-Current Limit	$V_{OCP\_limit\_Q2}$	Q2_OCP = 1			150		mV
		Q2_OCP = 0			210		
System Short or SRN < 2.4V	$V_{OCP\_limit\_SYS\ SHORT\_Q2}$	Q2_OCP = 1			45		mV
		Q2_OCP = 0			60		

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Converter Over-Current Comparator (ACX)						
Converter Over-Current Limit	$V_{OCP\_limit\_ACX}$	ACX_OCP = 1		151		mV
		ACX_OCP = 0		282		
System Short or SRN < 2.4V	$V_{OCP\_limit\_SYS\ SHORT\_ACX}$	ACX_OCP = 1		91		mV
		ACX_OCP = 0		151		
Thermal Shutdown Comparator						
Thermal Shutdown Rising Temperature	T_{SHUT_RISE}	Temperature increasing		155		℃
Thermal Shutdown Falling Temperature	$T_{SHUTF\_F\ ALL}$	Temperature reducing		135		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}			20		℃
Thermal Deglitch Shutdown Rising	t_{SHUT_RDEG}			100		μs
Thermal Deglitch Shutdown Falling	t_{SHUT_FHYS}			12		ms
VSYS PROCHOT Comparator						
VSYS_TH1 Comparator Falling Threshold	VSYS_TH1	VSYS_TH1[3:0] = 0111, 2-cell to 4-cell		6.6		V
		VSYS_TH1[3:0] = 0100, 1-cell		3.5		
VSYS_TH2 Comparator Falling Threshold	VSYS_TH2	VSYS_TH2[1:0] = 10, 2-cell to 4-cell		6.5		V
		VSYS_TH2[1:0] = 10, 1-cell		3.5		
V_{SYS} Falling Deglitch for Throttling	$t_{SYS\_PRO\_falling\_DEG}$			4		μs
ICRIT PROCHOT Comparator						
Input Current Rising Threshold for Throttling as 10% above ILIM2 (ILIM2_VTH[4:0] Bits)	V_{ICRIT_PRO}	Only when ILIM2 setting is higher than 2A	TBD	110	TBD	%
INOM PROCHOT Comparator						
INOM Rising Threshold as 10% above IIN (IIN_HOST Register)	V_{INOM_PRO}		TBD	110	TBD	%
IDCHG PROCHOT Comparator						
IDCHG Threshold for Throttling for IDSCHG of 6A	V_{IDCHG_PRO}	IDCHG_VTH[5:0] = 001100		6145		mA
			TBD		TBD	%
Independent Comparator						
Independent Comparator Threshold	V_{INDEP_CMP}	CMP_REF = 1, CMPIN falling	TBD	1.2	TBD	V
		CMP_REF = 0, CMPIN falling	TBD	2.3	TBD	
Independent Comparator Hysteresis	$V_{INDEP\_CMP\_HYS}$	CMP_POL = 0, CMPIN falling		103		mV
Power MOSFET Driver						
PWM Oscillator and Ramp						
PWM Switching Frequency	f_{SW}	PWM_FREQ = 0		1200		kHz
		PWM_FREQ = 1		800		
BATFET Gate Driver (BATDRV)						
Gate Drive Voltage on BATFET	V_{BATDRV_ON}		TBD	10.8	TBD	V
Drain-Source Voltage on BATFET during Ideal Diode Operation	V_{BATDRV_DIODE}			27		mV
Measured by Sourcing 10μA Current to BATDRV	R_{BATDRV_ON}		TBD	4.5	TBD	kΩ
Measured by Sinking 10μA Current from BATDRV	R_{BATDRV_OFF}			1.3	TBD	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM High-side Driver (HIDRV Q1)						
High-side Driver (HSD) Turn-On Resistance	$R_{DS\_HI\_ON\_Q1}$	V_{BTST1} - V_{SW1} = 5V		5.1		Ω
High-side Driver Turn-Off Resistance	$R_{DS\_HI\_OFF\_Q1}$	V_{BTST1} - V_{SW1} = 5V		1.1	TBD	Ω
Bootstrap Refresh Comparator Falling Threshold Voltage	$V_{BTST1\_REFRESH}$	V_{BTST1} - V_{SW1} when low-side refresh pulse is requested	TBD	3.9	TBD	V
PWM High-side Driver (HIDRV Q4)						
High-side Driver (HSD) Turn-On Resistance	$R_{DS\_HI\_ON\_Q4}$	V_{BTST2} - V_{SW2} = 5V		4.9		Ω
High-side Driver Turn-Off Resistance	$R_{DS\_HI\_OFF\_Q4}$	V_{BTST2} - V_{SW2} = 5V		1.2	TBD	Ω
Bootstrap Refresh Comparator Falling Threshold Voltage	$V_{BTST2\_REFRESH}$	V_{BTST2} - V_{SW2} when low-side refresh pulse is requested	TBD	3.9	TBD	V
PWM Low-side Driver (LODRV Q2)						
Low-side Driver (LSD) Turn-On Resistance	$R_{DS\_LO\_ON\_Q2}$	V_{BTST1} - V_{SW1} = 5.5V		4.6		Ω
Low-side Driver Turn-Off Resistance	$R_{DS\_LO\_OFF\_Q2}$	V_{BTST1} - V_{SW1} = 5.5V		1.3	TBD	Ω
PWM Low-side Driver (LODRV Q3)						
Low-side Driver (LSD) Turn-On Resistance	$R_{DS\_LO\_ON\_Q3}$	V_{BTST2} - V_{SW2} = 5.5V		4.7		Ω
Low-side Driver Turn-Off Resistance	$R_{DS\_LO\_OFF\_Q3}$	V_{BTST2} - V_{SW2} = 5.5V		1.2	TBD	Ω
Internal Soft-Start during Charge Enable						
Soft-Start Step Size	SSSTEP_DAC			64		mA
Soft-Start Step Time	t_{SSSTEP_DAC}			8		μs
Integrated BTST Diode (D1)						
Forward Bias Voltage	V_{F_D1}	I_F = 20mA at +25℃		0.8		V
Reverse Breakdown Voltage	V_{R_D1}	I_R = 2μA at +25℃			20	V
Integrated BTST Diode (D2)						
Forward Bias Voltage	V_{F_D2}	I_F = 20mA at +25℃		0.8		V
Reverse Breakdown Voltage	V_{R_D2}	I_R = 2μA at +25℃			20	V
Interface						
Logic Input (SDA, SCL, EN_OTG)						
Input Low Threshold	V_{IN_LO}	SMBus		0.6	TBD	V
Input High Threshold	V_{IN_HI}	SMBus	TBD	1.2		V
Logic Output Open Drain (SDA, CHRG_OK, CMPOUT)						
Output Saturation Voltage	V_{OUT_LO}	5mA drain current			0.4	V
Leakage Current	I_{OUT_LEAK}	Connected to 7V	-1		1	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Output Open-Drain (PROCHOT)						
Output Saturation Voltage	$V_{OUT\_LO\_PROCHOT}$	50Ω pull-up to 1.05V/5mA			300	mV
Leakage Current	$I_{OUT\_LEAK\_PROCHOT}$	Connected to 5.5V	-1		1	μA
Analog Input (ILIM_HIZ)						
Voltage to Get out of HIZ Mode	V_{HIZ_HIGH}	ILIM_HIZ pin rising	TBD	0.8		V
Voltage to Enable HIZ Mode	V_{HIZ_LOW}	ILIM_HIZ pin falling		0.6	TBD	V
Analog Input (CELL_BATPRESZ)						
4-Cell	V_{CELL_4S}	REGN of REGN = 6V, as percentage	TBD	75		%
3-Cell	V_{CELL_3S}	REGN of REGN = 6V, as percentage	TBD	55	TBD	%
2-Cell	V_{CELL_2S}	REGN of REGN = 6V, as percentage	TBD	40	TBD	%
Battery is Present	$V_{CELL\_BATPRESZ\_RISE}$	CELL_BATPRESZ rising	TBD	17.6		%
Battery is Removed	$V_{CELL\_BATPRESZ\_FALL}$	CELL_BATPRESZ falling		16.3	TBD	%

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMBus Timing Characteristics						
SCLK/SDATA Rise Time	t_R				300	ns
SCLK/SDATA Fall Time	t_F				300	ns
SCLK Pulse Width High	$t_{W(H)}$		0.6		50	μs
SCLK Pulse Width Low	$t_{W(L)}$		1.3			μs
Setup Time for START Condition	$t_{SU(STA)}$		0.6			μs
START Condition Hold Time after which First Clock Pulse is Generated	$t_{H(STA)}$		0.6			μs
Data Setup Time	$t_{SU(DAT)}$		100			ns
Data Hold Time	$t_{H(DAT)}$		300			ns
Setup Time for STOP Condition	$t_{SU(STOP)}$		0.6			μs
Bus Free Time between START and STOP Condition	t_{BUF}		1.3			μs
Clock Frequency	f_{SCL}		10		400	kHz
Host Communication Failure						
SMBus Bus Release Timeout (1)	$t_{TIMEOUT}$		25		35	ms
Watchdog Timeout Period	t_{WDI}	WDTMR_ADJ[1:0] = 01		5		s
		WDTMR_ADJ[1:0] = 10		88		
		WDTMR_ADJ[1:0] = 11		175		

NOTE:

1. A transfer will be timed out for participating devices when any clock low period exceeds the minimum $t_{TIMEOUT}$ (25ms). The communication must be reset within the maximum $t_{TIMEOUT}$ (35ms) if a timeout condition is detected. Both the master and slave must take action within the maximum $t_{TIMEOUT}$ which has incorporated the master cumulative stretch limit (10ms) and slave cumulative stretch limit (25ms).

TYPICAL APPLICATION CIRCUITS

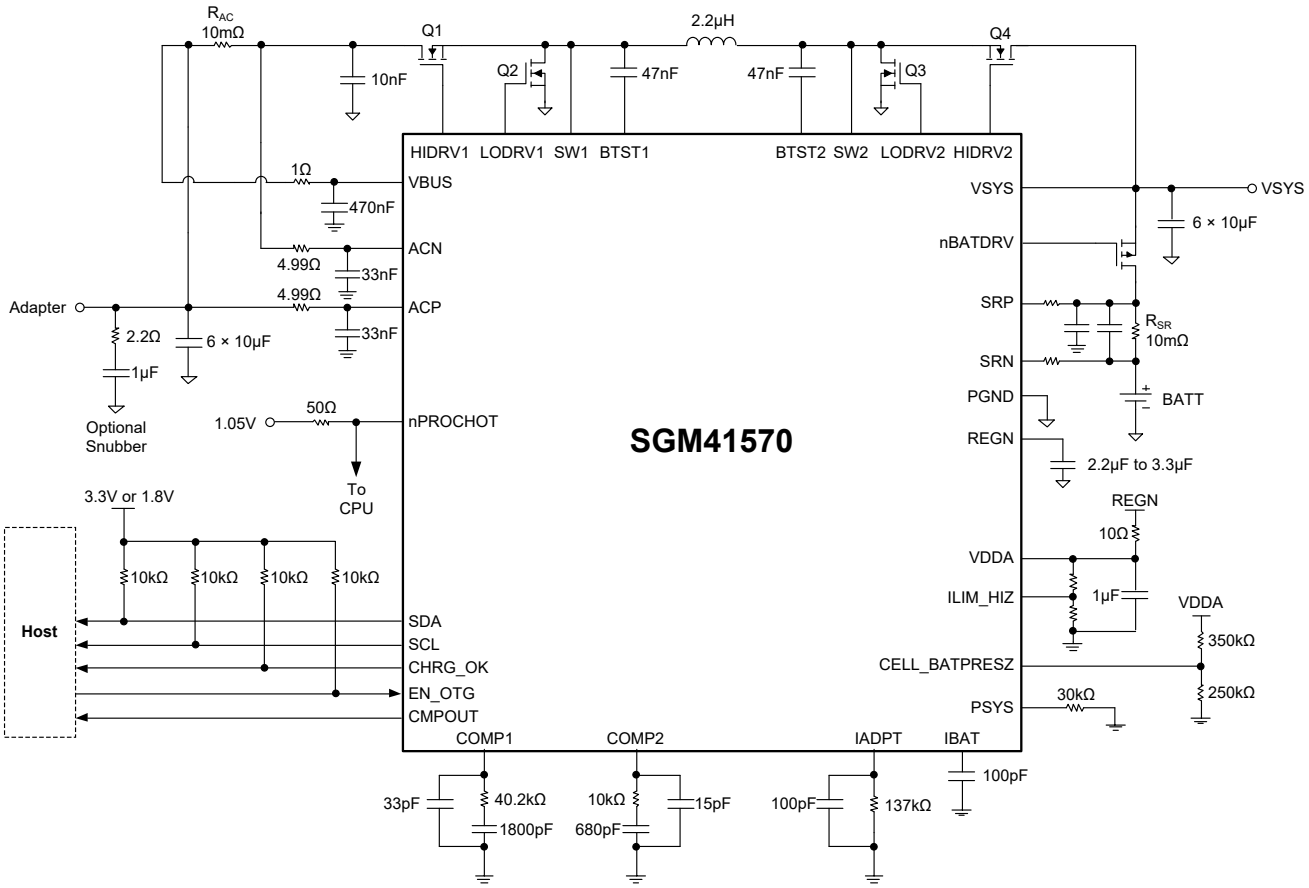


Figure 2. Typical Application Circuit

REGISTER ADDRESS MAPPING

Slave Device Address: 0x09 (0000 1001 + W/R).

Table 1. Command Register Summary

SMBus Address	Register Name	Description	Type	Links
12h	ChargeOption0 Register	Charge Option and Function Enable/Disable	R/W	Go
14h	ChargeCurrent Register	Charge Current Setting	R/W	Go
15h	MaxChargeVoltage Register	Charge Voltage Setting	R/W	Go
30h	ChargeOption1 Register	Charge Option 1	R/W	Go
31h	ChargeOption2 Register	Charge Option 2	R/W	Go
32h	ChargeOption3 Register	Charge Option 3	R/W	Go
33h	ProchotOption0 Register	PROCHOT Option 0	R/W	Go
34h	ProchotOption1 Register	PROCHOT Option 1	R/W	Go
35h	ADCOption Register	ADC Option	R/W	Go
20h	ChargerStatus Register	Charger Status	R	Go
21h	ProchotStatus Register	Prochot Status	R	Go
22h	IIN_DPM Register	Actual Input Current Limit Programmed by IIN_HOST or ICO Algorithm	R	Go
23h	ADCVBUS/PSYS Register	Digital Output of Input Voltage and System Power	R	Go
24h	ADCIBAT Register	Digital Output of Battery Charge/Discharge Current	R	Go
25h	ADCIINCMPIN Register	Digital Output of Input Current and CMPIN Voltage	R	Go
26h	ADCVSYSVBAT Register	Digital Output of System and Battery Voltage	R	Go
3Bh	OTGVoltage Register	OTG Voltage Setting	R/W	Go
3Ch	OTGCurrent Register	OTG Output Current Setting	R/W	Go
3Dh	InputVoltage Register	Input Voltage Setting	R/W	Go
3Eh	MinSystemVoltage Register	Minimum System Voltage Setting	R/W	Go
3Fh	IIN_HOST()	Input Current Limit Set by Host	R/W	Go
FEh	ManufactureID Register	Manufacture ID - 0x07	R	Go
FFh	DeviceID Register	Device ID	R	Go
36h	ChargeOption4 Register	Charge Option 4	R/W	Go

REGISTER AND DATA

R/W: Read/Write bit(s)
R: Read only bit(s)
RC: Bit(s) cleared to 0 by being read
PORV: Power-On Reset Value
n: Parameter code formed by the bits as an unsigned binary number.

Setting Charge and nPROCHOT Options

ChargeOption0 Register (SMBus Address = 12h) [Reset = E70Eh]

Table 2. ChargeOption0 Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	EN_LWPWR	Low Power Mode Enable 0 = Disable low power mode. With battery only, the current/power monitor buffer, nPROCHOT, and comparator follow register setting 1 = Enable low power mode (default). With battery only, the device enters low power mode for lowest quiescent current. The LDO is off, the discharge current monitor buffer, nPROCHOT, power monitor buffer and independent comparator are disabled, and ADC is not available. The independent comparator can be enabled by setting EN_PROCHOT_LPWR bit to 1	1	R/W
D[14:13]	WDTMR_ADJ[1:0]	WATCHDOG Timer Adjust 00 = Disable watchdog timer 01 = 5s 10 = 88s 11 = 175s (default) Set maximum delay between consecutive SMBus write of charge voltage or charge current command. Within the watchdog time period, if device does not receive a write on the MaxChargeVoltage register or the ChargeCurrent register, the charger will be suspended by setting the ChargeCurrent register to 0mA. After expiration, the timer will resume upon the write of ChargeCurrent register, MaxChargeVoltage register or WDTMR_ADJ[1:0]. The charger will resume if the values are valid.	11	R/W
D[12]	IDPM_AUTO_DISABLE	IDPM Auto Disable 0 = Disable the IDPM auto disable function (default). CELL_BATPRESZ going low will not disable IDPM 1 = Enable the IDPM auto disable function. CELL_BATPRESZ going low will disable IDPM If CELL_BATPRESZ pin is low, the IDPM function will be disabled automatically by setting EN_IDPM bit = 0. The IDPM function can be enabled later by writing EN_IDPM bit = 1.	0	R/W
D[11]	OTG_ON_CHRGOK	Add OTG to CHRG_OK 0 = Disable (default) 1 = Enable In OTG mode, drive CHRG_OK to high.	0	R/W
D[10]	EN_OOA	Out-of-Audio Enable 0 = No lower limit for PFM burst frequency 1 = Limit PFM burst frequency to above 25kHz for avoiding audio noise (default)	1	R/W
D[9]	PWM_FREQ	Switching Frequency Selection Bit (Choose based on the inductor value) 0 = 1200kHz 1 = 800kHz (default) 800kHz is recommended for 2.2μH or 3.3μH, and 1.2MHz for 1μH or 1.5μH.	1	R/W
D[8]	LOW_PTM_ RIPPLE	Reduce the Input Voltage and Current Ripple in PTM Mode 0 = Disable 1 = Enable (default)	1	R/W

REGISTER AND DATA (continued)

Table 2. ChargeOption0 Register Details (continued)

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[7]	Reserved	Reserved.	0	R/W
D[6]	SYS_SHORT_DISABLE	Disable the Hiccup during System Short 0 = Enable hiccup 1 = Disabled hiccup	0	R/W
D[5]	EN_LEARN	In LEARN mode, the battery is allowed to discharge while the adapter is present. Over a complete discharge/charge cycle, the battery gauge is calibrated. When the battery voltage is below depletion threshold, the system switches back to adapter input. The device exits LEARN mode and this bit is reset to 0 when CELL_BATPRESZ pin is low. 0 = Disable LEARN mode (default) 1 = Enable LEARN mode	0	R/W
D[4]	IADPT_GAIN	IADPT Amplifier Gain Ratio Selection Bit 0 = 20× (default) 1 = 40× The ratio of IADPT voltage to the sense voltage across ACP and ACN.	0	R/W
D[3]	IBAT_GAIN	IBAT Amplifier Gain Ratio Selection Bit 0 = 8× 1 = 16× (default) The ratio of IBAT voltage to the sense voltage across SRP and SRN.	1	R/W
D[2]	EN_LDO	LDO Mode Enable 0 = Disable LDO mode. BATFET is fully on and charge current follows the ChargeCurrent register setting when battery voltage is below the programmed minimum system voltage setting in MinSystemVoltage register 1 = Enable LDO mode. BATFET is in LDO mode and pre-charge current follows the ChargeCurrent register setting and clamped below 384mA (2-cell to 4-cell) or 2A (1-cell). The system is regulated at the minimum system voltage (default)	1	R/W
D[1]	EN_IDPM	IDPM Enable 0 = Disable IDPM 1 = Enable IDPM (default)	1	R/W
D[0]	CHRG_INHIBIT	Charge Inhibit 0 = Enable charge (default) 1 = Inhibit charge The device starts charging battery depending on the valid charge current and charge voltage programmed in registers if this bit is 0.	0	R/W

REGISTER AND DATA (continued)

ChargeOption1 Register (SMBus Address = 30h) [Reset = 0211h]

Table 3. ChargeOption1 Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	EN_IBAT	IBAT Output Buffer Enable 0 = Disable IBAT buffer to minimize I_Q (default) 1 = Enable IBAT buffer IBAT buffer is disabled even this bit is 1 if EN_LWPWR bit = 1.	0	R/W
D[14]	Reserved	Reserved.	0	R/W
D[13]	EN_PROCHOT_LPWR	Enable nPROCHOT during Battery Only Low Power Mode 0 = Disable low power nPROCHOT (default) 1 = Enable VSYS low power nPROCHOT With battery only, enable VSYS in nPROCHOT with low power consumption. Do not enable this function with adapter present. Refer to nPROCHOT during low power mode for more details.	0	R/W
D[12]	EN_PSYS	PSYS Sense Circuit and Output Buffer Enable 0 = Disable PSYS buffer to minimize I_Q (default) 1 = Enable PSYS buffer PSYS sense circuit and output buffer are disabled even this bit is 1 if EN_LWPWR bit = 1.	0	R/W
D[11]	RSNS_RAC	Input Sense Resistor RAC 0 = 10mΩ (default) 1 = 20mΩ	0	R/W
D[10]	RSNS_RSR	Charge Sense Resistor RSR 0 = 10mΩ (default) 1 = 20mΩ	0	R/W
D[9]	PSYS_RATIO	PSYS Gain Ratio 0 = 0.25μA/W 1 = 1μA/W (default) The ratio of PSYS output current to the total power of input and battery (10mΩ sense resistor).	1	R/W
D[8]	PTM_PINSEL	ILIM_HIZ Pin Function Selection Bit 0 = Enter HIZ mode when pull ILIM_HIZ pin to low (default) 1 = Enter PTM mode when pull ILIM_HIZ pin to low	0	R/W
D[7]	CMP_REF	Internal Reference Voltage of Independent Comparator 0 = 2.3V (default) 1 = 1.2V	0	R/W
D[6]	CMP_POL	Output Polarity of Independent Comparator 0 = Negative. CMPOUT is low when CMPIN is above internal reference threshold (internal hysteresis) (default) 1 = Positive. CMPOUT is low when CMPIN is below internal reference threshold (external hysteresis)	0	R/W
D[5:4]	CMP_DEG[1:0]	Deglitch Time of Independent Comparator 00 = Disable the Independent comparator 01 = Enable independent comparator with 1μs output deglitch time (default) 10 = Enable independent comparator with 2ms output deglitch time 11 = Enable independent comparator with 5s output deglitch time Only applied to the CMPOUT falling edge (HIGH → LOW).	01	R/W
D[3]	FORCE_LATCHOFF	Force Power Path Off 0 = Disable this function (default) 1 = Enable this function When independent comparator is enabled and triggered, Q1 and Q4 are turned off, system is disconnected from the input source, and CHRG_OK signal goes to low. The user must unplug the adapter to clear the LATCHOFF condition to enable the converter again.	0	R/W
D[2]	EN_PTM	PTM Enable 0 = Disable PTM (default) 1 = Enable PTM	0	R/W
D[1]	EN_SHIP_DCHG	Discharge Battery for Shipping Mode 0 = Disable shipping mode (default) 1 = Enable shipping mode When set to 1, discharge battery down below 3.8V in 140ms. When 140ms is over, this bit is reset to 0.	0	R/W
D[0]	AUTO_WAKEUP_EN	Auto Wakeup Enable 0 = Disable 1 = Enable (default) When set to 1, if battery voltage is below the minimum system voltage programmed in MinSystemVoltage register, wake up charge with 128mA charge current for 30mins is automatically enabled. When the battery voltage is charged above the minimum system voltage, the wake up charge will terminate and the bit is reset to 0.	1	R/W

REGISTER AND DATA (continued)

ChargeOption2 Register (SMBus Address = 31h) [Reset = 02B7h]

Table 4. ChargeOption2 Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:14]	PKPWR_TOVLD_DEG[1:0]	Input Overload Time in Peak Power Mode 00 = 1ms (default) 01 = 2ms 10 = 10ms 11 = 20ms	00	R/W
D[13]	EN_PKPWR_IDPM	Enable Input Current Overshoot to Trigger Peak Power Mode 0 = Disable input current overshoot to trigger peak power mode (default) 1 = Enable input current overshoot to trigger peak power mode If EN_PKPWR_IDPM and EN_PKPWR_VSYS are both 0, peak power mode is disabled. These bits are both reset to 0 when adapter removal.	0	R/W
D[12]	EN_PKPWR_VSYS	Enable System Voltage Under-Shoot to Trigger Peak Power Mode 0 = Disable system voltage under-shoot to trigger peak power mode (default) 1 = Enable system voltage under-shoot to trigger peak power mode If EN_PKPWR_IDPM and EN_PKPWR_VSYS are both 0, peak power mode is disabled. These bits are both reset to 0 when adapter removal.	0	R/W
D[11]	PKPWR_OVLD_STAT	Status Bit Indicates that it is in overload cycle. Write 0 to get out of overload cycle. 0 = Not in overload cycle (default) 1 = In overload cycle	0	R/W
D[10]	PKPWR_RELAX_STAT	Status Bit Indicates that it is in relax cycle. Write 0 to get out of relax cycle. 0 = Not in relax cycle (default) 1 = In relax cycle	0	R/W
D[9:8]	PKPWR_TMAX[1:0]	Peak Power Mode Overload and Relax Cycle Time 00 = 5ms 01 = 10ms 10 = 20ms (default) 11 = 40ms When PKPWR_TOVLD_DEG[1:0] is programmed longer than PKPWR_TMAX[1:0], there is no relax time.	10	R/W
D[7]	EN_EXTILIM	Enable ILIM_HIZ Pin to Set External Input Current Limit 0 = Disable ILIM_HIZ pin to set external input current limit 1 = Enable ILIM_HIZ pin to set external input current limit. The actual input current limit is set by the lower value of external input current limit, IIN_DPM and IIN_HOST register (default)	1	R/W
D[6]	EN_ICHG_IDCHG	0 = IBAT pin output represents discharge current (default) 1 = IBAT pin output represents charge current	0	R/W
D[5]	Q2_OCP	Q2 OCP Threshold Sensed by Q2 V_{DS} Voltage 0 = 210mV 1 = 150mV (default)	1	R/W
D[4]	ACX_OCP	Input Current OCP Threshold Sensed by the Voltage across ACP and ACN 0 = 280mV 1 = 150mV (default)	1	R/W
D[3]	EN_ACOC	ACOC Enable 0 = Disable ACOC (default) 1 = Enable ACOC If ACOC is detected, the converter is disabled after 100μs blank-out time.	0	R/W
D[2]	ACOC_VTH	ACOC Limit (As Percentage of ILIM2) 0 = 133% 1 = 200% (default)	1	R/W
D[1]	EN_BATOC	Battery Discharge Over-Current (BATOC) Enable 0 = Disable BATOC 1 = Enable BATOC (default) If BATOC is detected, converter is disabled.	1	R/W
D[0]	BATOC_VTH	Battery Discharge Over-Current threshold Sensed by the Voltage across SRN and SRP (As Percentage of IDCHG_VTH[5:0]) 0 = 133% 1 = 200% (default)	1	R/W

REGISTER AND DATA (continued)

ChargeOption3 Register (SMBus Address = 32h) [Reset = 0030h]

Table 5. ChargeOption3 Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	EN_HIZ	HIZ Mode Enable 0 = Not in HIZ mode (default) 1 = In HIZ mode In HIZ mode, the device draws minimal quiescent current, REGN LDO remains on, and system is powered from battery.	0	R/W
D[14]	RESET_REG	Reset Registers All the registers are reset to default except VINDPM register. 0 = Idle (default) 1 = Reset the registers to default. This bit is reset to 0 after reset Using this bit to reset the registers to default is not recommended when the battery voltage is below minimal system voltage or in battery removal.	0	R/W
D[13]	RESET_VINDPM	Reset VINDPM Threshold 0 = Idle (default) 1 = Temporary disable the converter to measure VINDPM threshold. After the measurement is done, this bit is reset to 0 and converter restarts	0	R/W
D[12]	EN_OTG	OTG Enable 0 = Disable OTG (default) 1 = Enable OTG	0	R/W
D[11]	EN_ICO_MODE	Enable ICO 0 = Disable ICO (default) 1 = Enable ICO	0	R/W
D[10:7]	Reserved	Reserved.	0000	R/W
D[6]	EN_CON_VAP	Enable the Conservative VAP Mode 0 = Disabled. When $V_{SYS} < V_{SYS\_TH2}$, generate an nPROCHOT pulse if PROCHOT_PROFILE_VSYS bit = 1 (default) 1 = Enabled. When $V_{BUS} < V_{VBUS\_CONVENZ}$, generate an nPROCHOT pulse if PROCHOT_PROFILE_VSYS bit = 1	0	R/W
D[5]	OTG_VAP_MODE	OTG/VAP Pin Control Selection 0 = The OTG/VAP pin controls the Enable/Disable of VAP 1 = The OTG/VAP pin controls the Enable/Disable of OTG (default)	1	R/W
D[4:3]	IL_AVG[1:0]	Inductor Average Current Clamp Selection 00 = 6A 01 = 10A 10 = 15A (default) 11 = Disabled	10	R/W
D[2]	OTG_RANGE_LOW	OTG Output Voltage Range Selection 0 = High range 4.28V - 20.8V (default) 1 = Low range 3V - 19.52V	0	R/W
D[1]	BATFETOFF_HIZ	BATFET On/Off during HIZ Mode 0 = On (default) 1 = Off	0	R/W
D[0]	PSYS_OTG_IDCHG	PSYS Function during OTG Mode 0 = PSYS reports the battery discharge power minus OTG output power (default) 1 = PSYS reports the battery discharge power only	0	R/W

REGISTER AND DATA (continued)

ProchotOption0 Register (SMBus Address = 33h) [Reset = 4A65h]

Table 6. ProchotOption0 Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:11]	ILIM2_VTH[4:0]	I_{LIM2} Threshold Sensed by the Voltage between ACP and CAN (As Percentage of the Value Setting in IIN_HOST Register) 00001 - 11001 = 110% - 230%, step 5% 11010 - 11110 = 250% - 450%, step 50% 11111 = Out of range (ignored) Default: 150%, or 01001	0 1001	R/W
D[10:9]	ICRIT_DEG[1:0]	ICRIT Deglitch Time to Trigger nPROCHOT ICRIT is 110% of I_{LIM2}. 00 = 15μs 01 = 100μs (default) 10 = 400μs (max 500μs) 11 = 800μs (max 1ms)	01	R/W
D[8]	PROCHOT_ VDPM_80_90	Lower Threshold of the PROCHOT_VDPM Comparator (As Percentage of VINDPM Threshold) 0 = 80% (default) 1 = 90% The threshold of the PROCHOT_VDPM comparator is determined by this bit if LOWER_PROCHOT_VDPM bit = 1.	0	R/W
D[7:4]	VSYS_TH1[3:0]	VSYS Threshold in to Discharge VBUS in VAP Mode In VAP mode, when the VSYS pin voltage is below this threshold with fixed 5μs deglitch time, VBUS starts to discharge. For 2-cell to 4-cell batteries: 0000 - 1111 = 5.9V - 7.4V with 0.1V step Default: 0b0110, V_{SYS_TH1} = 6.5V For 1-cell battery: 0000 - 0111 = 3.1V - 3.8V with 0.1V step 1000 - 1111 = 3.1V - 3.8V with 0.1V step Default: 0b0110, V_{SYS_TH1} = 3.7V	0110	R/W
D[3:2]	VSYS_TH2[1:0]	VSYS Threshold to Assert PROCHOT_VSYS When the VSYS pin voltage is below this threshold with fixed 5μs deglitch time, assert the PROCHOT_VSYS. For 2-cell to 4-cell batteries: 00 = 5.9V 01 = 6.2V (default) 10 = 6.5V 11 = 6.8V For 1-cell battery: 00 = 3.1V 01 = 3.3V (default) 10 = 3.5V 11 = 3.7V	01	R/W
D[1]	INOM_DEG	INOM Deglitch Time 0 = 1ms (must be max) (default) 1 = 50ms (max 65ms) INOM is 110% of the input current limit setting in IIN_HOST register. When the current sensed by voltage across ACP and ACN is above INOM with this deglitch time, INOM is triggered.	0	R/W
D[0]	LOWER_PROCHOT _VDPM	Lower Threshold of the PROCHOT_VDPM Comparator Enable 0 = Disable. The PROCHOT_VDPM comparator threshold follows the InputVoltage register setting 1 = Enable. The PROCHOT_VDPM comparator threshold is lower and determined by PROCHOT_ VDPM_80_90 bit setting (default)	1	R/W

REGISTER AND DATA (continued)

ProchotOption1 Register (SMBus Address = 34h) [Reset = 81A0h]

Table 7. ProchotOption1 Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:10]	IDCHG_VTH[5:0]	IDCHG Threshold IDCHG is measured by the sensed voltage between SRN and SRP. IDCHG is triggered when the discharge current is above this threshold. Range from 0A to 32256mA with 512mA step, If the value is programmed to 000000b, IDCHG threshold is 128mA. Default: 100000b for16384mA	10 0000	R/W
D[9:8]	IDCHG_DEG[1:0]	IDCHG Deglitch Time 00 = 1.6ms 01 = 100μs (default) 10 = 6ms 11 = 12ms	01	R/W
D[7]	PROCHOT _PROFILE_VDPM	Enable PROCHOT_PROFILE_VDPM 0 = Disable 1 = Enable (default) When all bits in the ProchotOption1 register are 0, nPROCHOT function is disabled. This bit detects the VBUS voltage.	1	R/W
D[6]	PROCHOT _PROFILE_COMP	Enable PROCHOT_PROFILE_COMP 0 = Disable (default) 1 = Enable	0	R/W
D[5]	PROCHOT _PROFILE_ICRIT	Enable PROCHOT_PROFILE_ICRIT 0 = Disable 1 = Enable (default)	1	R/W
D[4]	PROCHOT _PROFILE_INOM	Enable PROCHOT_PROFILE_INOM 0 = Disable (default) 1 = Enable	0	R/W
D[3]	PROCHOT _PROFILE_IDCHG	Enable PROCHOT_PROFILE_IDCHG 0 = Disable (default) 1 = Enable	0	R/W
D[2]	PROCHOT _PROFILE_VSYS	Enable PROCHOT_PROFILE_VSYS 0 = Disable (default) 1 = Enable When device enters the VAP mode, PROCHOT_PROFILE_VSYS bit will be automatically set to 1.	0	R/W
D[1]	PROCHOT _PROFILE_BATPRES	Enable PROCHOT__PROFILE_BATPRES 0 = Disable (default) 1 = Enable (one-shot falling edge triggered) If PROCHOT_PROFILE_BATPRES is enabled in nPROCHOT after the battery removal, one-shot nPROCHOT pulse will be send immediately.	0	R/W
D[0]	PROCHOT _PROFILE_ACOK	Enable PROCHOT_PROFILE_ACOK 0 = Disable (default) 1 = Enable If PROCHOT_PROFILE_ACOK is enabled in nPROCHOT, it will assert nPROCHOT pulse after adapter removal.	0	R/W

REGISTER AND DATA (continued)

ADCOption Register (SMBus Address = 35h) [Reset = 2000h]

The ADC registers reading order: VBAT, VSYS, ICHG, IDCHG, IIN, PSYS, VBUS, CMPIN. In low power mode, ADC is disabled.

Table 8. ADCOption Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	ADC_CONV	ADC conversion update Mode Selection 0 = One-shot update. Update the registers of ADCVBUS/PSYS, ADCIBAT, ADCIINCMPIN and ADCVSYSVBAT once after ADC_START = 1 (default) 1 = Continuous update. Update the registers of ADCVBUS/PSYS, ADCIBAT, ADCIINCMPIN and ADCVSYSVBAT every 1 sec The typical time of ADC conversion is 10ms.	0	R/W
D[14]	ADC_START	0 = No ADC conversion (default) 1 = Start ADC conversion This bit automatically resets to 0 when the one-shot update is completed.	0	R/W
D[13]	ADC_FULLSCALE	ADC Input Voltage Range 0 = 2.04V (recommended when input voltage is below 5V or 1-cell battery) 1 = 3.06V (default)	1	R/W
D[12:8]	Reserved	Reserved.	0 0000	R/W
D[7]	EN_ADC_CMPIN	0 = Disable (default) 1 = Enable	0	R/W
D[6]	EN_ADC_VBUS	0 = Disable (default) 1 = Enable	0	R/W
D[5]	EN_ADC_PSYS	0 = Disable (default) 1 = Enable	0	R/W
D[4]	EN_ADC_IIN	0 = Disable (default) 1 = Enable	0	R/W
D[3]	EN_ADC_IDCHG	0 = Disable (default) 1 = Enable	0	R/W
D[2]	EN_ADC_ICHG	0 = Disable (default) 1 = Enable	0	R/W
D[1]	EN_ADC_VSYS	0 = Disable (default) 1 = Enable	0	R/W
D[0]	EN_ADC_VBAT	0 = Disable (default) 1 = Enable	0	R/W

REGISTER AND DATA (continued)

Charge and nPROCHOT Status

ChargerStatus Register (SMBus Address = 20h) [Reset = 0000h]

Table 9. ChargerStatus Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	AC_STAT	0 = Input not present (default) 1 = Input is present	0	R
D[14]	ICO_DONE	The bit is set to 1 when the ICO routine is successfully executed. 0 = ICO is not complete (default) 1 = ICO is complete	0	R
D[13]	IN_VAP	0 = Not in VAP mode (default) 1 = In VAP mode	0	R
D[12]	IN_VINDPM	0 = Not in VINDPM during forward mode, or not in voltage regulation during OTG mode (default) 1 = In VINDPM during forward mode, or in voltage regulation during OTG mode	0	R
D[11]	IN_IINDPM	0 = Not in IINDPM (default) 1 = In IINDPM	0	R
D[10]	IN_FCHRG	0 = Not in fast charge (default) 1 = In fast charger	0	R
D[9]	IN_PCHRG	0 = Not in pre-charge (default) 1 = In pre-charge	0	R
D[8]	IN_OTG	0 = Not in OTG (default) 1 = In OTG	0	R
D[7]	Fault ACOV	0 = No fault (default) 1 = ACOV fault has occurred. After the ACOV fault disappears, host reads this bit to reset it to 0	0	RC
D[6]	Fault BATOC	0 = No fault (default) 1 = BATOC fault has occurred. After the BATOC fault disappears, host reads this bit to reset it to 0	0	RC
D[5]	Fault ACOC	0 = No fault (default) 1 = ACOC fault has occurred. After the ACOC fault disappears, host reads this bit to reset it to 0	0	RC
D[4]	SYSOVP_STAT	SYSOVP Status and Clear Bit 0 = Not in SYSOVP (default) 1 = SYSOVP has occurred. After the SYSOVP condition is removed, host writes this bit to 0 or unplug the adapter to clear the SYSOVP latch	0	R/W
D[3]	Fault SYS_SHORT	0 = No fault (default) 1 = SYS_SHORT fault has occurred. After the SYS_SHORT fault disappears, host writes this bit to 0 to clear the SYS_SHORT latch	0	R/W
D[2]	Fault Latchoff	0 = No fault (default) 1 = Latch off (FORCE_LATCHOFF bit) fault has occurred	0	R
D[1]	Fault_OTG_OVP	0 = No fault (default) 1 = OTG OVP fault has occurred. After the OTG OVP fault disappears, host reads this bit to reset it to 0	0	RC
D[0]	Fault_OTG_UVP	0 = No fault (default) 1 = OTG UVP fault has occurred. After the OTG UVP fault disappears, host reads this bit to reset it to 0	0	RC

REGISTER AND DATA (continued)

ProchotStatus Register (SMBus Address = 21h) [Reset = A800h]

Table 10. ProchotStatus Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	Reserved	Reserved.	1	R
D[14]	EN_PROCHOT_EXIT	nPROCHOT Pulse Extension Enable 0 = Disable (default) 1 = Enable When it is enabled, the nPROCHOT pin voltage keeps low until PROCHOT_CLEAR bit = 0 is written.	0	R/W
D[13:12]	PROCHOT_WIDTH[1:0]	Minimum nPROCHOT Pulse Width when EN_PROCHOT_EXIT Bit = 0 00 = 100μs 01 = 1ms 10 = 10ms (default) 11 = 5s	10	R/W
D[11]	PROCHOT_CLEAR	nPROCHOT Pulse Clear when EN_PROCHOT_EXIT Bit = 1. 0 = Clear nPROCHOT pulse and drive nPROCHOT pin high 1 = Idle (default)	1	R/W
D[10]	TSHUT	TDIE Thermal Shutdown Fault Status Bit 0 = No TDIE thermal shutdown fault (default) 1 = Device in TDIE thermal shutdown fault status	0	R
D[9]	STAT_VAP_FAIL	Status bit reports that it fails to load VBUS 7 consecutive times in VAP mode, which indicates the battery voltage might be too low to enter VAP mode, or the VAP loading current settings is too high. 0 = Not in VAP failure (default) 1 = In VAP failure, the charger exits VAP mode, and latches off until host writes this bit to 0	0	R/W
D[8]	STAT_EXIT_VAP	In VAP mode, the charger can exit VAP mode by either being disabled through host, or any charger faults occurs. 0 = STAT_EXIT_VAP is not active (default) 1 = STAT_EXIT_VAP is active. nPROCHOT pin keeps low until host writes 0 to this bit	0	R/W
D[7]	STAT_VDPM	0 = Not triggered (default) 1 = Triggered. Assert nPROCHOT pin low when PROCHOT_PROFILE_VDPM bit = 1. Host writes 0 to this bit to reset it to 0	0	R/W
D[6]	STAT_COMP	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_COMP bit = 1. After CMPOUT pin goes high, host reads this bit to reset it to 0	0	RC
D[5]	STAT_ICRIT	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_ICRIT bit = 1. After adapter peak current falls below 110% of I_{LIM2}, host reads this bit to reset it to 0	0	RC
D[4]	STAT_INOM	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_INOM bit = 1. After adapter average current falls below 110% of IINDPM, host reads this bit to reset it to 0	0	RC
D[3]	STAT_IDCHG	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_IDCHG bit = 1. After battery discharge current falls below IDCHG_VTH, host reads this bit to reset it to 0	0	RC
D[2]	STAT_VSYS	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_VSYS bit = 1. After V_{SYS} rises above V_{SYS_TH2} when EN_CON_VAP bit = 0, or V_{BUS} rises above V_{VBUS_CONVEN} when EN_CON_VAP bit = 1, host reads this bit to reset it to 0	0	RC
D[1]	STAT_Battery_Removal	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_BATPRES bit = 1. Host reads this bit to reset it to 0	0	RC
D[0]	STAT_Adapter_Removal	0 = Not triggered (default) 1 = Triggered. Generate an nPROCHOT pulse when PROCHOT_PROFILE_ACOK bit = 1. After $V_{BUS} > V_{VBUS\_CONVEN}$ and CHRG_OK pin goes high, host reads this bit to reset it to 0	0	RC

REGISTER AND DATA (continued)

ChargeCurrent Register

Charge current is set in ChargeCurrent register. When a 10mΩ sense resistor is used, the charge current range is 64mA to 8.128A with 64mA resolution.

The ChargeCurrent register will be set to 0A when auto wakeup is not active after POR, as well as the CELL_BATPRESZ going low. Writing MaxChargeVoltage register to 0 will also force the ChargeCurrent to 0A to disable charge.

The default current sense resistor R_{SR} between SRP and SRN is 10mΩ, other value resistor can also be used. Larger sense resistor will increase the regulation accuracy but increase the conduction loss at the same time, thus values above 20mΩ are not recommended.

ChargeCurrent Register with 10mΩ Sense Resistor (SMBus Address = 14h) [Reset = 0000h]

Table 11. ChargeCurrent Register with 10mΩ Sense Resistor Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:13]	Reserved	Reserved.	000	R/W
D[12]	Charge Current, Bit 6	0 = Adds 0mA of charger current (default) 1 = Adds 4096mA of charger current	0	R/W
D[11]	Charge Current, Bit 5	0 = Adds 0mA of charger current (default) 1 = Adds 2048mA of charger current	0	R/W
D[10]	Charge Current, Bit 4	0 = Adds 0mA of charger current (default) 1 = Adds 1024mA of charger current	0	R/W
D[9]	Charge Current, Bit 3	0 = Adds 0mA of charger current (default) 1 = Adds 512mA of charger current	0	R/W
D[8]	Charge Current, Bit 2	0 = Adds 0mA of charger current (default) 1 = Adds 256mA of charger current	0	R/W
D[7]	Charge Current, Bit 1	0 = Adds 0mA of charger current (default) 1 = Adds 128mA of charger current	0	R/W
D[6]	Charge Current, Bit 0	0 = Adds 0mA of charger current (default) 1 = Adds 64mA of charger current	0	R/W
D[5:0]	Reserved	Reserved.	00 0000	R/W

Battery Pre-Charge Current Clamp

In pre-charge, BATFET operates in linear (LDO) mode when EN_LDO bit = 1. For 2-cell/3-cell/4-cell battery, VSYS voltage is regulated at minimum system voltage and pre-charge current is clamped at 384mA. For 1-cell battery, the pre-charge current is clamped at 384mA. When VBAT is above 3V but below minimum system voltage, the BATFET operates in LDO mode and the charge current is clamped at 2A.

REGISTER AND DATA (continued)

MaxChargeVoltage Register (SMBus Address = 15h) [Reset Value Based on CELL_BATPRESZ Pin Setting]

Charge voltage is set in MaxChargeVoltage register. The charge voltage range is 1.024V to 19.200V with 8mV resolution.

The MaxChargeVoltage register is set to 4200mV for 1-cell, 8400mV for 2-cell, 12600mV for 3-cell or 16800mV for 4-cell by default. After CHRG_OK goes high, the charge will start depending on the charge current setting in ChargeCurrent register and the charge voltage setting in MaxChargeVoltage register. MaxChargeVoltage register needs to be set before ChargeCurrent register for correct battery voltage setting if battery voltage different from 4.2V/cell is wanted. Writing MaxChargeVoltage register to 0 will set MaxChargeVoltage register to the default value based on CELL_BATPRESZ pin.

The battery voltage is sensed on SRN pin for regulation, and the battery should be placed as close to SRN pin as possible.

Table 12. MaxChargeVoltage Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	Reserved	Reserved.	0	R/W
D[14]	Max Charge Voltage, Bit 11	0 = Adds 0mV of charger voltage (default) 1 = Adds 16384mV of charger voltage	0	R/W
D[13]	Max Charge Voltage, Bit 10	0 = Adds 0mV of charger voltage (default) 1 = Adds 8192mV of charger voltage	0	R/W
D[12]	Max Charge Voltage, Bit 9	0 = Adds 0mV of charger voltage (default) 1 = Adds 4096mV of charger voltage	0	R/W
D[11]	Max Charge Voltage, Bit 8	0 = Adds 0mV of charger voltage (default) 1 = Adds 2048mV of charger voltage	0	R/W
D[10]	Max Charge Voltage, Bit 7	0 = Adds 0mV of charger voltage (default) 1 = Adds 1024mV of charger voltage	0	R/W
D[9]	Max Charge Voltage, Bit 6	0 = Adds 0mV of charger voltage (default) 1 = Adds 512mV of charger voltage	0	R/W
D[8]	Max Charge Voltage, Bit 5	0 = Adds 0mV of charger voltage (default) 1 = Adds 256mV of charger voltage	0	R/W
D[7]	Max Charge Voltage, Bit 4	0 = Adds 0mV of charger voltage (default) 1 = Adds 128mV of charger voltage	0	R/W
D[6]	Max Charge Voltage, Bit 3	0 = Adds 0mV of charger voltage (default) 1 = Adds 64mV of charger voltage	0	R/W
D[5]	Max Charge Voltage, Bit 2	0 = Adds 0mV of charger voltage (default) 1 = Adds 32mV of charger voltage	0	R/W
D[4]	Max Charge Voltage, Bit 1	0 = Adds 0mV of charger voltage (default) 1 = Adds 16mV of charger voltage	0	R/W
D[3]	Max Charge Voltage, Bit 0	0 = Adds 0mV of charger voltage (default) 1 = Adds 8mV of charger voltage	0	R/W
D[2:0]	Reserved	Reserved.	000	R/W

REGISTER AND DATA (continued)

MinSystemVoltage Register

The minimum system voltage is set in MinSystemVoltage register. The minimum system voltage range is 1.024V to 16.128V with 256mV resolution. Any out-of-range write is ignored. The MinSystemVoltage register is set to 3.584V for 1-cell, 6.144V for 2-cell, 9.216V for 3-cell, and 12.288V for 4-cell by default. Writing MinSystemVoltage register to 0 will set MinSystemVoltage register to the default value based on CELL_BATPRESZ pin.

MinSystemVoltage Register (SMBus Address = 3Eh) [Reset Value Based on CELL_BATPRESZ Pin Setting]

Table 13. MinSystemVoltage Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:14]	Reserved	Reserved.	00	R/W
D[13]	Minimum System Voltage, Bit 5	n = D[5:0] Minimum System Voltage Value = 256n (mV) (n ≥ 4) Range: 1024mV (000100) - 16128Mv (1111111)	0	R/W
D[12]	Minimum System Voltage, Bit 4		0	R/W
D[11]	Minimum System Voltage, Bit 3		1	R/W
D[10]	Minimum System Voltage, Bit 2		1	R/W
D[9]	Minimum System Voltage, Bit 1		1	R/W
D[8]	Minimum System Voltage, Bit 0		0	R/W
D[7:0]	Reserved	Reserved	0000 0000	R/W

System Voltage Regulation

The system is separated from battery by BATFET, and the system is regulated above the minimum system voltage setting in MinSystemVoltage register even if the battery is completely depleted or removed.

The BATFET is in LDO mode and the system is regulated above V_{SYSMIN} when the battery voltage is below V_{SYSMIN}.

The BATFET is fully on (during charge or in supplement mode) and the system voltage is regulated at battery voltage plus the VDS of BATFET when the battery voltage is above V_{SYSMIN}.

The BATFET is off and the system voltage is regulated at battery voltage plus about 200mV when the device is in charging or no supplement mode.

VSYS is shorted to SRP if BATFET is removed. At this condition, LDO mode must be disabled before starting converter, follow the sequence below to configure charger.

1. Before the adapter is plugged in, set the charger into HIZ mode by pulling ILIM_HIZ pin to ground or setting EN_HIZ bit to 1.
2. Disable LDO mode by setting EN_LDO bit to 0.
3. Disable auto-wakeup mode by setting AUTO_WAKEUP_EN bit to 0.
4. Make sure the battery voltage is set properly in MaxChargeVoltage register.
5. Set pre-charge/charge current in ChargeCurrent register.
6. Exit HIZ mode by releasing ILIM_HIZ from ground and set EN_HIZ bit to 0.

When exiting HIZ mode, low input current limit (a few hundred milliamps) should be set to avoid accidental SW mistakes.

REGISTER AND DATA (continued)

Input Current and Input Voltage Registers for Dynamic Power Management

The SGM41570 features Dynamic Power Management (DPM). When the input current tries to exceed the input current limits or the input voltage tends to fall below the input voltage limit, the device gives priority to provide system load by reducing the battery charge current adequately to avoid the input parameter (voltage or current) exceeding the limit.

If the charge current is decreased and reached to zero, but the input is still overloaded, the system voltage starts to drop with the system load rising. When the system voltage drops below the battery voltage, the device operates in supplement mode and the battery provides a portion of system power demand through BATFET.

Input Current Limit Registers

The input current limit is set in IIN_HOST register. With a 10mΩ sense resistor, the input current limit range is 50mA to 6400mA with 50mA resolution. The default input current limit is 3.25A. The input current limit is reset to default value when adapter removal, and the input current limit is 50mA when the IIN_HOST register code is set to 0.

The default current sense resistor R_{AC} between ACP and ACN is 10mΩ, other value resistor such as 20mΩ can also be used. Larger sense resistor will increase the regulation accuracy, but will increase the conduction loss at the same time.

External input current limit can be set by ILIM_HIZ pin voltage using the following equation, in which I_{DPM} is the target input current limit.

$$V_{ILIM\_HIZ} = 1V + 40 \times (V_{ACP} - V_{ACN}) = 1+ 40 \times I_{DPM} \times R_{AC} \quad (2)$$

Writing EN_EXTILIM bit to 0 or pulling ILIM_HIZ pin above 4.0V can disable ILIM_HIZ pin.

IIN_HOST Register with 10mΩ Sense Resistor (SMBus Address = 3Fh) [Reset = 4100h]

Table 14. IIN_HOST Register with 10mΩ Sense Resistor Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	Reserved	Reserved.	0	R/W
D[14]	Input Current set by Host, Bit 6	n = D[6:0] IIN_HOST Value = 50n (mA) (n ≠ 0) Range: 50mA (0000001) - 6350Ma (1111111)	1	R/W
D[13]	Input Current set by Host, Bit 5		0	R/W
D[12]	Input Current set by Host, Bit 4		0	R/W
D[11]	Input Current set by Host, Bit 3		0	R/W
D[10]	Input Current set by Host, Bit 2		0	R/W
D[9]	Input Current set by Host, Bit 1		0	R/W
D[8]	Input Current set by Host, Bit 0		1	R/W
D[7:0]	Reserved	Reserved.	0000 0000	R

NOTE: The low clamp value is 0b0000001.

REGISTER AND DATA (continued)

IIN_DPM Register with 10mΩ Sense Resistor (SMBus Address = 22h) [Reset = 4100h]

IIN_DPM register reports the actual input current limit programmed by IIN_HOST or ICO algorithm. ICO algorithm may change the input current limit and the value in IIN_DPM register. The input current limit read-back value is 50mA when IIN_DPM register code is 0.

Table 15. IIN_DPM Register with 10mΩ Sense Resistor Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	Reserved	Reserved.	0	R
D[14]	Input Current in DPM, Bit 6	n = D[6:0] Input Current Limit Read-Back Value = 50 (mA) (n = 0) Input Current Limit Read-Back Value = 50n (mA) (n ≠ 0) Range: 50mA (0000000) - 6350mA (1111111)	1	R
D[13]	Input Current in DPM, Bit 5		0	R
D[12]	Input Current in DPM, Bit 4		0	R
D[11]	Input Current in DPM, Bit 3		0	R
D[10]	Input Current in DPM, Bit 2		0	R
D[9]	Input Current in DPM, Bit 1		0	R
D[8]	Input Current in DPM, Bit 0		1	R
D[7:0]	Reserved	Reserved.	0000 0000	R

InputVoltage Register (SMBus Address = 3Dh) [Reset = VBUS - 1.28V]

The input voltage limit is set in InputVoltage register. When the input voltage drops below the value programmed in InputVoltage register, the charger enters VINDPM. The default value of input voltage limit is 1.28V below the no-load VBUS voltage, and the value is 3.2V when setting InputVoltage register code to 0.

Table 16. InputVoltage Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:14]	Reserved	Reserved.	00	R/W
D[13]	Input Voltage, Bit 7	0 = Adds 0mV of input voltage (default) 1 = Adds 8192mV of input voltage	0	R/W
D[12]	Input Voltage, Bit 6	0 = Adds 0mV of input voltage (default) 1 = Adds 4096mV of input voltage	0	R/W
D[11]	Input Voltage, Bit 5	0 = Adds 0mV of input voltage (default) 1 = Adds 2048mV of input voltage	0	R/W
D[10]	Input Voltage, Bit 4	0 = Adds 0mV of input voltage (default) 1 = Adds 1024mV of input voltage	0	R/W
D[9]	Input Voltage, Bit 3	0 = Adds 0mV of input voltage (default) 1 = Adds 512mV of input voltage	0	R/W
D[8]	Input Voltage, Bit 2	0 = Adds 0mV of input voltage (default) 1 = Adds 256mV of input voltage	0	R/W
D[7]	Input Voltage, Bit 1	0 = Adds 0mV of input voltage (default) 1 = Adds 128mV of input voltage	0	R/W
D[6]	Input Voltage, Bit 0	0 = Adds 0mV of input voltage (default) 1 = Adds 64mV of input voltage	0	R/W
D[5:0]	Reserved	Reserved.	00 0000	R/W

REGISTER AND DATA (continued)

OTGVoltage Register (SMBus Address = 3Bh) [Reset = 0000h]

The OTG output voltage limit is set in OTGVoltage register. The range of OTG output voltage limit is 3V to 20.56V. Although it is possible to successfully write the registers with a value below the minimum or above the maximum, the actual OTG output voltage is limited. The DAC offset is 1.28V when OTG_RANGE_LOW bit = 0, and there is no offset when OTG_RANGE_LOW bit = 1.

Table 17. OTGVoltage Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:14]	Reserved	Reserved.	00	R/W
D[13]	OTG Voltage, Bit 11	0 = Adds 0mV of OTG voltage (default) 1 = Adds 16384mV of OTG voltage	0	R/W
D[12]	OTG Voltage, Bit 10	0 = Adds 0mV of OTG voltage (default) 1 = Adds 8192mV of OTG voltage	0	R/W
D[11]	OTG Voltage, Bit 9	0 = Adds 0mV of OTG voltage (default) 1 = Adds 4096mV of OTG voltage	0	R/W
D[10]	OTG Voltage, Bit 8	0 = Adds 0mV of OTG voltage (default) 1 = Adds 2048mV of OTG voltage	0	R/W
D[9]	OTG Voltage, Bit 7	0 = Adds 0mV of OTG voltage (default) 1 = Adds 1024mV of OTG voltage	0	R/W
D[8]	OTG Voltage, Bit 6	0 = Adds 0mV of OTG voltage (default) 1 = Adds 512mV of OTG voltage	0	R/W
D[7]	OTG Voltage, Bit 5	0 = Adds 0mV of OTG voltage (default) 1 = Adds 256mV of OTG voltage	0	R/W
D[6]	OTG Voltage, Bit 4	0 = Adds 0mV of OTG voltage (default) 1 = Adds 128mV of OTG voltage	0	R/W
D[5]	OTG Voltage, Bit 3	0 = Adds 0mV of OTG voltage (default) 1 = Adds 64mV of OTG voltage	0	R/W
D[4]	OTG Voltage, Bit 2	0 = Adds 0mV of OTG voltage (default) 1 = Adds 32mV of OTG voltage	0	R/W
D[3]	OTG Voltage, Bit 1	0 = Adds 0mV of OTG voltage (default) 1 = Adds 16mV of OTG voltage	0	R/W
D[2]	OTG Voltage, Bit 0	0 = Adds 0mV of OTG voltage (default) 1 = Adds 8mV of OTG voltage	0	R/W
D[1:0]	Reserved	Reserved.	00	R/W

OTGCurrent Register (SMBus Address = 3Ch) [Reset =0000h]

The OTG output current limit is set in OTGCurrent register.

Table 18. OTGCurrent Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	Reserved	Reserved.	0	R/W
D[14]	OTG Current Set by Host, Bit 6	n = D[6:0] OTG Output Current Limit Value = 50n (mA) Range: 0mA (0000000) - 6350mA (1111111)	0	R/W
D[13]	OTG Current Set by Host, Bit 5		0	R/W
D[12]	OTG Current Set by Host, Bit 4		0	R/W
D[11]	OTG Current Set by Host, Bit 3		0	R/W
D[10]	OTG Current Set by Host, Bit 2		0	R/W
D[9]	OTG Current Set by Host, Bit 1		0	R/W
D[8]	OTG Current Set by Host, Bit 0		0	R/W
D[7:0]	Reserved	Reserved.	0000 0000	R/W

REGISTER AND DATA (continued)

ADCVBUS/PSYS Register (SMBus Address = 23h)

• VBUS: Range from 3200mV to 19520mV with 64mV LSB
• PSYS: Range from 0V to 3.06V with 12mV LSB

Table 19. ADCVBUS/PSYS Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:8]		8-Bit Digital Output of Input Voltage	0000 0000	R
D[7:0]		8-Bit Digital Output of System Power	0000 0000	R

ADCIBAT Register (SMBus Address = 24h)

• ICHG: Range from 0A to 8.128A with 64mA LSB
• IDCHG: Range from 0A to 32.512A with 256mA LSB

Table 20. ADCIBAT Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15]	Reserved	Reserved.	0	R
D[14:8]		7-Bit Digital Output of Battery Charge Current	000 0000	R
D[7]	Reserved	Reserved.	0	R
D[6:0]		7-Bit Digital Output of Battery Discharge Current	000 0000	R

ADCIINCMPIN Register (SMBus Address = 25h)

• IIN: Range from 0A to 12.75A with 50mA LSB
• CMPIN: Range from 0V to 3.06V with 12mV LSB

Table 21. ADCIINCMPIN Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:8]		8-Bit Digital Output of Input Current	0000 0000	R
D[7:0]		8-Bit Digital Output of CMPIN voltage	0000 0000	R

ADCVSYSVBAT Register (SMBus Address = 26h)

• VSYS: Range from 2.88V to 19.2V with 64mV LSB
• VBAT: Range from 2.88V to 19.2V with 64mV LSB

Table 22. ADCVSYSVBAT Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:8]		8-Bit Digital Output of System Voltage	0000 0000	R
D[7:0]		8-Bit Digital Output of Battery Voltage	0000 0000	R

REGISTER AND DATA (continued)

ID Registers

ManufactureID Register (SMBus Address = FEh) [Reset = 07h]

Table 23. ManufactureID Register Details

BITS	BIT NAME	DESCRIPTION (READ ONLY)	PORV	TYPE
D[15:8]	Reserved	Reserved.	0000 0000	R
D[7:0]	MANUFACTURE_ID	07h	0000 0111	R

DeviceID (DeviceAddress) Register (SMBus Address = FFh) [Reset = 88h]

Table 24. DeviceID (DeviceAddress) Register Details

BITS	BIT NAME	DESCRIPTION (READ ONLY)	PORV	TYPE
D[15:8]	Reserved	Reserved.	0000 0000	R
D[7:0]	DEVICE_ID	SMBus 88h = SGM41570	1000 1000	R

Setting Other Charge Options

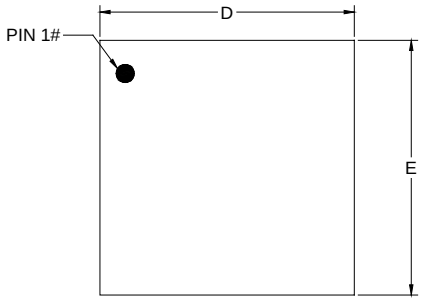
ChargeOption4 Register (SMBus Address = 36h) [Reset =00h]

Table 25. ChargeOption4 Register Details

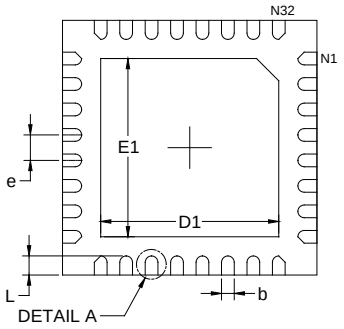
BITS	BIT NAME	DESCRIPTION	PORV	TYPE
D[15:2]	Reserved	Reserved.	00 0000	R/W
D[1:0]	PKPWR_TMAX2[1:0]	Peak Power Mode Overload and Relax Cycle Time 00 = The time follows the same PKPWR_TMAX[1:0] bits setting in ChargeOption2 Register (SMBus Address = 31h) (default) 01 = 100ms 10 = 500ms 11 = 1000ms	00	R/W

PACKAGE OUTLINE DIMENSIONS

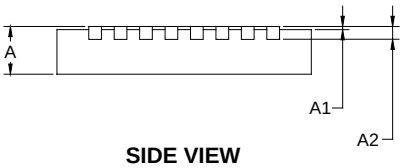
TQFN-4×4-32AL



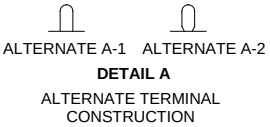
TOP VIEW



BOTTOM VIEW

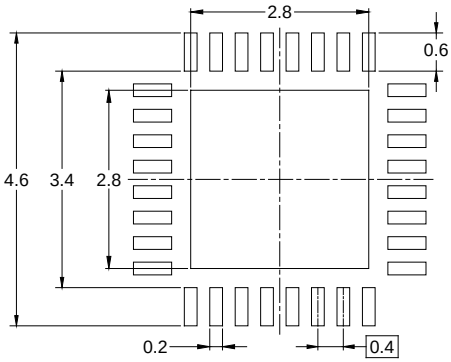


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



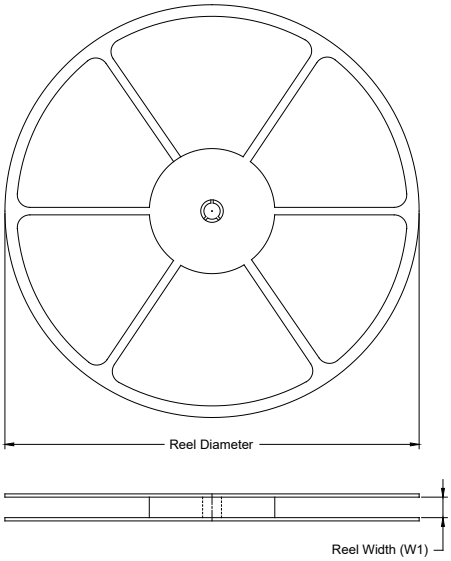
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.200 REF		
D	3.900	4.000	4.100
E	3.900	4.000	4.100
D1	2.700	2.800	2.900
E1	2.700	2.800	2.900
b	0.150	0.200	0.250
e	0.400 BSC		
L	0.250	0.300	0.350

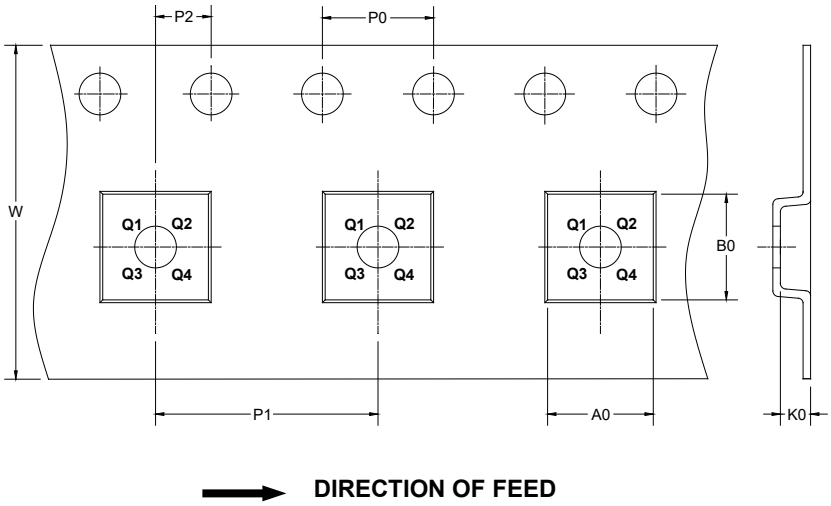
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



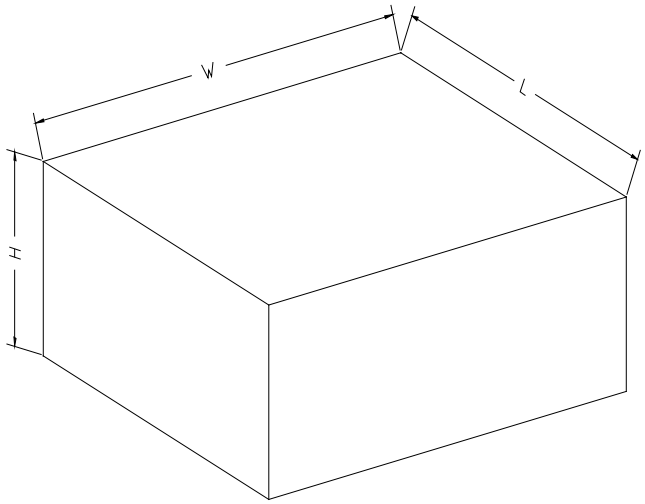
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-32AL	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002