

GENERAL DESCRIPTION

The SGM6029 family is a low voltage, efficient and miniature synchronous Buck converter with ultra-low quiescent current. Operating at high switching frequency (4.0MHz, TYP), miniature inductors and capacitors can be used to achieve minimal solution size. The rated load current is from 0.6A to 1A depending on the input voltage and operating frequency. For high light-load efficiency, the operating mode can smoothly and automatically change between power-save mode and PWM.

The dual-role VSEL/MODE pin sets the output voltage to one of the 16 preset values by sensing an external resistor during startup using an integrated resistor to digital (R2D) converter. After startup, this pin acts as MODE input and applying a logic high on it will force the device in the pulse width modulation (PWM) mode. This will allow using the same part for a wide range of voltage rails in different applications and offer a better output accuracy compared to the conventional external feedback resistor divider. In the forced-PWM (FPWM), the device switches at 4.0MHz (A, B and C versions) or 1.5MHz (D and E versions). High switching frequency reduces the output ripple, but at lighter loads, sacrifices the efficiency a little bit.

The SGM6029 is available in a Green WLCSP-0.74×1.09-6B package.

FEATURES

- 1.95V to 5.5V Input Voltage Range
- 2.3µA (TYP) Quiescent Current
- Selectable Switching Frequency of 4.0MHz or 1.5MHz
- 0.4V Internal Reference Voltage
- 0.6A to 1A Peak Output Current
- 2% Output Voltage Regulation Accuracy Full Temperature Range
- Programmable Light Load PSM or FPWM
- Simple Output Voltage Programming with Integrated R2D Converter
- 16 Selectable + 1 Fixed Output Voltage Levels:
 - ♦ SGM6029A (4.0MHz): 0.4V to 0.775V
 - ♦ SGM6029B (4.0MHz): 0.8V to 1.55V
 - ♦ SGM6029C (4.0MHz): 1.8V to 3.3V
 - ♦ SGM6029D (1.5MHz): 0.4V to 0.775V
 - ♦ SGM6029E (1.5MHz): 0.8V to 1.55V
- Enable Pin with Auto Pull-Down during Startup
- Miniature 0201 Optimized Pinout
- Output Discharge Feature (When Disabled)
- 100% Duty Cycle Operation Capability
- Available in a Green WLCSP-0.74×1.09-6B Package

APPLICATIONS

- Wearable Electronics
- IoT Applications
- 2 × 1.5V Battery Powered Applications
- Smart Phones

TYPICAL APPLICATION

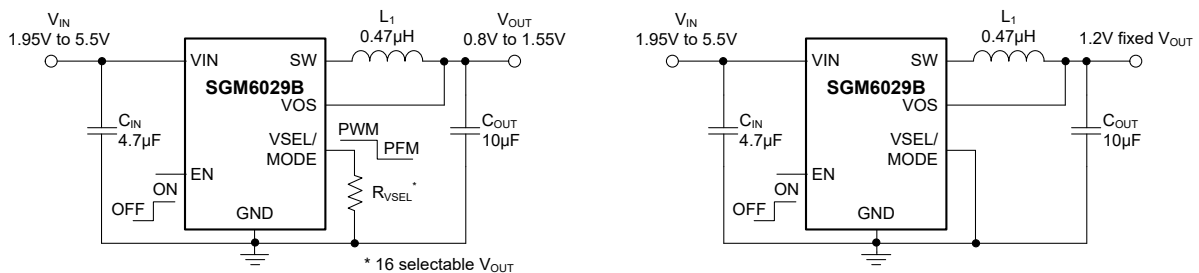


Figure 1. Typical Application Circuits

PACKAGE/ORDERING INFORMATION

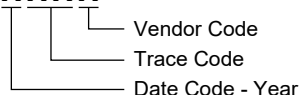
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6029A ⁽¹⁾	WLCSP-0.74×1.09-6B	-40°C to +85°C	SGM6029AYG/TR	XXXX SVQ	Tape and Reel, 3000
SGM6029B	WLCSP-0.74×1.09-6B	-40°C to +85°C	SGM6029BYG/TR	XXXX SVR	Tape and Reel, 3000
SGM6029C	WLCSP-0.74×1.09-6B	-40°C to +85°C	SGM6029CYG/TR	XXXX SVS	Tape and Reel, 3000
SGM6029D ⁽¹⁾	WLCSP-0.74×1.09-6B	-40°C to +85°C	SGM6029DYG/TR	XXXX SVT	Tape and Reel, 3000
SGM6029E ⁽¹⁾	WLCSP-0.74×1.09-6B	-40°C to +85°C	SGM6029EYG/TR	XXXX SVU	Tape and Reel, 3000

NOTE: 1. Product Preview.

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.

XXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

DEVICE DESCRIPTION

Device	Function VSEL/MODE	Fixed V _{OUT} (V)	Selectable Output Voltages with R _{VSEL}	I _{OUT} (A)	f _{sw} (MHz)	Soft-Start t _{SS} (μs)	Output Discharge
SGM6029A	VSEL + MODE	0.7 (VSEL/MODE = GND)	0.4V ~ 0.775V in 25mV steps	1	4.0	200	Yes
SGM6029B	VSEL + MODE	1.2 (VSEL/MODE = GND)	0.8V ~ 1.55V in 50mV steps	1	4.0	200	Yes
SGM6029C	VSEL + MODE	1.8 (VSEL/MODE = GND)	1.8V ~ 3.3V in 100mV steps	1	4.0	400	Yes
SGM6029D	VSEL + MODE	0.7 (VSEL/MODE = GND)	0.4V ~ 0.775V in 25mV steps	0.6	1.5	200	Yes
SGM6029E	VSEL + MODE	1.2 (VSEL/MODE = GND)	0.8V ~ 1.55V in 50mV steps	0.6	1.5	200	Yes

ABSOLUTE MAXIMUM RATINGS

VIN Voltage	-0.3V to 6V
SW Voltage	-0.3V to VIN + 0.3V
SW (AC), Less than 10ns, while Switching Voltage	-1V to 8V
EN, VSEL/MODE Voltages	-0.3V to VIN + 0.3V
VOS Voltage	-0.3V to 5V
Package Thermal Resistance	
WLCSP-0.74×1.09-6B, θJA	214°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility	
HBM	4000V
CDM	1000V

OVERSTRESS CAUTION

Stresses beyond the limits listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

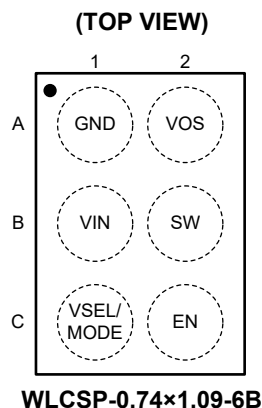
DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, VIN	1.95V to 5.5V
Output Current, IOUT (MAX)	
SGM6029A/SGM6029B/SGM6029C, VIN ≥ 2.3V	1A
SGM6029A/SGM6029B/SGM6029C, VIN < 2.3V	0.7A
SGM6029D/SGM6029E	0.6A
Effective Inductance, L	
SGM6029A/B/C	0.33μH to 1μH, 0.47μH (TYP)
SGM6029D/SGM6029E	0.7μH to 1.2μH, 1.0μH (TYP)
Effective Output Capacitance, COUT	
SGM6029A/SGM6029B/SGM6029C	5μF to 10μF
SGM6029D/SGM6029E	5μF to 10μF
Effective Input Capacitance, CIN	2.2μF to 4.7μF (TYP)
External Parasitic Capacitance at VSEL/MODE Pin, CVSEL/MODE	30pF (MAX)
Resistance Range for External Resistor at VSEL/MODE Pin (E96 1% Resistor Values), RVSEL	10kΩ to 249kΩ
External Resistor Tolerance E96 Series at VSEL/MODE Pin	1% (MAX)
E96 Resistor Series Temperature Coefficient (TC)	-200ppm/°C to +200ppm/°C
Operating Junction Temperature Range	-40°C to +125°C

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	DESCRIPTION
A1	GND	G	Ground Pin. Connect the C_{IN} and C_{OUT} ground terminals close to this pin.
A2	VOS	I	Output Voltage Sense Input. This pin is internally connected to the feedback loop and a MOSFET to discharge the output (V_{OUT}) when the device is disabled. Connect it with a short trace to the output capacitor.
B1	VIN	P	Power Supply Input. Connect a ceramic capacitor (C_{IN}) close to this pin and GND.
B2	SW	O	Switching Node Output. Connect it to the filter inductor.
C1	VSEL/MODE	I	Connect an accurate resistor between this pin and GND to select one of the 16 preset output voltage values. An R2D converter is only enabled during startup to read this resistor. After startup, this pin acts as MODE input. A logic high sets the device in the FPWM mode and a logic low selects the power-save mode operation.
C2	EN	I	Active High Enable Input. Apply a logic high voltage to enable the device or a logic low to disable it. During the initial phase of startup, an internal 570k Ω pull-down resistor is temporarily connected to the EN input. The pull-down resistor is removed after all internal circuits are powered up and functional.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_J = +40°C to +125°C, typical values are at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supplies						
Input Voltage Range	V _{IN}		1.95		5.5	V
Quiescent Current (Power-Save Mode)	I _Q	V _{EN} = V _{IN} , I _{OUT} = 0μA, V _{OUT} = 1.2V, device not switching		2.3	5.5	μA
		V _{EN} = V _{IN} , I _{OUT} = 0μA, V _{OUT} = 1.2V, device switching		2.8		
Quiescent Current (PWM Mode)		V _{EN} = V _{IN} , I _{OUT} = 0mA, V _{OUT} = 1.2V, VSEL/MODE = V _{IN} (after power-up), device switching		8.5		mA
Shutdown Current	I _{SD}	EN = GND, shutdown current into V _{IN} , VSEL/MODE = GND, T _J = -40°C to +85°C		120	250	nA
Under-Voltage Lockout Threshold	V _{UVLO}	V _{IN} rising		1.76	1.95	V
Input EN						
High Level Input Voltage	V _{IH}		0.85			V
Low Level Input Voltage	V _{IL}				0.40	V
Input Bias Current	I _{IN}	EN = high, T _J = -40°C to +85°C		10	100	nA
Internal Pull-Down Resistance	R _{PD}	EN = low		570		kΩ
Input VSEL/MODE						
High Level Input Voltage (Digital Input)	V _{IH}		0.89			V
Low Level Input Voltage (Digital Input)	V _{IL}				0.40	V
Input Bias Current	I _{IN}	EN = high		10	130	nA
Power Switches						
Leakage Current into SW Pin	I _{LKG_SW}	V _{SW} = 1.2V, T _J = -40°C to +85°C		1	50	nA
High-side MOSFET On-Resistance	R _{DSON}	I _{OUT} = 100mA		185	310	mΩ
Low-side MOSFET On-Resistance		I _{OUT} = 100mA		125	230	
High-side MOSFET Switch Current Limit	I _{LIMF}	T _J = +25°C	1.58	1.78	1.98	A
Low-side MOSFET Switch Current Limit		T _J = +25°C	0.90	1.20	1.50	
MOSFET On-Resistance	R _{DSCHE_SW}	EN = GND, I _{SW} = -10mA into SW pin, T _J = -40°C to +85°C		4	11	Ω
Bias Current into VOS Pin	I _{IN_VOS}	EN = V _{IN} , V _{OUT} = 1.2V (internal 7MΩ resistor divider), T _J = -40°C to +85°C		250	450	nA
Thermal Protection						
Thermal Shutdown Temperature	T _{SD}	Rising junction temperature, PWM mode		160		°C
Thermal Shutdown Hysteresis	T _{HYS}			20		°C
Output						
Output Voltage Range	V _{OUT}	SGM6029A/SGM6029D, 25mV steps	0.4		0.775	V
		SGM6029B/SGM6029E, 50mV steps	0.8		1.55	
		SGM6029C, 100mV steps	1.8		3.3	
Output Voltage Accuracy		Power-Save mode		0.5		%
		PWM mode, I _{OUT} = 0mA	-2	0	2	

ELECTRICAL CHARACTERISTICS (continued)(V_{IN} = 3.6V, T_J = +40°C to +125°C, typical values are at T_J = +25°C, unless otherwise noted.)

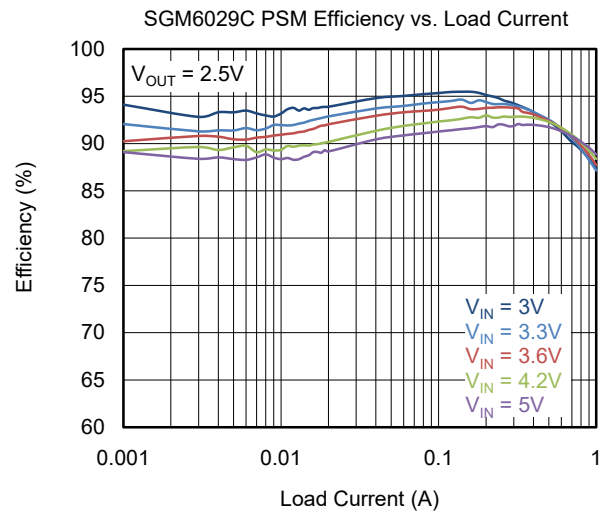
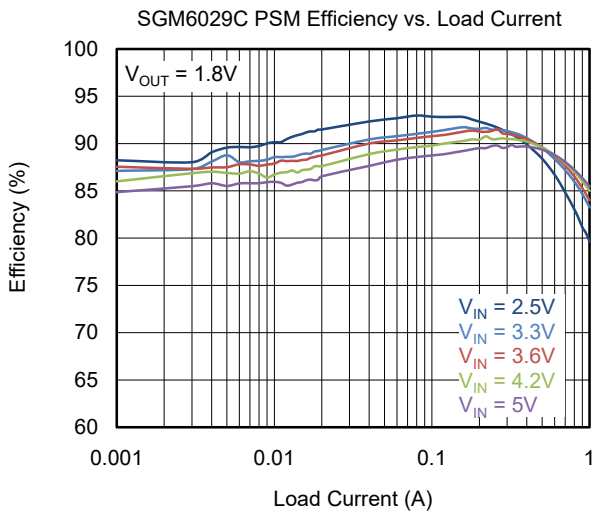
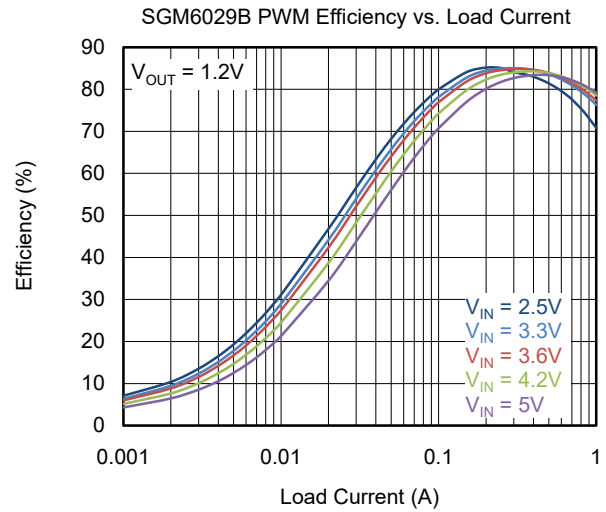
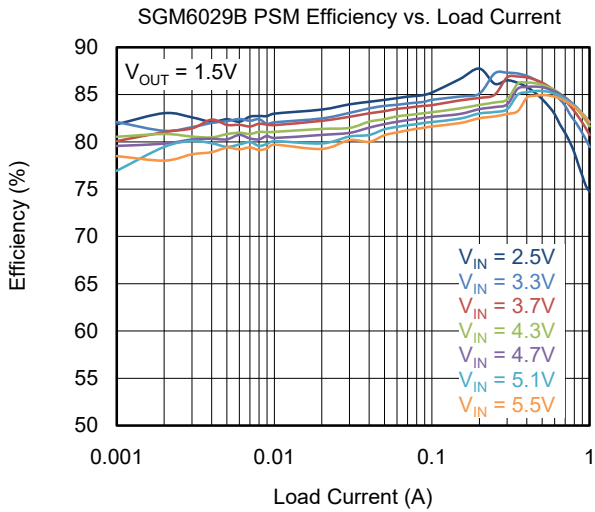
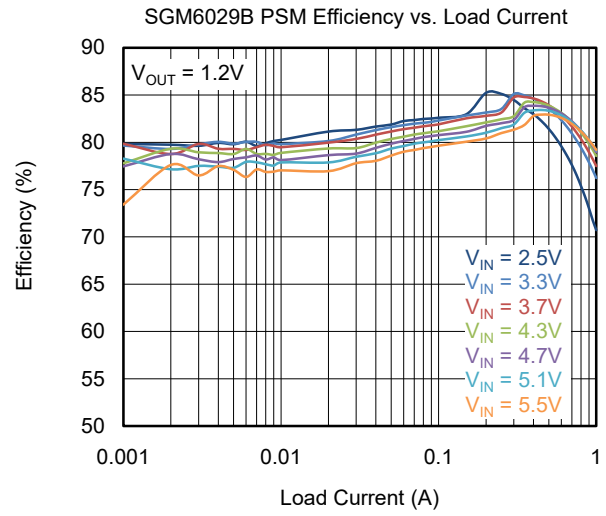
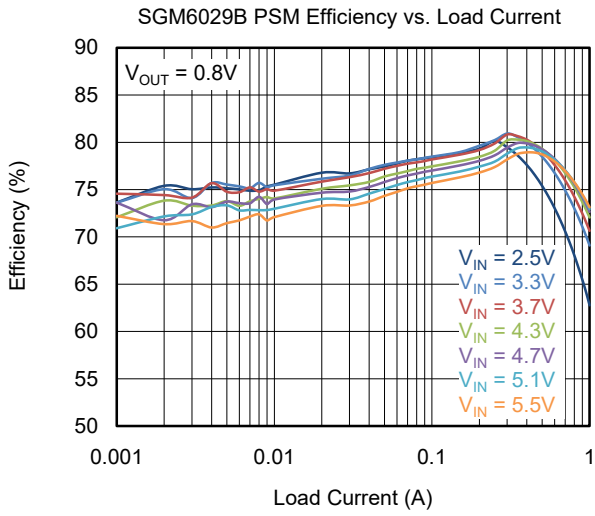
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	f _{SW}	SGM6029A/SGM6029B/SGM6029C		4		MHz
		SGM6029D/SGM6029E		1.5		
Regulator Startup Delay Time	t _{STARTUP_DELAY}	Delay from EN low to high transition until device starts switching, VSEL = 16		700	1170	μs
Soft-Start Time	t _{SS}	SGM6029A/SGM6029B/SGM6029D/SGM6029E, V _{OUT} rising from 0V to 0.95% × V _{OUT} nominal		200	500	μs
		SGM6029C, V _{OUT} rising from 0V to 0.95% × V _{OUT} nominal		410	785	

OUTPUT VOLTAGE SETTINGTable 1. Selecting the Programming Resistor (R_{VSEL}) for Output Voltage Setting (VSEL/MODE Pin)

VSEL	Output Voltage Setting V _{OUT} (V)			R _{VSEL} Resistance (E96, 1%, TC ± 200ppm/°C)
	SGM6029A/ SGM6029D	SGM6029B/ SGM6029E	SGM6029C	
0	0.700	1.2	1.8	Short to GND
1	0.400	0.8	1.8	10.0kΩ
2	0.425	0.85	1.9	12.1kΩ
3	0.450	0.9	2.0	15.4kΩ
4	0.475	0.95	2.1	18.7kΩ
5	0.500	1.0	2.2	23.7kΩ
6	0.525	1.05	2.3	28.7kΩ
7	0.550	1.1	2.4	36.5kΩ
8	0.575	1.15	2.5	44.2kΩ
9	0.600	1.2	2.6	56.2kΩ
10	0.625	1.25	2.7	68.1kΩ
11	0.650	1.3	2.8	86.6kΩ
12	0.675	1.35	2.9	105.0kΩ
13	0.700	1.4	3.0	133.0kΩ
14	0.725	1.45	3.1	162.0kΩ
15	0.750	1.5	3.2	205.0kΩ
16	0.775	1.55	3.3	249.0kΩ or larger

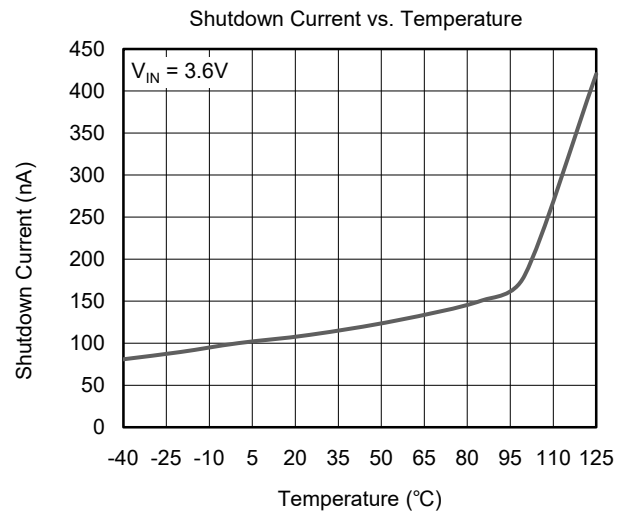
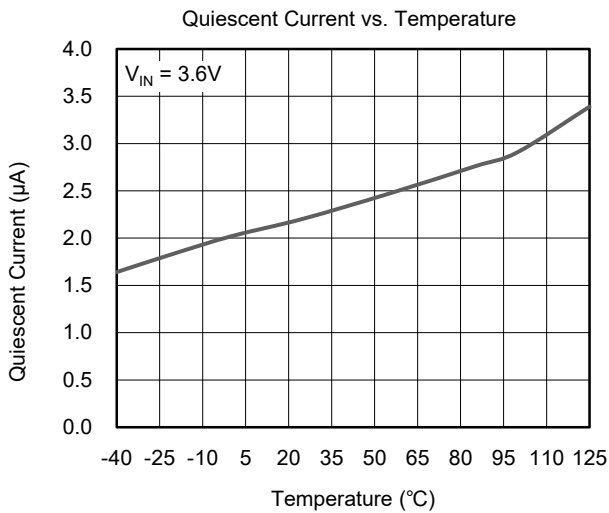
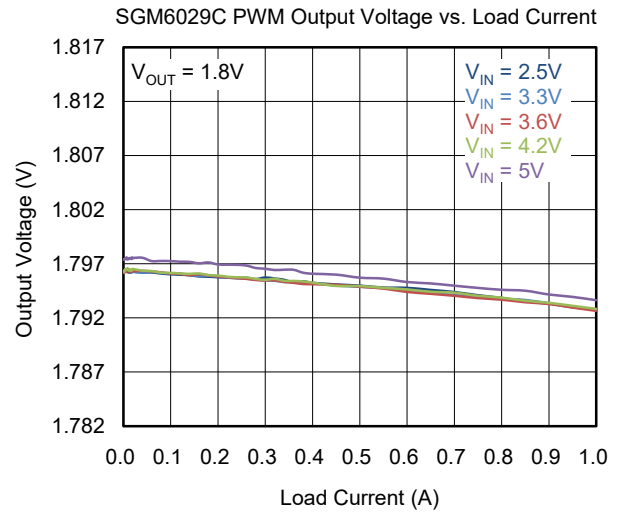
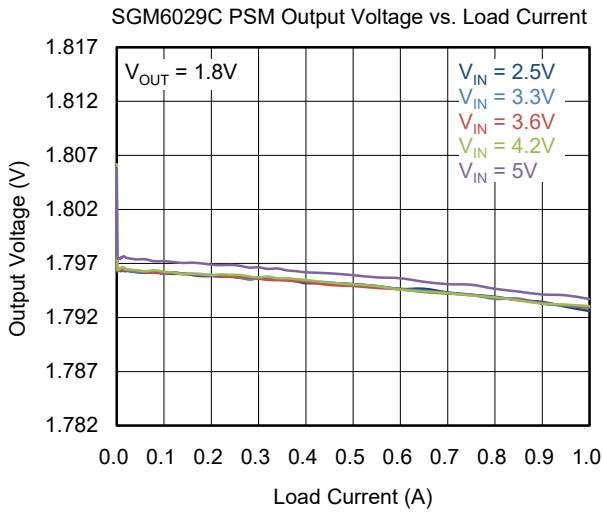
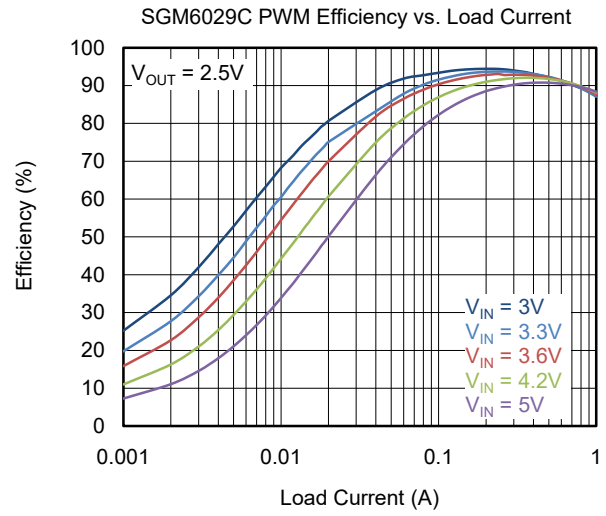
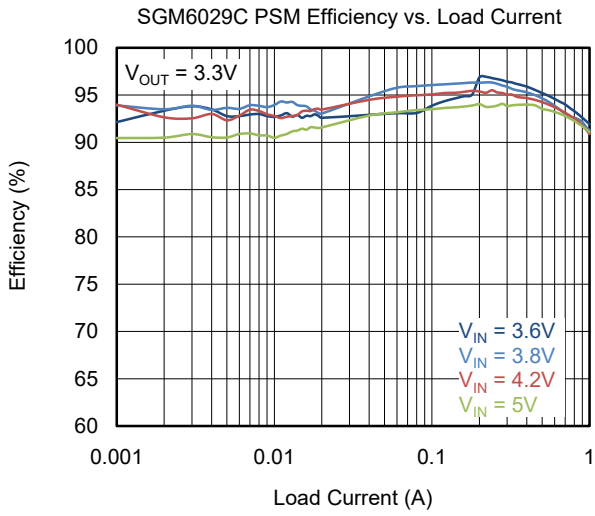
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, L = 0.47µH for SGM6029A/SGM6029B/SGM6029C, L = 1µH for SGM6028D/SGM6029E, unless otherwise noted.



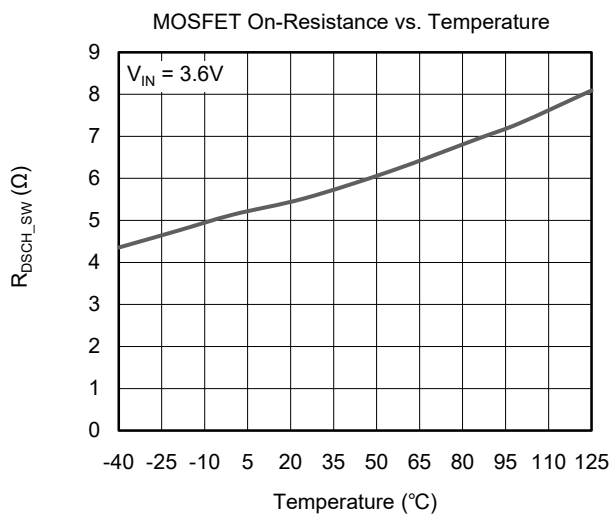
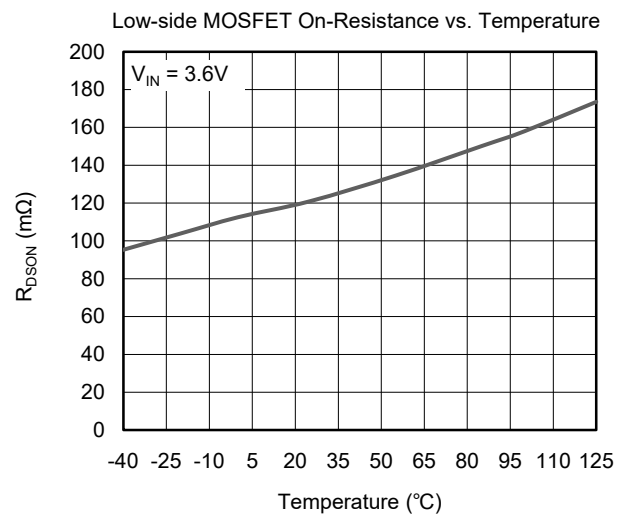
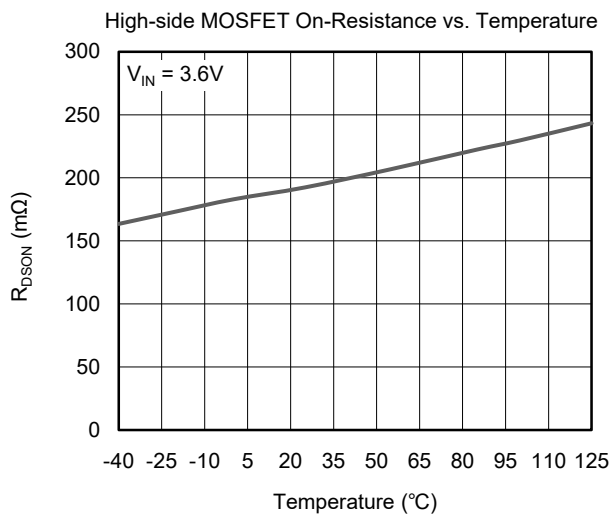
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

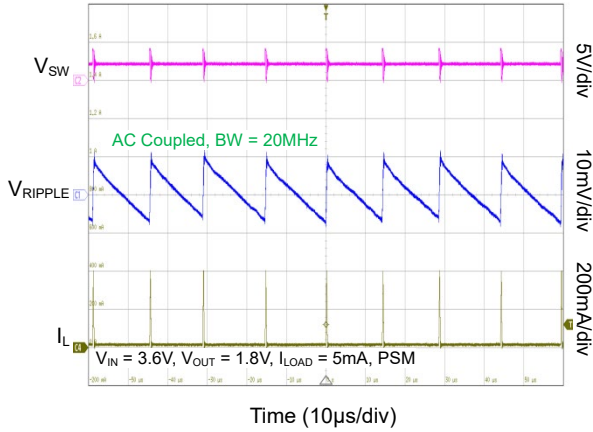
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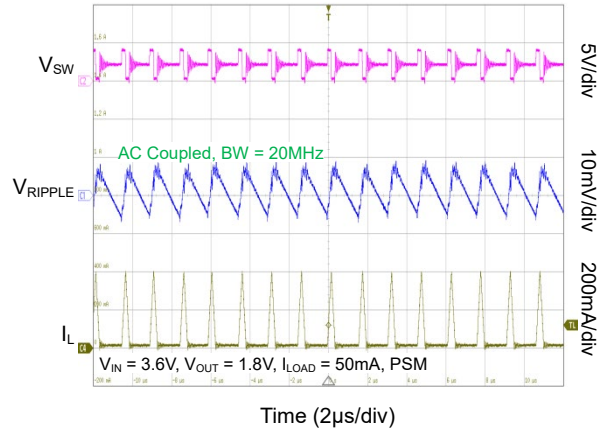
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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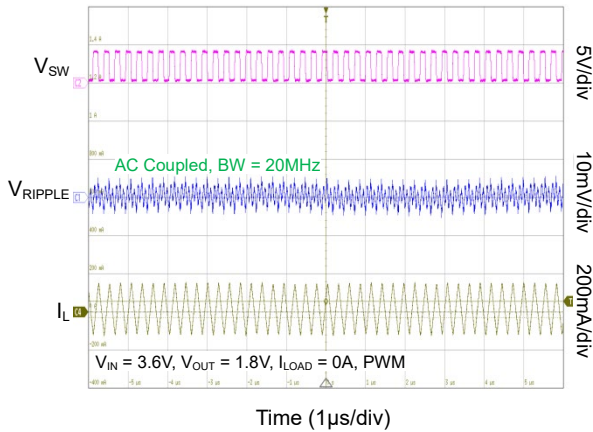
SGM6029C Output Voltage Ripple



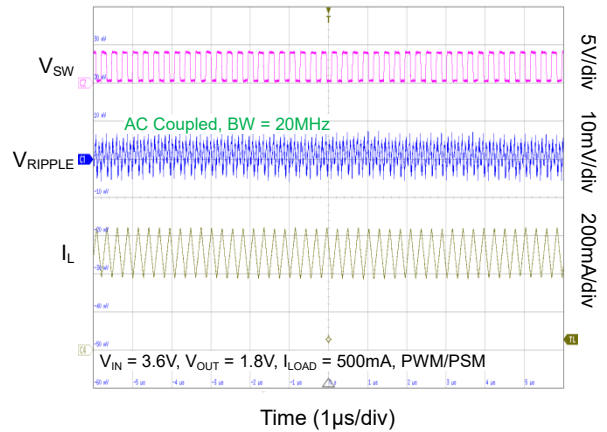
SGM6029C Output Voltage Ripple



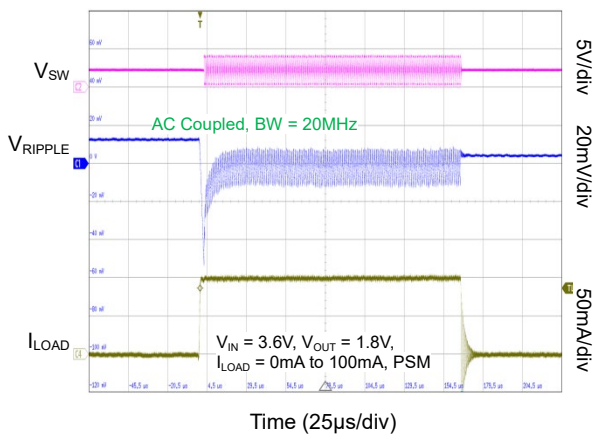
SGM6029C Output Voltage Ripple



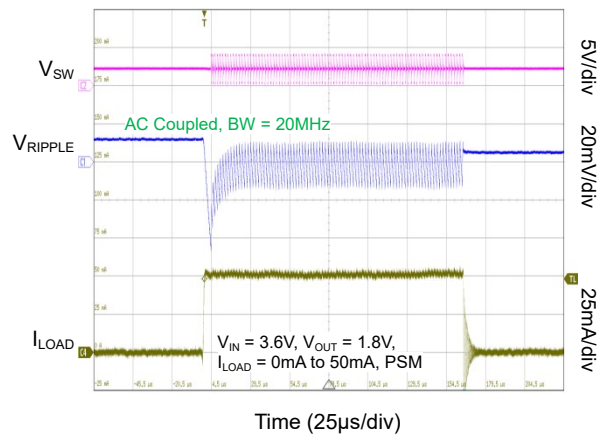
SGM6029C Output Voltage Ripple



SGM6029C Load Transition



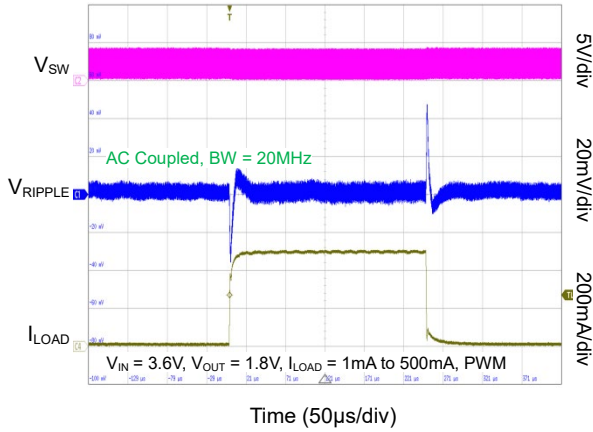
SGM6029C Load Transition



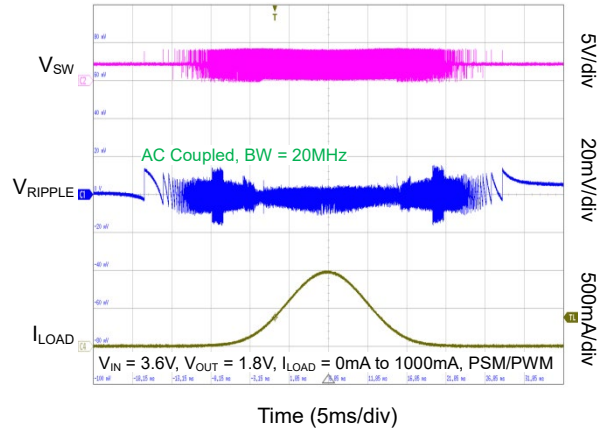
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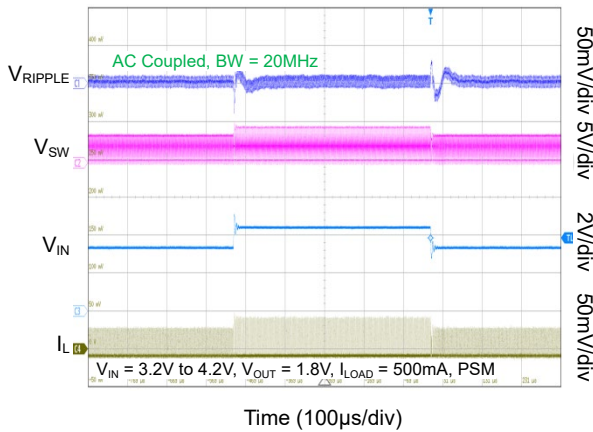
SGM6029C Load Transition



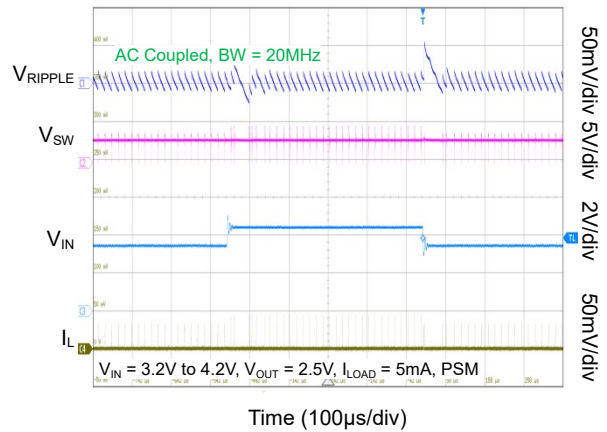
SGM6029C Load Sweep



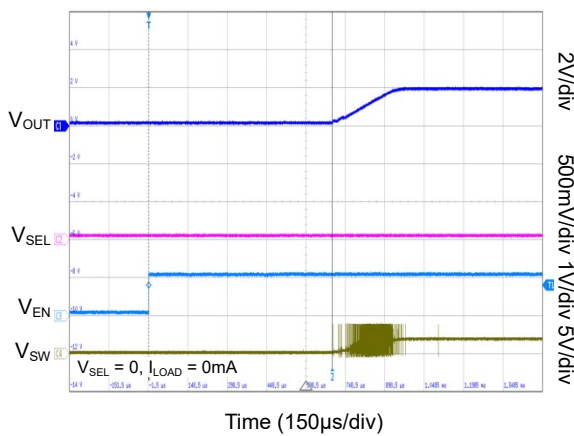
SGM6029C Line Transition



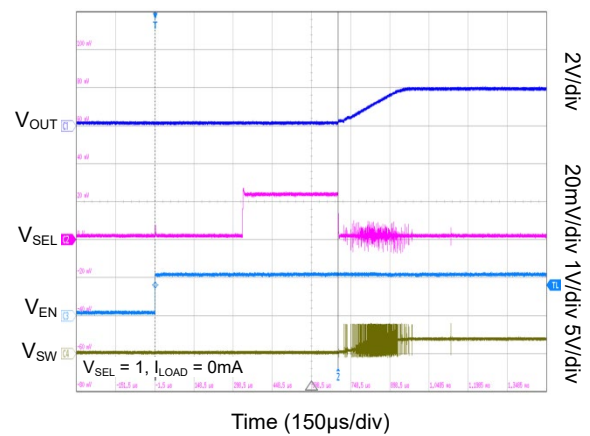
SGM6029C Line Transition



SGM6029C Startup Delay Time



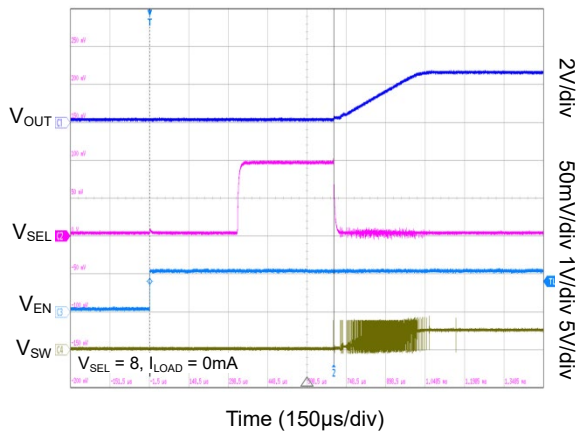
SGM6029C Startup Delay Time



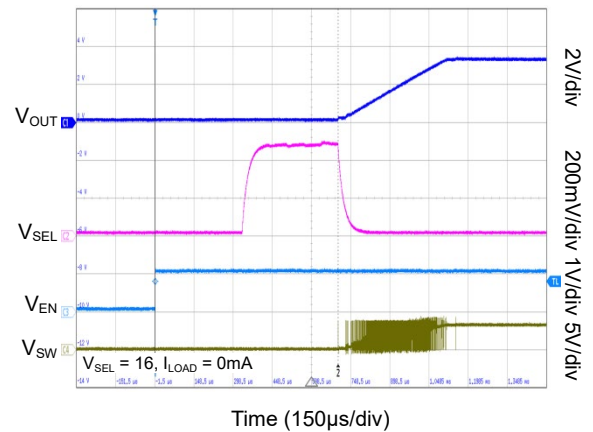
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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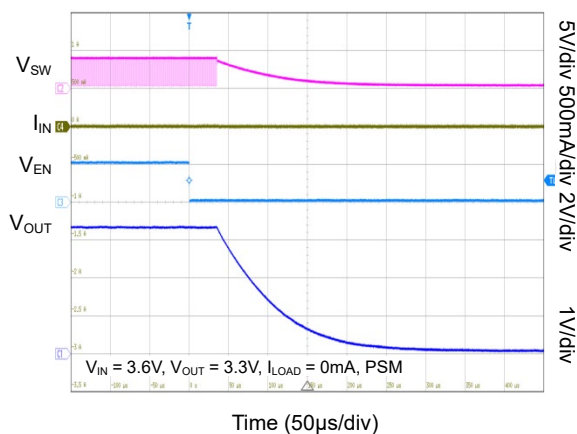
SGM6029C Startup Delay Time



SGM6029C Startup Delay Time



SGM6029C Output Discharge



FUNCTIONAL BLOCK DIAGRAM

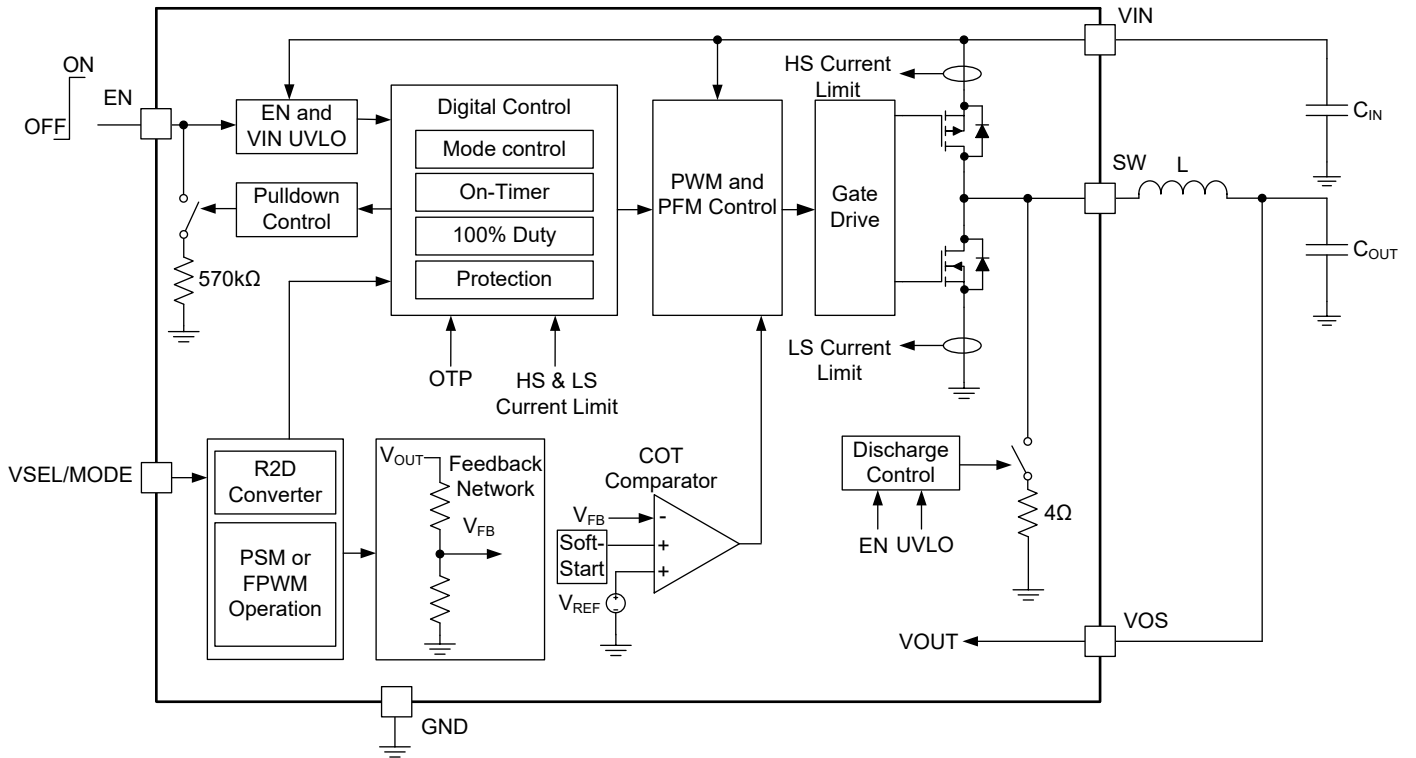


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM6029 family is a low quiescent current and high frequency synchronous Buck converter. It offers high efficiency over a wide load range including very low output currents in the power-save mode. It can be set to forced-PWM mode or automatic power-save mode/PWM mode. It features seamless and automatic transitions between power-save mode and PWM mode based on the inductor current continuity (CCM or DCM). The controllers have combined benefits of the hysteretic and voltage mode control and provide very low output ripple, outstanding DC and AC regulation and excellent transient response. Other than the accurate DC voltage feedback loop, the AC deviations of the output are also sensed by the VOS pin and are fed back to a second loop that controls the ramp signal of the comparator in the modulator stage. This arrangement provides fixed operation frequency in steady state but quickly changes the frequency upon a dynamic load change for instant response. The controller is internally compensated and is stable with low ESR output ceramic capacitors. These converters are perfect for the applications that require high efficiency at very light loads like small battery operated systems.

VIN Under-Voltage Lockout Protection (UVLO)

To avoid device malfunctioning when the VIN voltage is insufficient and for proper powering of the whole internal circuit, the input supply is constantly monitored to make sure it is above the under-voltage lockout (UVLO) threshold. When the device re-enters operation from UVLO status (V_{IN} rising), it will act like being enabled. Every time the device is disabled and enabled, a startup sequence with VSEL R2D converter will occur.

Enable Control and Shutdown Mode (EN Pin)

A logic low on the EN input will disable (shut down) the device and a high logic turns it on. To avoid problems caused by insufficient EN pull-down or floating during startup, such as weak pull-down at low voltage startup conditions, an internal 570k Ω resistor pulls this pin to GND during startup. This pull-down resistor is removed when the internal circuit and the reference have been powered up and stabilized. If the EN pin goes low, the SGM6029 is disabled and the internal pull-down resistor will connect.

Internal Soft-Start

If VIN voltage is in the operating range, when the EN is pulled high, the device is powered up and initialized within the startup delay time ($t_{STARTUP_DELAY}$). Then the converter starts to switch and the output voltage ramps up during the soft-start time (t_{SS}) as shown in Figure 3. The $t_{STARTUP_DELAY}$ duration depends on the selected output voltage (V_{SEL}). It is the shortest when $V_{SEL} = 0$ and the longest when $V_{SEL} = 16$.

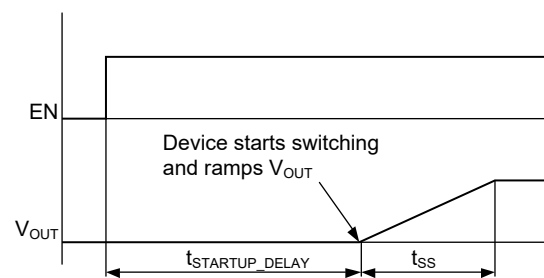


Figure 3. SGM6029 Startup Timings

DETAILED DESCRIPTION (continued)**The VSEL/MODE Pin**

VSEL/MODE is a dual-role pin. During startup, this pin acts as VSEL input and senses the connected resistor value for output voltage selection. After startup, it functions as MODE selection input to set the device operating mode in the forced-PWM (high) or power-save mode (low). See the Device Comparison Table and the VSEL resistor values (Table 1) for details.

Resistor to Digital (R2D) Converter and Selection of the Output Voltage

An external resistor (R_{VSEL}) placed between the VSEL/MODE pin and GND determines the output voltage. After enabling the device and when the internal reference is stable, the resistor to digital (R2D) converter starts sensing the R_{VSEL} before the $t_{STARTUP_DELAY}$ ends. A current is injected in the R_{VSEL} and an ADC reads the resulting voltage. Based on the sensed voltage, one of the preset internal feedback resistor dividers is chosen to set the output voltage. After completing R2D conversion, current injection is stopped and no current flows out of the VSEL/MODE pin. The output voltage is selected and fixed once and during startup only. Make sure there is no other external current leakage or capacitance ($>30\text{pF}$) present on this pin during VSEL detection or UVLO events to avoid wrong V_{OUT} setting. Use the E96 resistor values with maximum 1% tolerance and good thermal stability ($TC < 200\text{ppm}/^\circ\text{C}$) to set the output voltage as suggested in Table 1. Note that the R_{VSEL} does not affect the output accuracy.

Shorting VSEL to GND sets the default output voltage (SGM6029A/SGM6029D = 0.7V, SGM6029B/SGM6029E = 1.2V, SGM6029C = 1.8V) and saves more space by reducing one external resistor.

Power-Save Mode and Forced-PWM (FPWM) Operation Mode Selection

After the power-up period, the VSEL/MODE pin acts as mode select input. A logic low applied to this input selects the power-save mode and a logic high selects FPWM operation. Changing the mode during operation (after completing VSEL function) is allowed.

Output Voltage Discharge

To ensure that the output voltage drops to 0V in a controlled manner and remains close to 0V while the

device is disabled, a resistor (4Ω , TYP) is connected between the converter output and GND through the VOS pin as soon as the device is disabled. The output voltage discharge feature is present only after enabling the device for the first time after the input supply is applied. It is not active if the device is disabled and then power supply is applied. To keep this feature active, the supply voltage must remain above the UVLO falling threshold ($V_{IN} > V_{TH_UVLO}$).

Power-Save Mode Operation

The SGM6029 controller has power-save mode operation capability. With power-save mode, the modulator can enter the pulse frequency modulation (PFM) rather than the fixed-frequency PWM switching at light loads. One switching pulse is applied to the LC filter to charge the output capacitor and keep the output regulated and then the device enters a long sleep period while the output capacitor supplies the small load current. During the sleep period between successive pulses, almost all internal circuits of the SGM6029 are turned off to minimize the quiescent current. The length of the sleep period is longer when the load is lighter. A higher inductor peak-current setting can also extend the off-time duration. For the SGM6029, the quiescent current can be reduced to the ultra-low levels in the order of $2.3\mu\text{A}$ (TYP). Such low quiescent current levels are achieved by integrating high impedance feedback divider inside the device, using a very low power voltage reference and improved power-save mode operation. The switching frequency is almost proportional to the load current in PFM mode. When the load is increased, the inductor current becomes continuous (CCM mode) and the device automatically enters the fixed-frequency PWM.

The nominal PWM switching frequency for SGM6029A/SGM6029B/SGM6029C is $f_{SW} = 4.0\text{MHz}$ and for SGM6029D/SGM6029E is $f_{SW} = 1.5\text{MHz}$. However, the exact frequency depends on V_{IN} and V_{OUT} . The change between PFM and PWM occurs when the inductor current becomes marginally discontinued (valley current reaches zero). Using a unified controller to manage PFM and PWM operations, this device can seamlessly change mode with minimum output voltage ripple due to the mode change.

DETAILED DESCRIPTION (continued)

Forced-PWM Mode (FPWM) Operation

If the FPWM mode is selected (MODE = high), the device runs at the fixed-frequency PWM in the entire load range. The FPWM mode reduces the light load efficiency due to the circulating currents, but the high frequency interference is significantly reduced due to the wider soft switching range of the converter at light loads and the relatively fixed-frequency spectrum of the noise.

100% Duty Cycle Operation Mode

When the voltage of the input source, such as battery, falls and its value is close to the output voltage, the PWM duty cycle ($D = V_{OUT}/V_{IN}$) increases to near 100%. Eventually the high-side switch remains continuously on to keep the output regulated. Even when the input voltage falls below the output, the high-side switch is turned on to minimize the error.

Short Circuit and Switch Current Limit Protections

To prevent damage to the SGM6029 or load when an output short circuit or over-current occurs, the high-side

and low-side MOSFET switch currents are monitored and limited in a cycle-by-cycle basis. If the high-side switch current exceeds its limit, it will be turned off and the low-side switch will be turned on to decrease the inductor current until it falls below the low-side current limit. At this time the low-side switch will be turned off and the high-side switch will be turned on again.

Thermal Shutdown Protection

To protect the device from overheating damage, thermal protection is included in the device. If the junction temperature (T_J) exceeds the thermal shutdown threshold ($T_{SD} = 160^\circ\text{C}$, TYP), both switches will be turned off. When the die cools down and T_J falls below hysteresis window (20°C , TYP), the switching resumes automatically after a soft-start. There is no R2D conversion after thermal shutdown and V_{OUT} sets to the previous value. Also please note that there is no thermal protection in the power-save mode.

APPLICATION INFORMATION

A few power supply design examples for some typical application with different input and output voltage requirements will be discussed in this section that can be used as reference. See Figure 4 and also other circuits provided in Figure 5 to Figure 10.

Typical Application

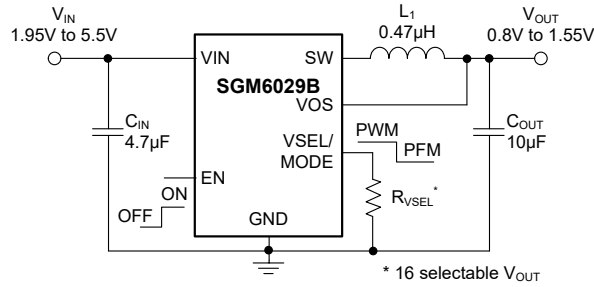


Figure 4. SGM6029B with Adjustable V_{OUT}

Design Requirements

The components designed for this application are listed in Table 2.

Table 2. Components for Application Characteristic Curves

Designed Component	Description/Part Number	Value/Main Parameters	Size (L × W × T) (mm ³ MAX)	Manufacturer
C _{IN}	GRT155R61A475ME13D	4.7µF, X5R, 10V, ±20%	0402 (1 × 0.5 × 0.5)	Murata
C _{OUT}	GRM155R61A106ME44D	10µF, X5R, 10V, ±20%	0402 (1 × 0.5 × 0.5)	Murata
L ₁	Inductor DFE18SANR47MG0L	0.47µH, 54mΩ (DCR _{max} @20°C), 2.6A (I _{max} , 40°C rise), 3.3A (I _{sat} , 30% L drop) ±20% (Initial Tolerance)	0603 (1.6 × 0.8 × 1.0)	Murata

Design Procedure

1. The V_{IN}, V_{OUT} and I_{OUT} requirements must be known to start the design.
2. For each application, the design can be optimized for efficiency, solution size or other factors.
3. Compare your design with solutions provided by SGMICRO.

Inductor Selection

The inductance of the output filter (L) determines the peak-to-peak ripple current and indirectly affects the converter efficiency and output voltage ripple. It also determines the current at which the PWM-to-PFM transition occurs (CCM to DCM). The ripple current (ΔI_L) can be estimated from Equation 1. It shows that ΔI_L decreases with larger inductance values and increases at higher voltage levels (V_{IN} or V_{OUT}).

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \tag{1}$$

In steady state, the maximum inductor current can be calculated from Equation 2.

$$I_{L_MAX} = I_{OUT_MAX} + \frac{\Delta I_L}{2} \tag{2}$$

Where, f is switching frequency, L is inductance value, ΔI_L is the inductor peak-to-peak ripple current and I_{L_MAX} is the peak inductor current. The maximum current should never reach the inductor saturation level. This situation can happen after a large load step. A common conservative option is to choose an inductor with a saturation current equal to or higher than the high-side switch current limit (I_{LIMF}).

Some of the inductor part numbers that satisfy these conditions are listed in Table 3.

APPLICATION INFORMATION (continued)

Table 3. A List of Inductors Suitable for this Application

Inductance (μH)	Part Number/Series	Size Imperial (Metric)	Size (L \times W \times T) (mm^3 MAX)	Manufacturer
0.47	DFE18SANR47ME0	0603(1608)	1.6 \times 0.8 \times 1.0	Murata
0.47	DFE18SANR47MG0L	0603(1608)	1.6 \times 0.8 \times 1.0	Murata
0.47	DFE201210U-R47M	0805(2012)	2.0 \times 1.2 \times 1.0	Murata
1.0	DFE201210U-1R0M	0805(2012)	2.0 \times 1.2 \times 1.1	Murata
0.47	HTEK12100F-R47MSR	0504(1210)	1.2 \times 1.0 \times 0.6	Cyntec
0.47	HTEL1412FE-R47MSR	0505(1412)	1.4 \times 1.2 \times 0.65	Cyntec
0.47/1.0	HTEL16080H	0603(1608)	1.6 \times 0.8 \times 0.8	Cyntec
1.0	HTEG20120G-1R0MDR	0805(2012)	2.0 \times 1.2 \times 0.7	Cyntec
0.47/1.0	HTEP20120H	0805(2013)	1.6 \times 0.8 \times 0.8	Cyntec

Input Capacitor (C_{IN})

A low ESR ceramic capacitor must be connected close to the VIN and GND pins to provide the pulsating input current of the converter and minimize switching noise and ringings. A 4.7 μF ceramic capacitor is satisfactory for most applications, however, if a high impedance source such as a coin cell-battery is used, larger input capacitance ($C_{\text{IN}} \geq 10\mu\text{F}$) is preferred to prevent voltage drops during startup or load steps. There is no high limit for the input capacitance, however, note that the higher leakage current of a large input capacitor will increase the total quiescent current of the power supply.

Some applicable input capacitors are listed in Table 4.

Table 4. Some Potential Part Numbers for the Input Capacitor

Capacitance (μF)	Capacitor Part Number	Size Imperial (Metric)	Size (L \times W \times T) (mm^3 MAX)	Manufacturer
10	GRM155R60J106ME	0402(1005)	1.0 \times 0.5 \times 0.5	Murata
10	GRM188R61A106M	0603(1608)	1.6 \times 0.8 \times 0.8	Murata
10	GRM188B30J106ME47	0603(1609)	1.6 \times 0.8 \times 0.9	Murata

Output Capacitor (C_{OUT})

Table 5 can be used to select the proper LC filter components for most design requirements. The inductor initial tolerance can be as high as -30% to +20% of the nominal value and proper current derating is usually required. Bias voltage can cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value.

$L_1 = 0.47\mu\text{H}$ or $1\mu\text{H}$ and $C_{\text{OUT}} = 10\mu\text{F}$ are the recommended values for the typical application of SGM6029A/SGM6029B/SGM6029C. $L_1 = 1\mu\text{H}$ and $C_{\text{OUT}} = 10\mu\text{F}$ are the recommended values for the typical application of SGM6029D/SGM6029E.

Table 5. Proper Output Capacitor and Inductor Combination

Device	L_1	C_{OUT}
SGM6029A/SGM6029B/SGM6029C	0.47 μH /1 μH	10 μF
SGM6029D/SGM6029E	1 μH	10 μF

APPLICATION INFORMATION (continued)

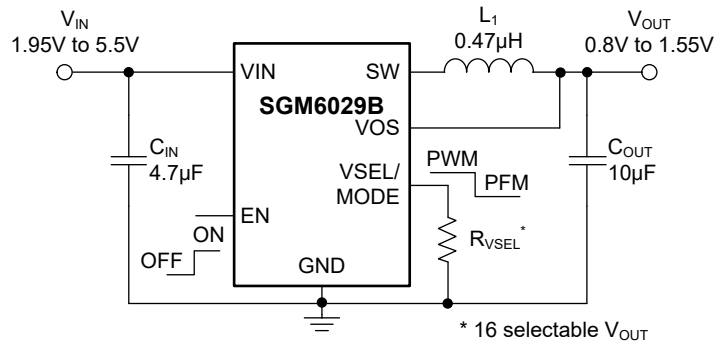


Figure 5. R_{VSEL} Selectable V_{OUT} (0.8V to 1.55V) with SGM6029B

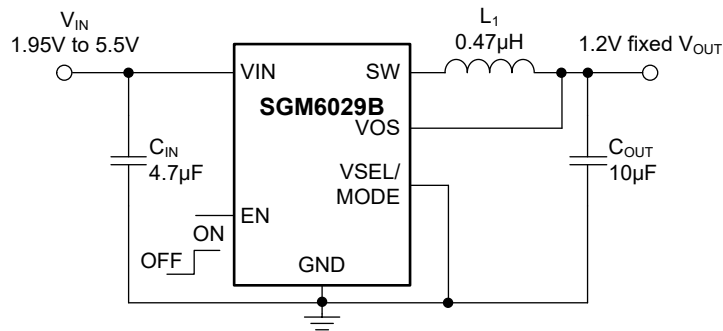


Figure 6. Fixed 1.2V Output with SGM6029B (VSEL is Grounded)

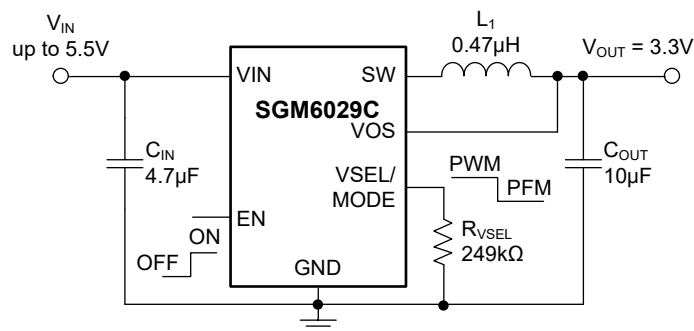


Figure 7. Adjustable Output Set to 3.3V with SGM6029C

APPLICATION INFORMATION (continued)

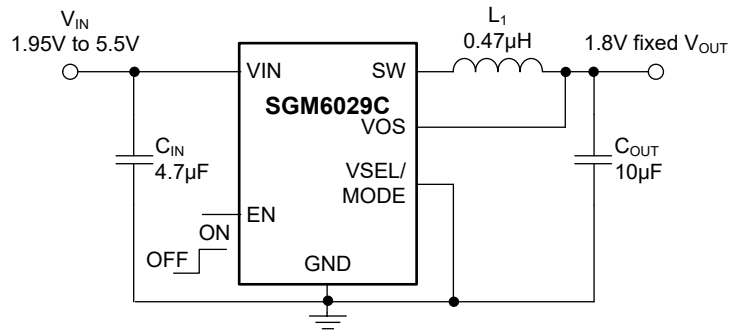


Figure 8. Fixed 1.8V Output with SGM6029C (VSEL is Grounded)

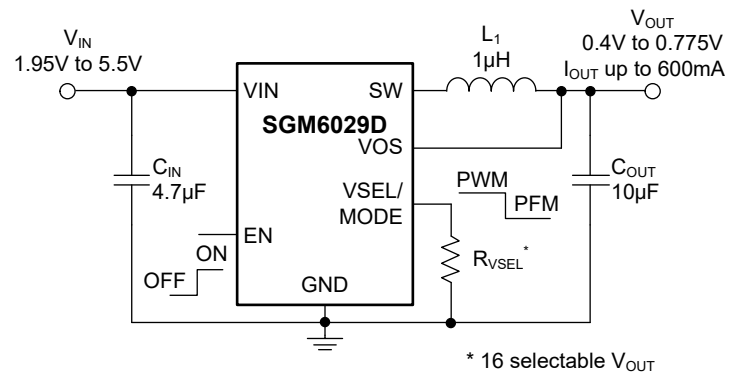


Figure 9. R_{VSEL} Selectable V_{OUT} (0.4V to 0.775V) with SGM6029D

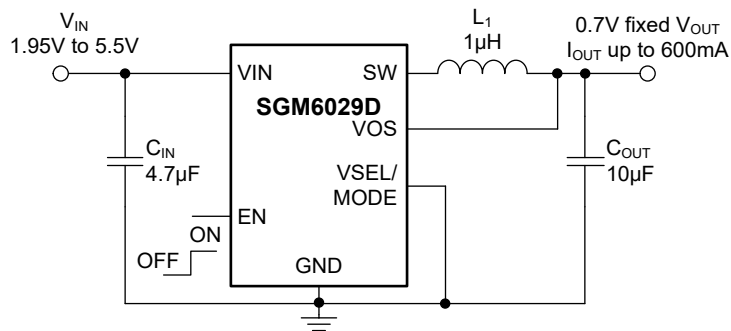


Figure 10. Fixed 0.7V Output with SGM6029D (VSEL Grounded)

APPLICATION INFORMATION (continued)

Layout Guidelines

A good printed-circuit-board (PCB) layout is a critical element of any high performance design. Follow the guidelines below for designing a good layout for the SGM6029.

- Place the input capacitor close to the device with the shortest possible connection traces.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device GND pin to minimize the AC current loops. Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep the signal traces like the VOS sense line away from SW or other noisy sources.

Refer to Figure 11 for a recommended PCB layout.

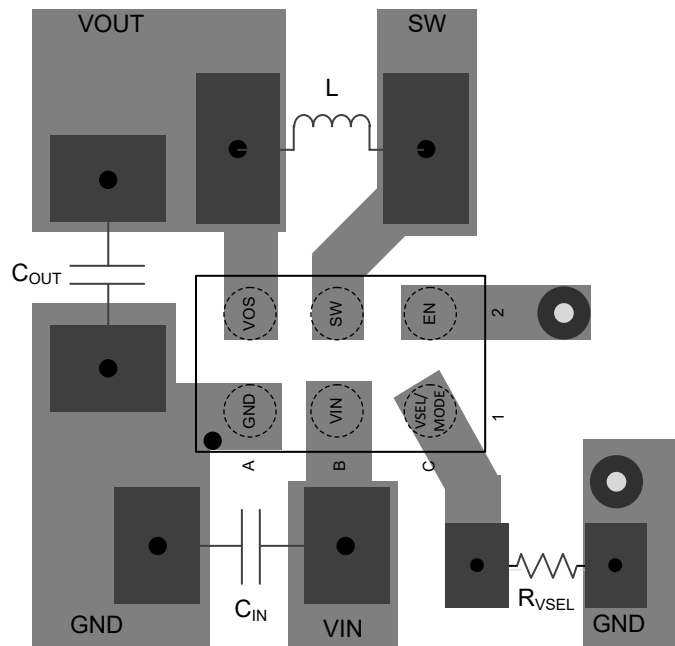


Figure 11. PCB Layout

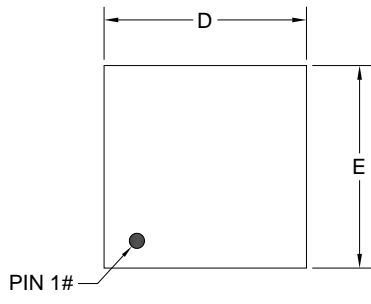
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

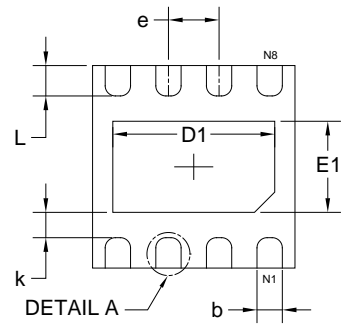
Changes from Original (SEPTEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

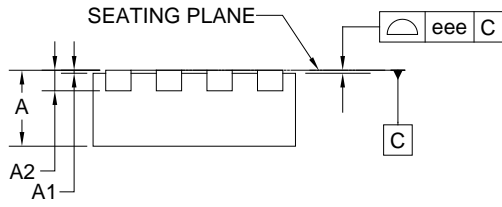
TDFN-2x2-8AL



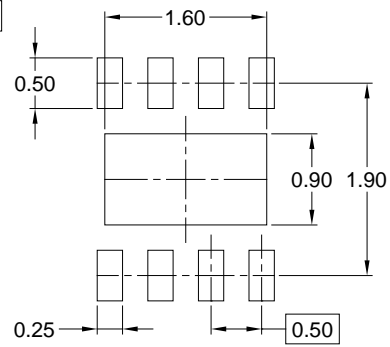
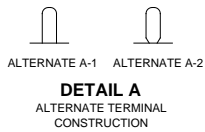
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

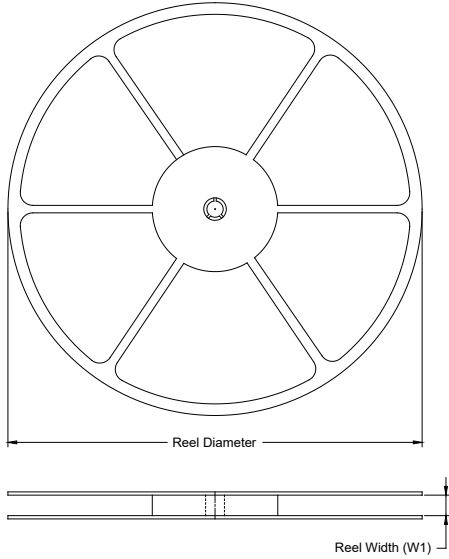
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	0.750	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	0.250	0.300
D	1.900	2.000	2.100
D1	1.450	1.600	1.700
E	1.900	2.000	2.100
E1	0.750	0.900	1.000
k	0.150	0.250	0.350
e	0.450	0.500	0.550
L	0.200	0.300	0.400
eee	0.080		

NOTE: This drawing is subject to change without notice.

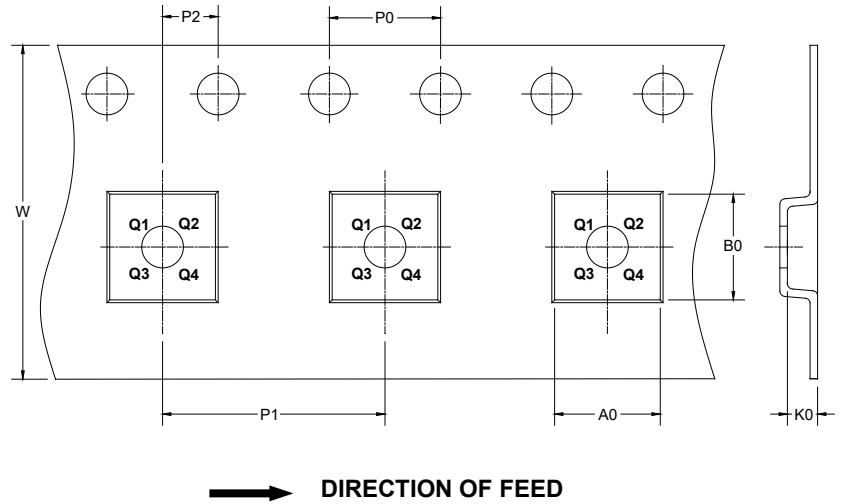
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-8AL	7"	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

000001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002