SGM2528
5A, 12V Electronic Fuse (eFuse) with Thermal Shutdown

GENERAL DESCRIPTION

The SGM2528 is a compact electronic fuse (eFuse) with a complete set of protection functions. The wide operating voltage range is specifically designed for many popular DC buses. The SGM2528 provides excellent accuracy, making it very suitable for many system protection applications.

It provides accurate over-voltage (OV) and under-voltage lockout (UVLO) protections, which ensure tight supervision of bus voltages and eliminate the need for supervisor circuits. The over-voltage (OV) protection will clamp the eFuse output at a fixed level during input voltage surges. During the input voltage transient, the internal FET remains on, which allows the load to continue to operate. If the transient duration remains long, the accumulated heat will cause the eFuse thermal shutdown. Once in thermal shutdown, latch-off and auto-retry thermal options are available.

The SGM2528 is available in a Green TDFN-3×3-10L package.

FEATURES

- **Wide Input Voltage Range from 9V to 18V with Surge up to 30V**
- **Extremely Low $R_{DS(ON)}$ for the Integrated Protection Switch: 26mΩ (TYP)**
- **3-State ENABLE/FAULT Pin, Bidirectional Interface**
- **Programmable Soft-Start Time**
- **Programmable Current Limit up to 5A**
- **Thermal Shutdown Options:**
  - **SGM2528A: Thermal Latch-Off with V_{CLAMP}**
  - **SGM2528B: Thermal Auto-Retry with V_{CLAMP}**
  - **SGM2528C: Thermal Latch-Off without V_{CLAMP}**
- **Fault Output for Thermal Shutdown**
- **Accurate Under-Voltage Lockout**
- **Accurate Over-Voltage Clamp (SGM2528A and SGM2528B)**
- **Available in a Green TDFN-3×3-10L Package**

APPLICATIONS

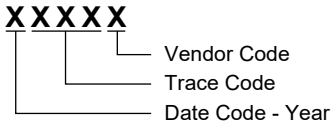
Hard Drives
PCIE SSD
Motherboard Power Management

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM2528A	TDFN-3×3-10L	-40℃ to +125℃	SGM2528AXTD10G/TR	SGM 2528AD XXXXX	Tape and Reel, 4000
SGM2528B	TDFN-3×3-10L	-40℃ to +125℃	SGM2528BXTD10G/TR	SGM 2528BD XXXXX	Tape and Reel, 4000
SGM2528C	TDFN-3×3-10L	-40℃ to +125℃	SGM2528CXTD10G/TR	SGM 2528CD XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Operating Input Voltage Range (V_{CC} to GND) (1)
- Steady-State ..... -0.3V to 18V
- Transient (100ms) ..... -0.6V to 25V

V_{CC}, SOURCE, I_{LIMIT} to GND ..... -0.3V to 25V
dV/dt, ENABLE/FAULT to GND ..... -0.3V to 5.5V
Package Thermal Resistance
TDFN-3×3-10L, θ_{JA} ..... 90℃/W
TDFN-3×3-10L, θ_{JB} ..... 54℃/W
TDFN-3×3-10L, θ_{JC} ..... 52℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

NOTE: 1. Negative voltage will not damage device provided that the power dissipation is limited to the rated allowable power for the package.

RECOMMENDED OPERATING CONDITIONS

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

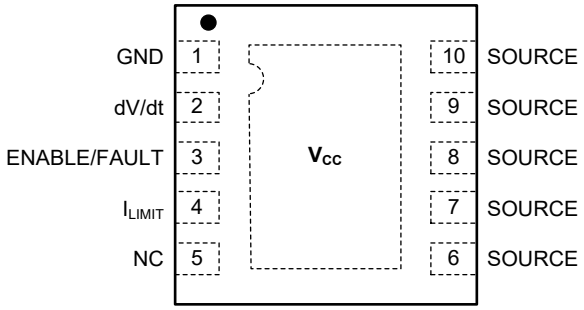
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-3×3-10L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	GND	Ground.
2	dV/dt	Internal dV/dt Circuit. The dV/dt pin is used to control the slew rate of the output voltage at turn-on. Leaving this pin open will allow the device to ramp up over a period of 2ms. An external capacitor can be connected to this pin to increase the ramp time.
3	ENABLE/ FAULT	Enable or Fault Pin. The ENABLE/FAULT pin is a 3-state, bidirectional interface. It can be used to enable or disable the output of the device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state to reflect its thermal shutdown status.
4	I_{LIMIT}	Current Limit Pin. A resistor between this pin and the SOURCE pin sets the overload and short-circuit current limit levels.
5	NC	No Connection.
6 - 10	SOURCE	Power Output Pins.
Exposed Pad	V_{CC}	Power Input Pin. Power input and supply voltage of the device.

ELECTRICAL CHARACTERISTICS

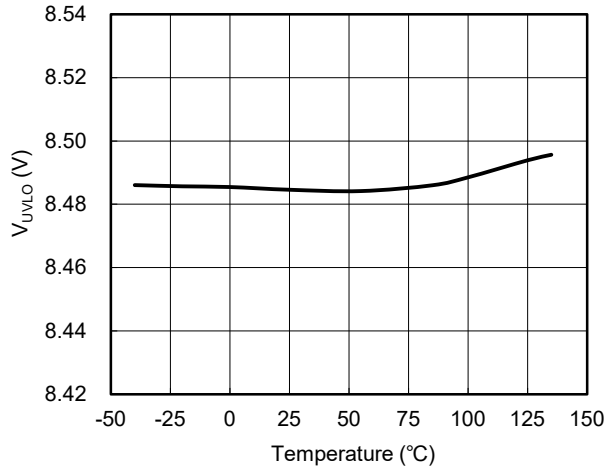
(T_J = +25℃, V_{CC} = 12V and dV/dt pin is open, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power FET						
Delay Time	t_{DLY}	Enabling of chip to I_D = 100mA with 1A resistive load		386		μs
Kelvin On-Resistance	$R_{DS(ON)}$	T_J = +25℃	21	26	31	mΩ
		T_J = +135℃		38		
Off-State Output Voltage	V_{OFF}	V_{CC} = 18V, V_{GS} = 0V, R_L = ∞		20	200	mV
Continuous Current	I_D			5		A
Thermal Latch						
Shutdown Temperature	T_{SD}			158		℃
Thermal Hysteresis	T_{HYST}	Decrease in die temperature for turn-on; does not apply to latch-off options.		22		℃
Under/Over-Voltage Protection						
Output Clamping Voltage	V_{CLAMP}	Over-voltage protection, V_{CC} = 18V	14.5	15	15.5	V
Under-Voltage Lockout	V_{UVLO}	Turn on, voltage going high	8.2	8.5	8.8	V
UVLO Hysteresis	V_{HYST}			0.83		V
Current Limit						
Kelvin Short-Circuit Current Limit	I_{LIM-SC}	R_{LIMIT} = 77Ω	0.5	0.95	1.4	A
Kelvin Overload Current Limit	I_{LIM-OL}	R_{LIMIT} = 77Ω		3		A
dV/dt Circuit						
Output Voltage Ramp Time	t_{SLEW}	Enable to V_{OUT} = 11.7V	1.3	2	2.8	ms
Maximum Capacitor Voltage	V_{MAX}				5.3	V
ENABLE/FAULT Pin						
Logic Level Low	V_{IN-LOW}	Output disabled	0.45	0.55	0.65	V
Logic Level Mid	V_{IN-MID}	Thermal fault, output disabled	1.35	1.45	1.55	V
Logic Level High	$V_{IN-HIGH}$	Output enabled	2.5	2.62	2.75	V
High State Maximum Voltage	V_{IN-MAX}		4.9	5.1	5.3	V
Logic Low Sink Current	I_{IN-LOW}	V_{ENABLE} = 0V		-15	-22	μA
Power Supply						
Quiescent Current	I_Q	Operating		110	140	μA
		Shutdown		48		

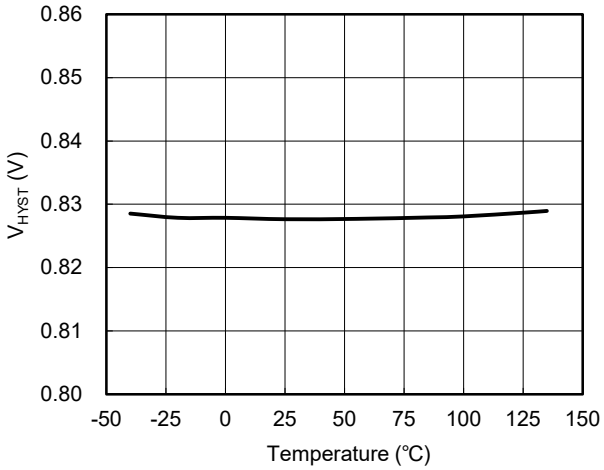
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, unless otherwise noted.

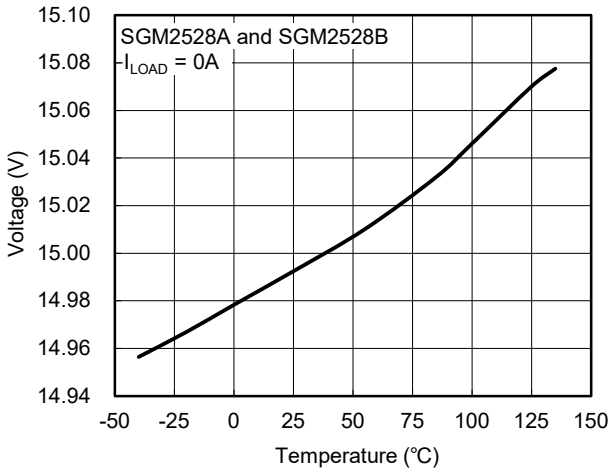
UVLO Turn-On Voltage vs. Temperature



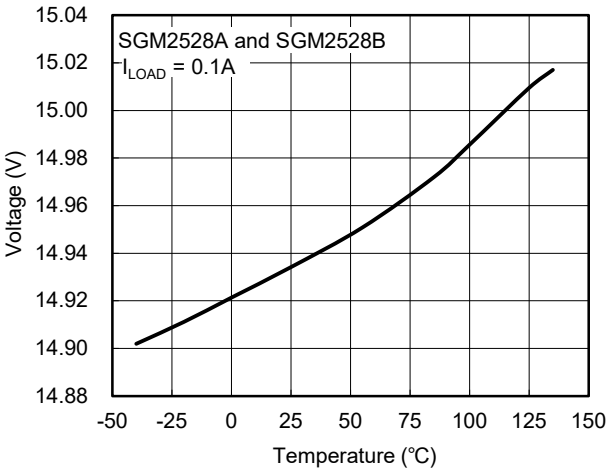
UVLO Hysteresis vs. Temperature



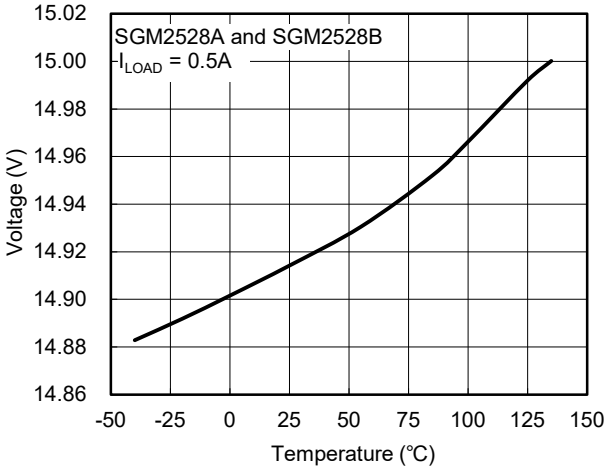
Output Clamping Voltage vs. Temperature



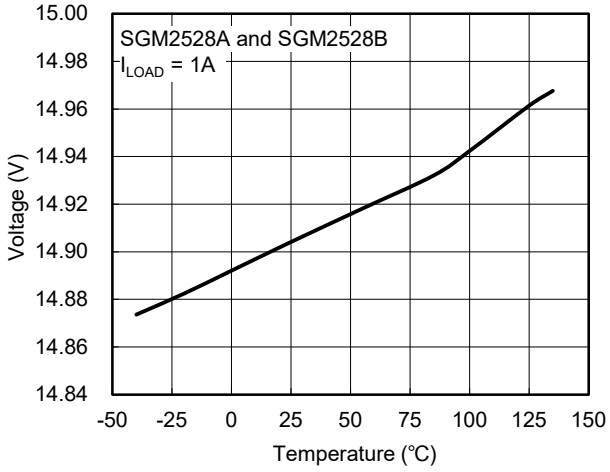
Output Clamping Voltage vs. Temperature



Output Clamping Voltage vs. Temperature



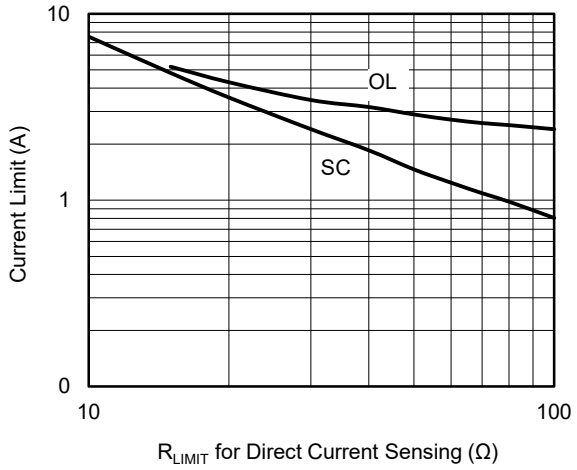
Output Clamping Voltage vs. Temperature



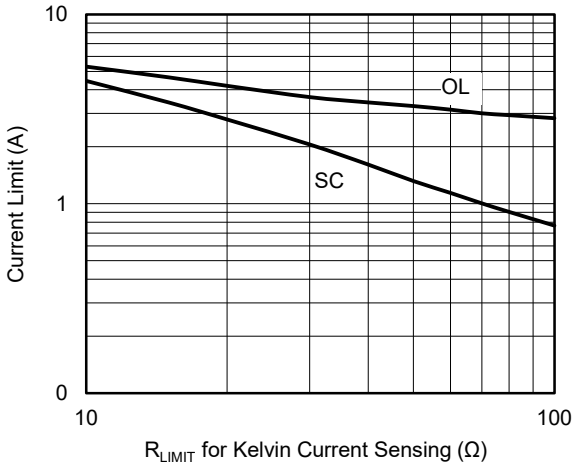
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

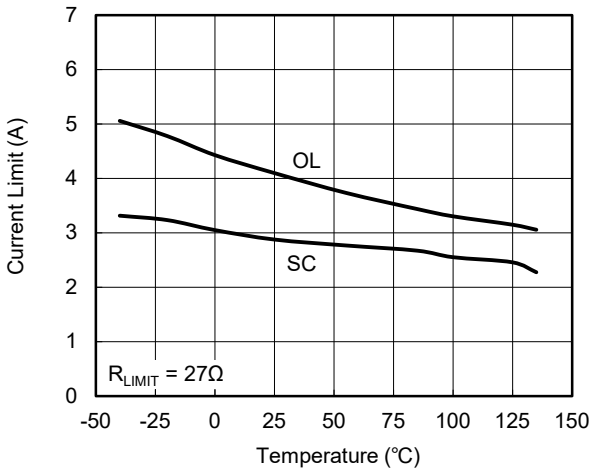
Current Limit vs. R_{LIMIT} for Direct Current Sensing



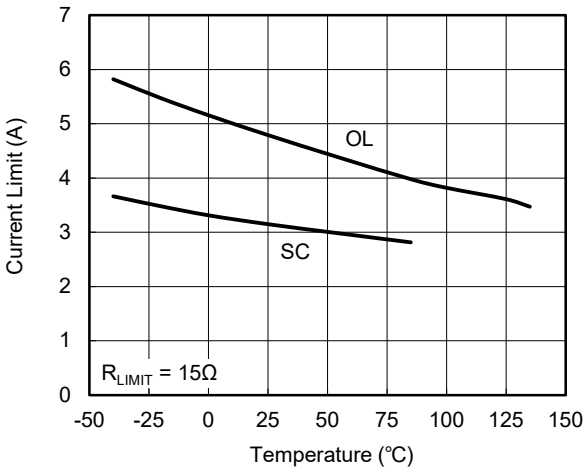
Current Limit vs. R_{LIMIT} for Kelvin Current Sensing



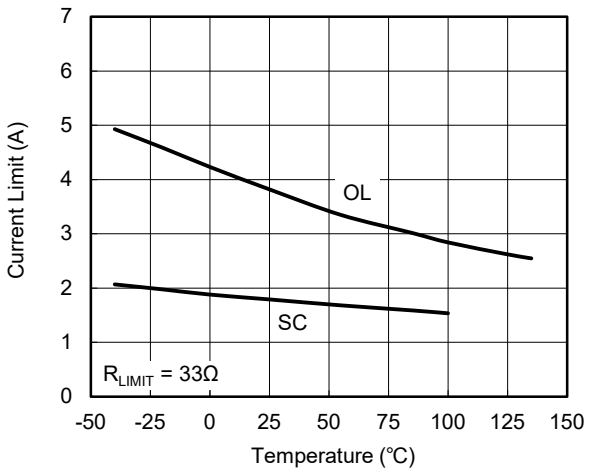
Direct Current Sensing Levels vs. Temperature



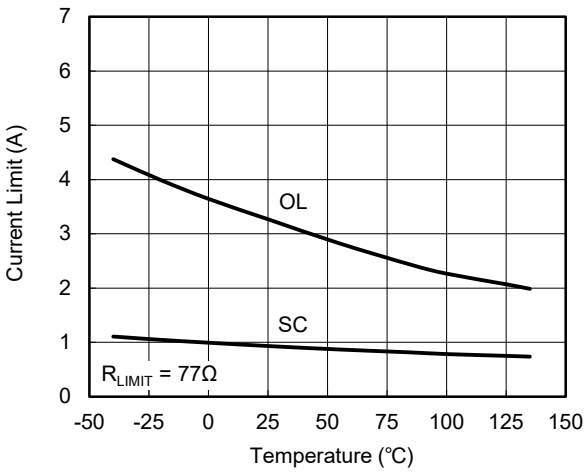
Kelvin Current Sensing Levels vs. Temperature



Kelvin Current Sensing Levels vs. Temperature



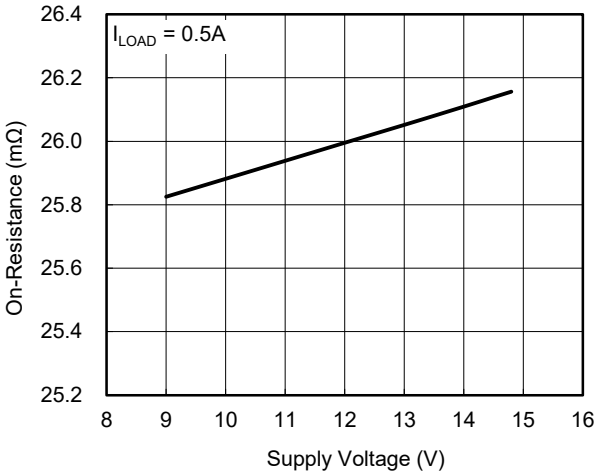
Kelvin Current Sensing Levels vs. Temperature



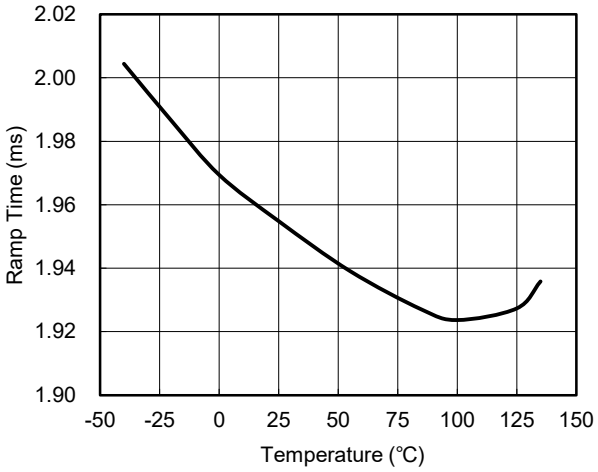
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_J = +25℃, unless otherwise noted.

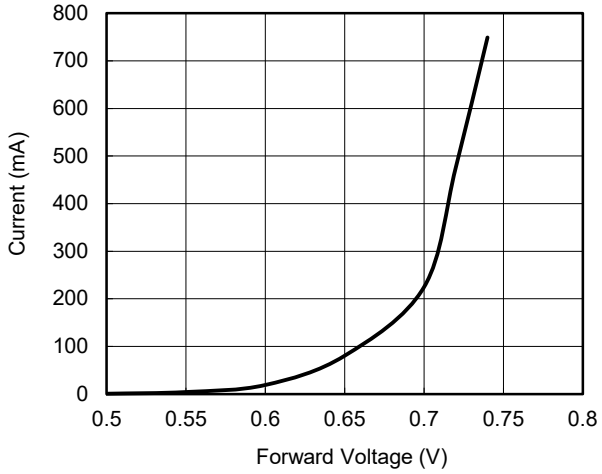
On-Resistance vs. Supply Voltage



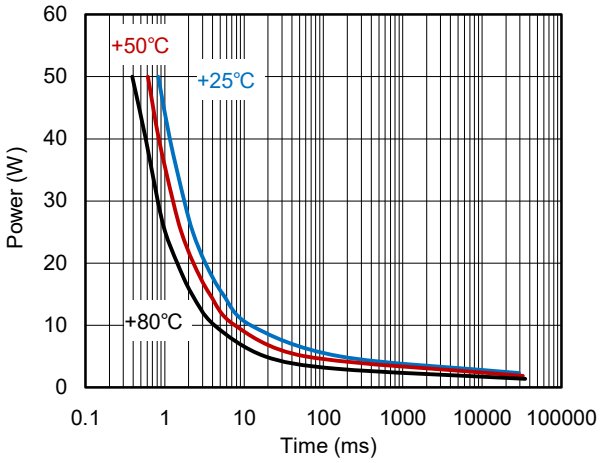
Output Voltage dV/dt Rate vs. Temperature



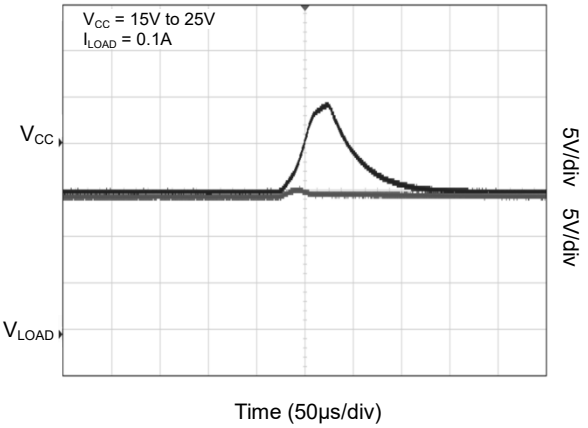
Body Diode Forward Characteristics



Power Dissipation vs. Thermal Trip Time



Input Transient Response



TYPICAL APPLICATION CIRCUITS

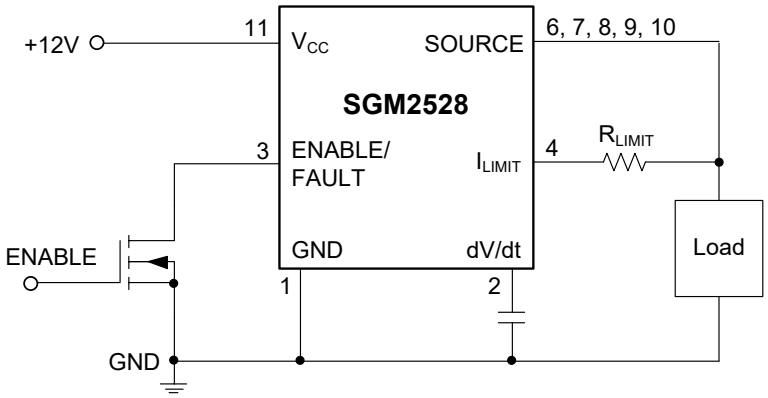


Figure 1. Application Circuit with Direct Current Sensing

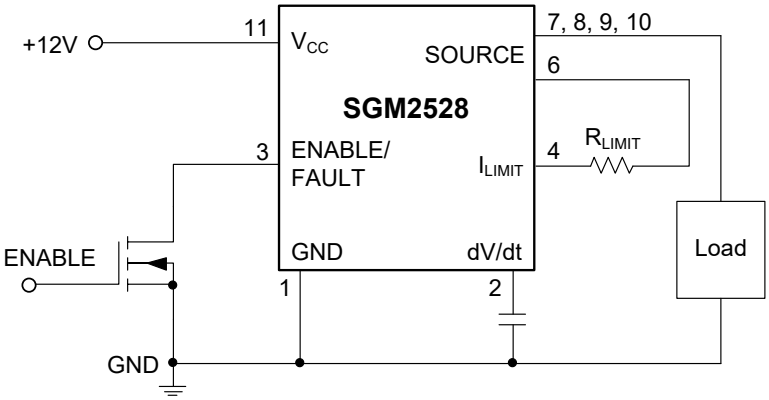


Figure 2. Application Circuit with Kelvin Current Sensing

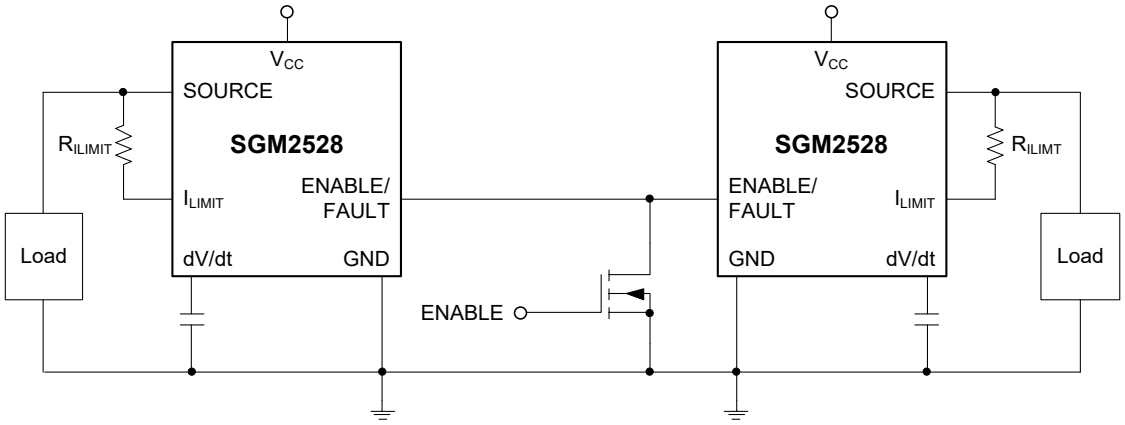
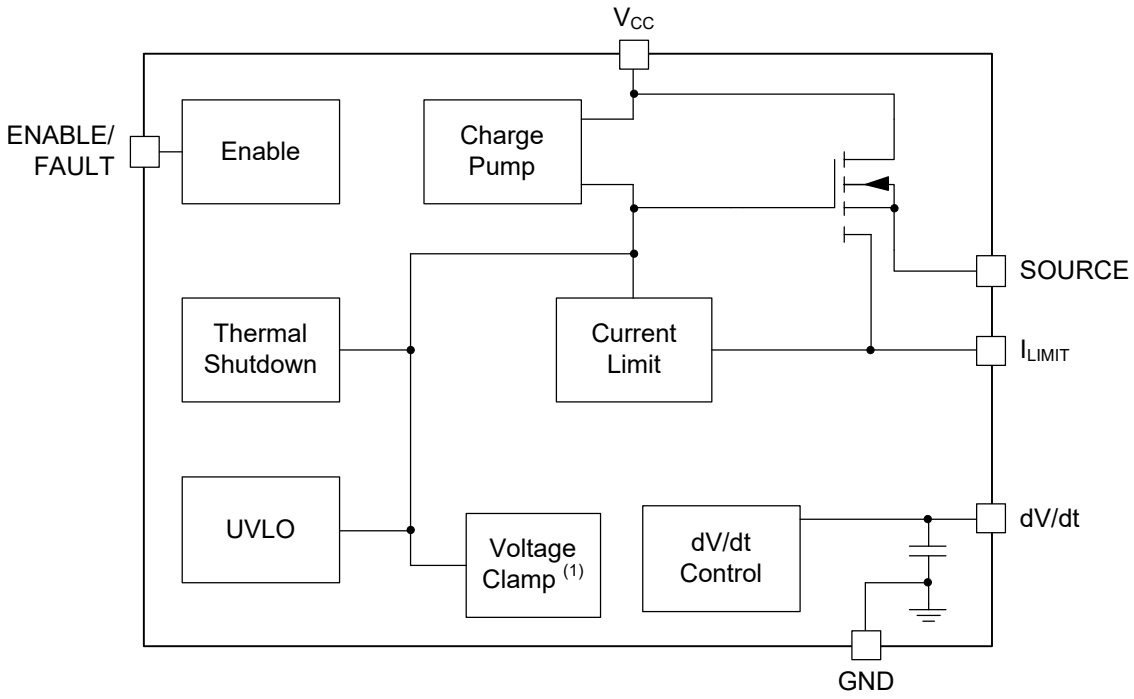


Figure 3. Common Thermal Shutdown

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. SGM2528A and SGM2528B versions.

Figure 4. Block Diagram

APPLICATION INFORMATION

Basic Operation

This device is a smart eFuse with enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 9V to 18V.

For hot plug boards, the device provides inrush current control and programmable output ramp rate. The SGM2528 integrates over-current and short-circuit protections. The precision over-current limit helps minimize over design of the input power supply; the short-circuit protection with fast response isolates the load from input immediately when the short circuit is detected. The device provides precision monitoring of bus voltage for brown-out and over-voltage conditions and asserts fault for downstream system. The SGM2528 is designed to protect systems such as hard disks, PCIE SSDs and motherboard systems.

This device will apply the input voltage to the load based on the restrictions of the controlling circuits. The dV/dt of the output voltage is controlled by the internal dV/dt circuit. The output voltage will ramp up in 2ms, unless additional capacitor is added to the dV/dt pin to slow down the ramp-up rate.

The device will remain on unless the temperature exceeds the factory-set shutdown threshold. The current limit circuit does not shut down the part, but limits the FET current to the level set by the I_{LIMIT} pin. The input over-voltage clamp also does not shut down the part, but limits the output voltage to 15V when the input exceeds that level.

Current Limit

The current limit circuit uses the current mirror structure to control the peak current in the device. The current mirror circuit allows a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sensing resistor and making the sensing resistor inexpensive.

APPLICATION INFORMATION (continued)

The current limit circuit has two limiting values: one is for overload events which are defined as the mode of operation in which the gate voltage is high and the FET is fully turned on; the other is for short-circuit operations when the device is actively limiting the current and the gate voltage is at an intermediate level.

There are two methods to bias the I_{LIMIT} pin with a sensing resistor (R_{LIMIT}). They are shown in Figure 1 and Figure 2.

For the direct current sensing method, the sensing resistor is connected between the I_{LIMIT} pin and the load. This method includes the bond wire resistance in the current limit circuit. This resistance has an impact on the current limit levels for a given resistor and may vary slightly depending on the impedance between the sensing resistor and the SOURCE pins. As all five SOURCE pins are connected in parallel, the on-resistance of the device will be slightly lower, and therefore the effective bond wire resistance is one fifth of the resistance for any given pin.

The other method is Kelvin current sensing. This method uses one of the SOURCE pins as the connection for the current sensing resistor. The circuit senses the voltage on the die, so any bond wire resistance and external impedance on the board have no effect on the current limit levels. With this method, the on-resistance is slightly increased relative to the direct sensing method since only four of the SOURCE pins are used for power.

Over-Voltage Clamp (SGM2528A and SGM2528B)

The over-voltage clamp circuit monitors the output voltage. If the input voltage exceeds 15V, the main integrated FET is regulated to limit the output voltage. This is intended to allow transient operation while protecting the load. If the over-voltage event lasts for a long time, the power consumption of the main FET may overheat the device, then triggering the thermal protection circuit which would shut down the device.

Under-Voltage Lockout

The under-voltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage is below the specified level, the output switch will be turned off.

dV/dt Circuit

The SGM2528 is designed to control the inrush current during hot plugging. This limits the voltage sag on the backplane power supply voltage and prevents unintended resets of the system power supply. The dV/dt circuit brings the output voltage up at a controlled rate regardless of the load impedance characteristics. The internal circuit generates a linear ramp and forces the output voltage to follow the ramp and scale factor.

If the dV/dt pin is left open, the output voltage ramps up in approximately 2ms. By connecting an external capacitor from this pin to ground, the user can get a longer output ramp-up time. There is an internal current source of approximately 100nA at the dV/dt pin. Since the current level is very low, the user should use a ceramic capacitor or a low leakage capacitor. Aluminum electrolytic capacitors are not recommended.

The ramp-up time of output voltage can be determined by the following equation:

$$t_{0\text{-}12} = 25.5e6\ (5pF + C_{EXT}) \quad (1)$$

$$C_{EXT} = \frac{t_{0\text{-}12}}{25.5e6} - 5pF \quad (2)$$

where:
C_{EXT} is in Farads.
t is in seconds.

Once the unit shuts down due to a fault, disable or recycling of input power, the timing capacitor will be discharged and the output voltage will ramp from 0V at turn-on.

APPLICATION INFORMATION (continued)

Enable/Fault

The ENABLE/FAULT is a multifunctional, bidirectional pin. It can control the output of the device as well as indicate the device thermal shutdown status. When this pin is low, the output of the eFuse will be turned off. When this pin is high, the output of the eFuse will be turned on.

It is recommended that an open-drain or open-collector circuit be connected to this pin. Due to its 3-state operation, it should not be connected to any type of circuit with pull-up structure.

If the chip is shut down when the die temperature reaches its thermal limit, the ENABLE/FAULT pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate whether a thermal shutdown has occurred. If this pin is tied to another device in this family, a thermal shutdown of one device will cause both devices to disable their outputs.

For the latch-off thermal devices, the outputs will be enabled after the ENABLE/FAULT pin has been pulled to ground with an external switch and then allowed to go high, or after the input power has been recycled. For the auto-retry devices, both devices will restart as soon as the die temperature of the device in shutdown has been reduced to the lower thermal limit threshold.

Thermal Protection

The SGM2528 includes an internal temperature sensing circuit that senses the temperature on the die of the power FET. If the temperature reaches +158℃, the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the ENABLE/FAULT pin. Power will automatically be reapplied to the load for auto-retry devices once the die temperature has been reduced by +22℃.

The thermal limit has been set high intentionally so that the trip time will be increased during high power transient events. It is not recommended to operate this device above +125℃ for extended periods of time.

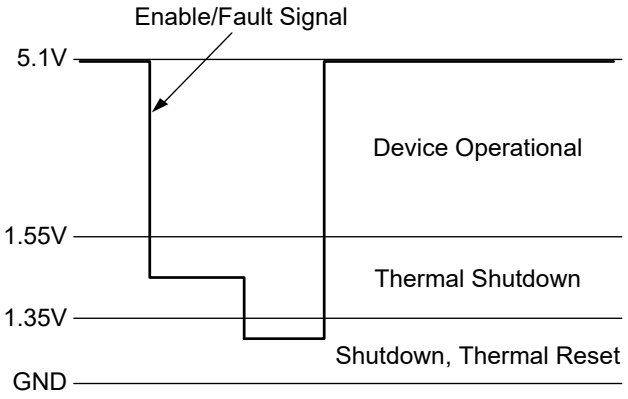


Figure 5. Enable/Fault Signal Levels

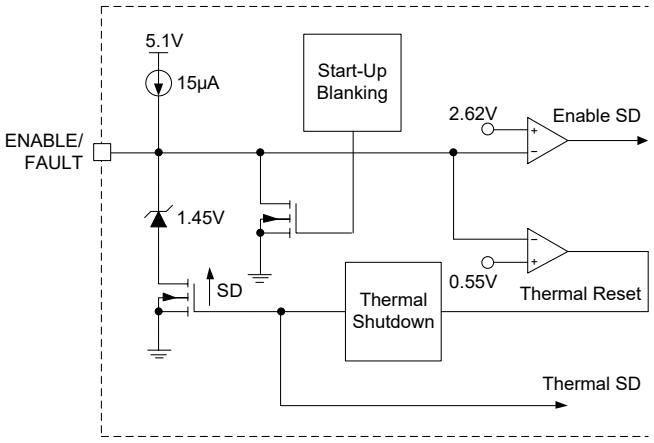


Figure 6. Enable/Fault Simplified Circuit

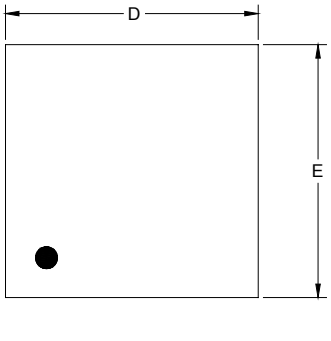
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

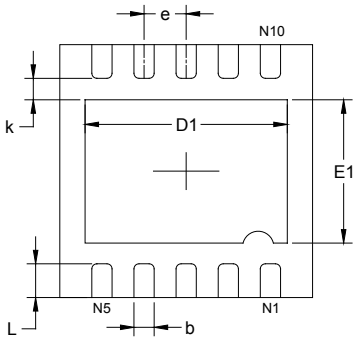
Changes from Original (JULY 2020) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

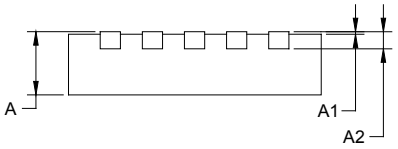
TDFN-3×3-10L



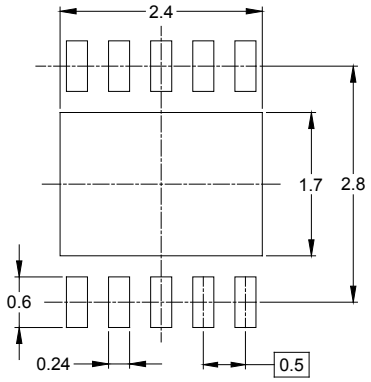
TOP VIEW



BOTTOM VIEW



SIDE VIEW

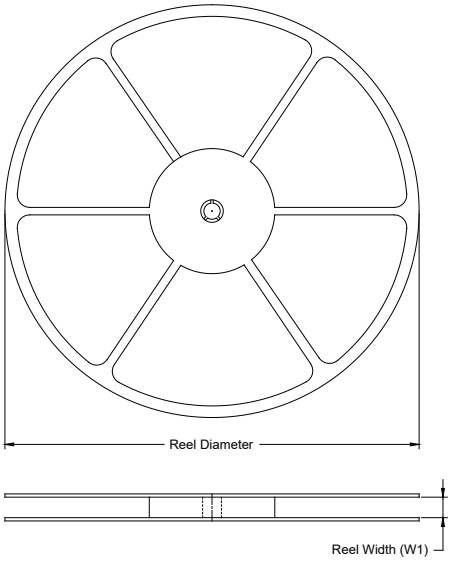


RECOMMENDED LAND PATTERN (Unit: mm)

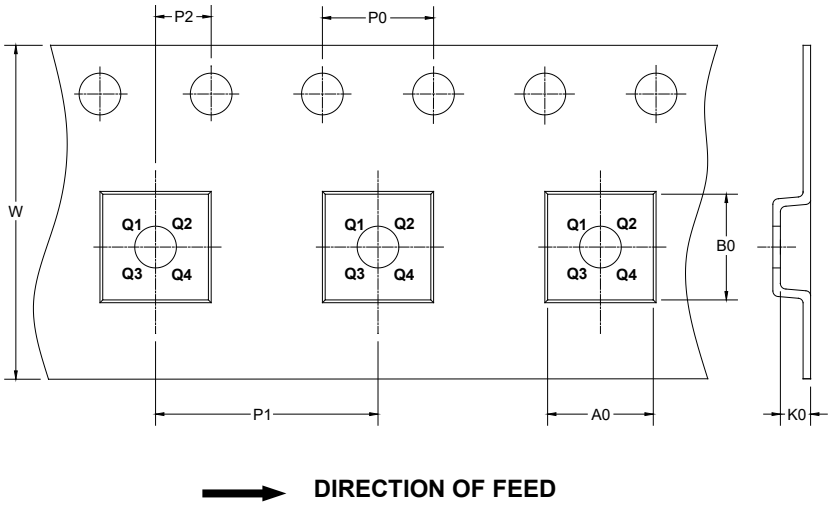
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



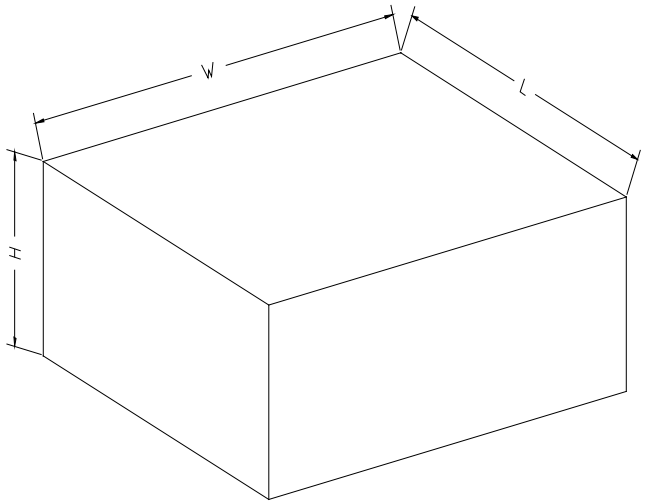
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-10L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002