

# 74LVC00A

## Quad 2-input NAND gate

Rev. 9 — 17 September 2021

Product data sheet

## 1. General description

The 74LVC00A is a quad 2-input NAND gate. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

## 2. Features and benefits

- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

| Type number | Package           |          |  | Version  |
|-------------|-------------------|----------|--|----------|
|             | Temperature range | Name     | Description  |          |
| 74LVC00AD   | -40 °C to +125 °C | SO14     | plastic small outline package; 14 leads;<br>body width 3.9 mm  | SOT108-1 |
| 74LVC00APW  | -40 °C to +125 °C | TSSOP14  | plastic thin shrink small outline package; 14 leads;<br>body width 4.4 mm  | SOT402-1 |
| 74LVC00ABQ  | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced<br>very thin quad flat package; no leads; 14 terminals;<br>body 2.5 × 3 × 0.85 mm | SOT762-1 |

### 4. Functional diagram

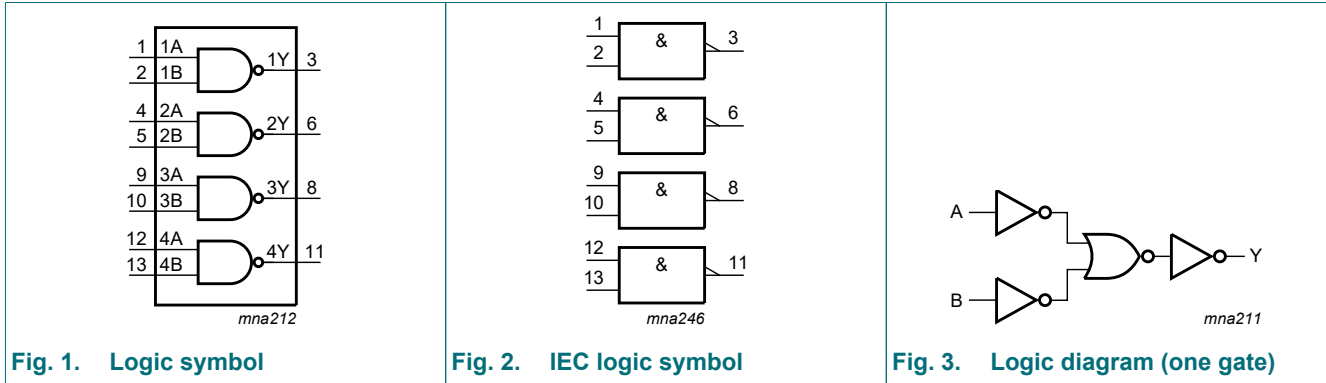


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Logic diagram (one gate)

### 5. Pinning information

#### 5.1. Pinning

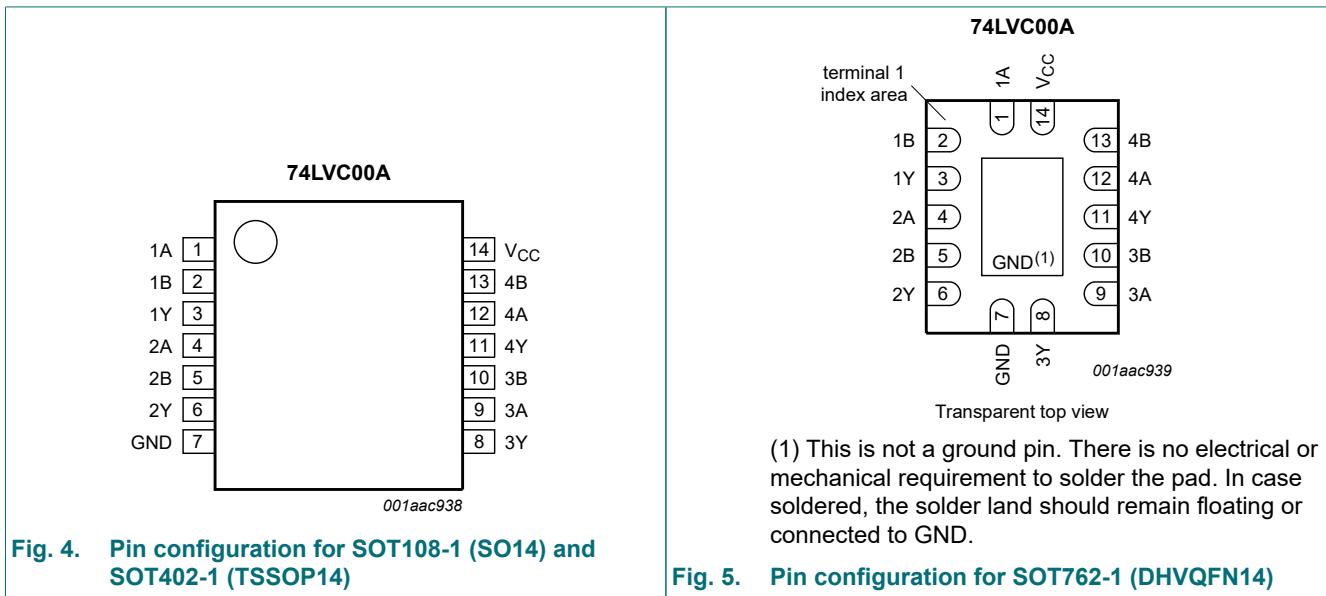


Fig. 4. Pin configuration for SOT108-1 (SO14) and SOT402-1 (TSSOP14)

Fig. 5. Pin configuration for SOT762-1 (DHVQFN14)

#### 5.2. Pin description

Table 2. Pin description

| Symbol          | Pin          | Description    |
|-----------------|--------------|----------------|
| 1A to 4A        | 1, 4, 9, 12  | data input     |
| 1B to 4B        | 2, 5, 10, 13 | data input     |
| 1Y to 4Y        | 3, 6, 8, 11  | data output    |
| GND             | 7            | ground (0 V)   |
| V <sub>CC</sub> | 14           | supply voltage |

## 6. Functional description

**Table 3. Function selection**

H = HIGH voltage level; L = LOW voltage level; X = don't care

| Input |    | Output |
|-------|----|--------|
| nA    | nB | nY     |
| L     | X  | H      |
| X     | L  | H      |
| H     | H  | L      |

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol    | Parameter               | Conditions                      | Min      | Max            | Unit |
|-----------|-------------------------|---------------------------------|----------|----------------|------|
| $V_{CC}$  | supply voltage          |                                 | -0.5     | +6.5           | V    |
| $I_{IK}$  | input clamping current  | $V_I < 0$ V                     | -50      | -              | mA   |
| $V_I$     | input voltage           |                                 | [1] -0.5 | +6.5           | V    |
| $I_{OK}$  | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V   | -        | ±50            | mA   |
| $V_O$     | output voltage          | output in HIGH or LOW-state     | [2] -0.5 | $V_{CC} + 0.5$ | V    |
| $I_O$     | output current          | $V_O = 0$ V to $V_{CC}$         | -        | ±50            | mA   |
| $I_{CC}$  | supply current          |                                 | -        | 100            | mA   |
| $I_{GND}$ | ground current          |                                 | -100     | -              | mA   |
| $P_{tot}$ | total power dissipation | $T_{amb} = -40$ °C to $+125$ °C | [3] -    | 500            | mW   |
| $T_{stg}$ | storage temperature     |                                 | -65      | +150           | °C   |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package:  $P_{tot}$  derates linearly with 9.6 mW/K above 98 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol              | Parameter                           | Conditions                   | Min  | Typ | Max      | Unit |
|---------------------|-------------------------------------|------------------------------|------|-----|----------|------|
| $V_{CC}$            | supply voltage                      |                              | 1.65 | -   | 3.6      | V    |
|                     |                                     | functional                   | 1.2  | -   | -        | V    |
| $V_I$               | input voltage                       |                              | 0    | -   | 5.5      | V    |
| $V_O$               | output voltage                      | output HIGH or LOW state     | 0    | -   | $V_{CC}$ | V    |
| $T_{amb}$           | ambient temperature                 |                              | -40  | -   | +125     | °C   |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to $2.7$ V | 0    | -   | 20       | ns/V |
|                     |                                     | $V_{CC} = 2.7$ V to $3.6$ V  | 0    | -   | 10       | ns/V |

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol           | Parameter                 | Conditions  | -40 °C to +85 °C      |        |                     | -40 °C to +125 °C     |                     | Unit |
|------------------|---------------------------|---|-----------------------|--------|---------------------|-----------------------|---------------------|------|
|                  |                           |   | Min                   | Typ[1] | Max                 | Min                   | Max                 |      |
| V <sub>IH</sub>  | HIGH-level input voltage  | V <sub>CC</sub> = 1.2 V   | 1.08                  | -      | -                   | 1.08                  | -                   | V    |
|                  |                           | V <sub>CC</sub> = 1.65 V to 1.95 V  | 0.65V <sub>CC</sub>   | -      | -                   | 0.65V <sub>CC</sub>   | -                   | V    |
|                  |                           | V <sub>CC</sub> = 2.3 V to 2.7 V  | 1.7                   | -      | -                   | 1.7                   | -                   | V    |
|                  |                           | V <sub>CC</sub> = 2.7 V to 3.6 V  | 2.0                   | -      | -                   | 2.0                   | -                   | V    |
| V <sub>IL</sub>  | LOW-level input voltage   | V <sub>CC</sub> = 1.2 V   | -                     | -      | 0.12                | -                     | 0.12                | V    |
|                  |                           | V <sub>CC</sub> = 1.65 V to 1.95 V  | -                     | -      | 0.35V <sub>CC</sub> | -                     | 0.35V <sub>CC</sub> | V    |
|                  |                           | V <sub>CC</sub> = 2.3 V to 2.7 V  | -                     | -      | 0.7                 | -                     | 0.7                 | V    |
|                  |                           | V <sub>CC</sub> = 2.7 V to 3.6 V  | -                     | -      | 0.8                 | -                     | 0.8                 | V    |
| V <sub>OH</sub>  | HIGH-level output voltage | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>   |                       |        |                     |                       |                     |      |
|                  |                           | I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V   | V <sub>CC</sub> - 0.2 | -      | -                   | V <sub>CC</sub> - 0.3 | -                   | V    |
|                  |                           | I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V  | 1.2                   | -      | -                   | 1.05                  | -                   | V    |
|                  |                           | I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V   | 1.8                   | -      | -                   | 1.65                  | -                   | V    |
|                  |                           | I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V  | 2.2                   | -      | -                   | 2.05                  | -                   | V    |
|                  |                           | I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V  | 2.4                   | -      | -                   | 2.25                  | -                   | V    |
| V <sub>OL</sub>  | LOW-level output voltage  | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>   |                       |        |                     |                       |                     |      |
|                  |                           | I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V  | -                     | -      | 0.2                 | -                     | 0.3                 | V    |
|                  |                           | I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V   | -                     | -      | 0.45                | -                     | 0.65                | V    |
|                  |                           | I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V  | -                     | -      | 0.6                 | -                     | 0.8                 | V    |
|                  |                           | I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V   | -                     | -      | 0.4                 | -                     | 0.6                 | V    |
|                  |                           | I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V   | -                     | -      | 0.55                | -                     | 0.8                 | V    |
| I <sub>I</sub>   | input leakage current     | V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND  | -                     | ±0.1   | ±5                  | -                     | ±20                 | μA   |
| I <sub>CC</sub>  | supply current            | V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A                          | -                     | 0.1    | 10                  | -                     | 40                  | μA   |
| ΔI <sub>CC</sub> | additional supply current | per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A | -                     | 5      | 500                 | -                     | 5000                | μA   |
| C <sub>I</sub>   | input capacitance         | V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>   | -                     | 4.0    | -                   | -                     | -                   | pF   |

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

| Symbol             | Parameter                     | Conditions  | -40 °C to +85 °C |        |     | -40 °C to +125 °C |     | Unit |
|--------------------|-------------------------------|---|------------------|--------|-----|-------------------|-----|------|
|                    |                               |   | Min              | Typ[1] | Max | Min               | Max |      |
| t <sub>pd</sub>    | propagation delay             | nA, nB to nY; see Fig. 6 [2]                          |                  |        |     |                   |     |      |
|                    |                               | V <sub>CC</sub> = 1.2 V                               | -                | 12     | -   | -                 | -   | ns   |
|                    |                               | V <sub>CC</sub> = 1.65 V to 1.95 V                    | 0.3              | 3.8    | 8.4 | 0.3               | 9.7 | ns   |
|                    |                               | V <sub>CC</sub> = 2.3 V to 2.7 V                      | 1.0              | 2.2    | 4.8 | 1.0               | 5.7 | ns   |
|                    |                               | V <sub>CC</sub> = 2.7 V                               | 1.0              | 2.3    | 5.1 | 1.0               | 5.9 | ns   |
|                    |                               | V <sub>CC</sub> = 3.0 V to 3.6 V                      | 0.5              | 2.0    | 4.3 | 0.5               | 5.1 | ns   |
| t <sub>sk(o)</sub> | output skew time              | V <sub>CC</sub> = 3.0 V to 3.6 V [3]                  | -                | -      | 1.0 | -                 | 1.5 | ns   |
| C <sub>PD</sub>    | power dissipation capacitance | per gate; V <sub>I</sub> = GND to V <sub>CC</sub> [4] |                  |        |     |                   |     |      |
|                    |                               | V <sub>CC</sub> = 1.65 V to 1.95 V                    | -                | 5.6    | -   | -                 | -   | pF   |
|                    |                               | V <sub>CC</sub> = 2.3 V to 2.7 V                      | -                | 8.9    | -   | -                 | -   | pF   |
|                    |                               | V <sub>CC</sub> = 3.0 V to 3.6 V                      | -                | 11.8   | -   | -                 | -   | pF   |

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

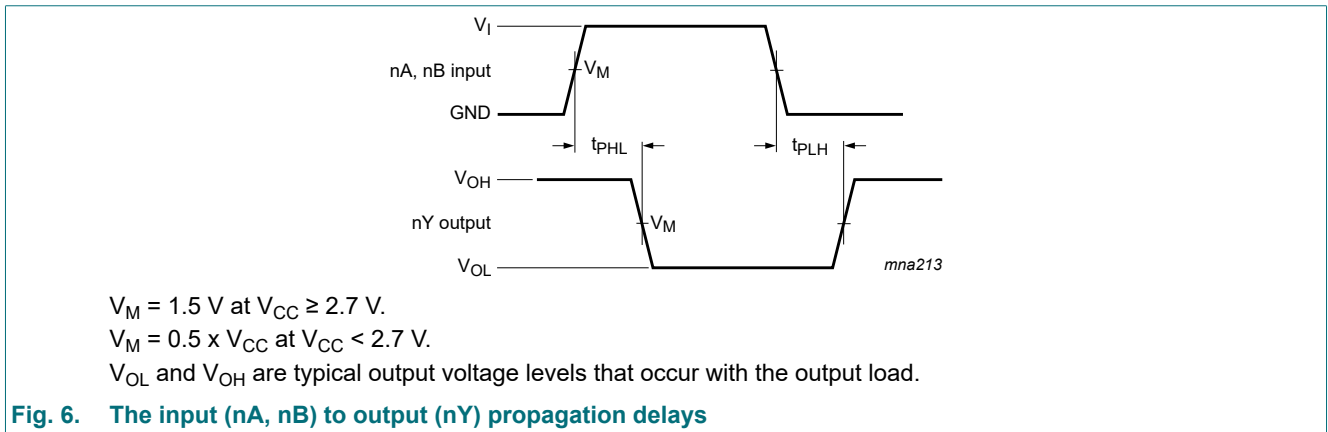
C<sub>L</sub> = output load capacitance in pF

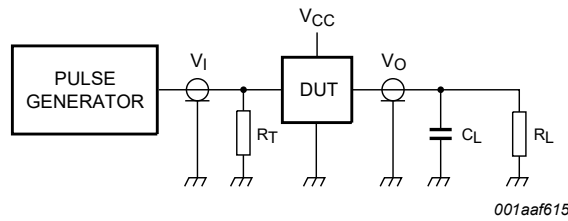
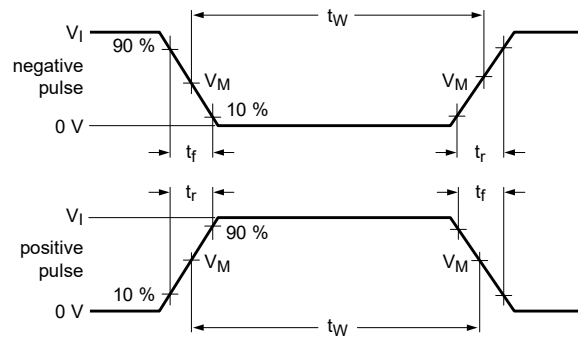
V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

### 10.1. Waveforms and test circuit





Test data is given in [Table 8](#). Definitions for test circuit:

$R_L$  = Load resistance

$C_L$  = Load capacitance including jig and probe capacitance

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator

**Fig. 7. Test circuit for measuring switching times**

**Table 8. Test data**

| Supply voltage   | Input    |               | Load  |              |
|------------------|----------|---------------|-------|--------------|
|                  | $V_I$    | $t_r, t_f$    | $C_L$ | $R_L$        |
| 1.2 V            | $V_{CC}$ | $\leq 2$ ns   | 30 pF | 1 k $\Omega$ |
| 1.65 V to 1.95 V | $V_{CC}$ | $\leq 2$ ns   | 30 pF | 1 k $\Omega$ |
| 2.3 V to 2.7 V   | $V_{CC}$ | $\leq 2$ ns   | 30 pF | 500 $\Omega$ |
| 2.7 V            | 2.7 V    | $\leq 2.5$ ns | 50 pF | 500 $\Omega$ |
| 3.0 V to 3.6 V   | 2.7 V    | $\leq 2.5$ ns | 50 pF | 500 $\Omega$ |

### 11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

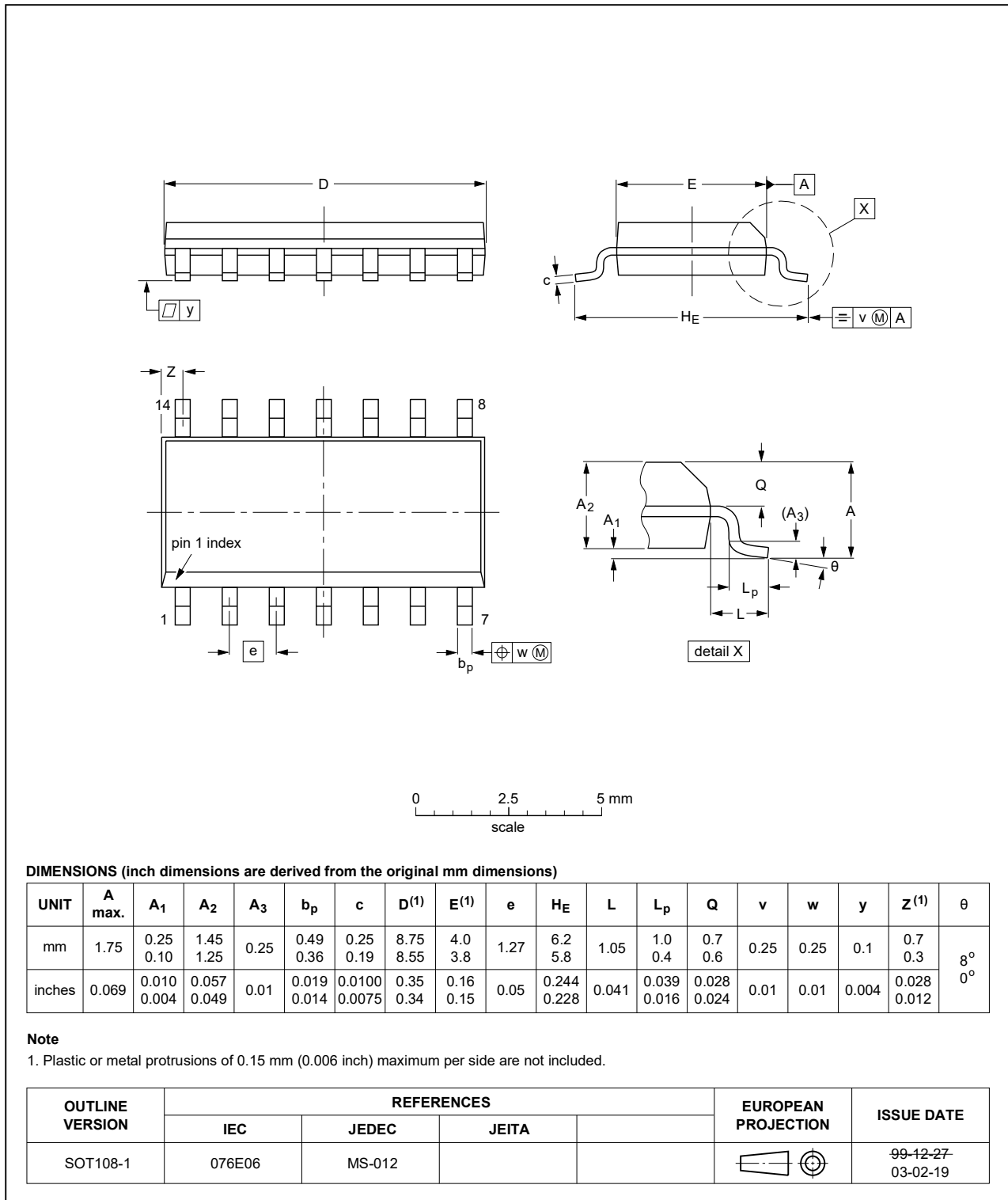


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

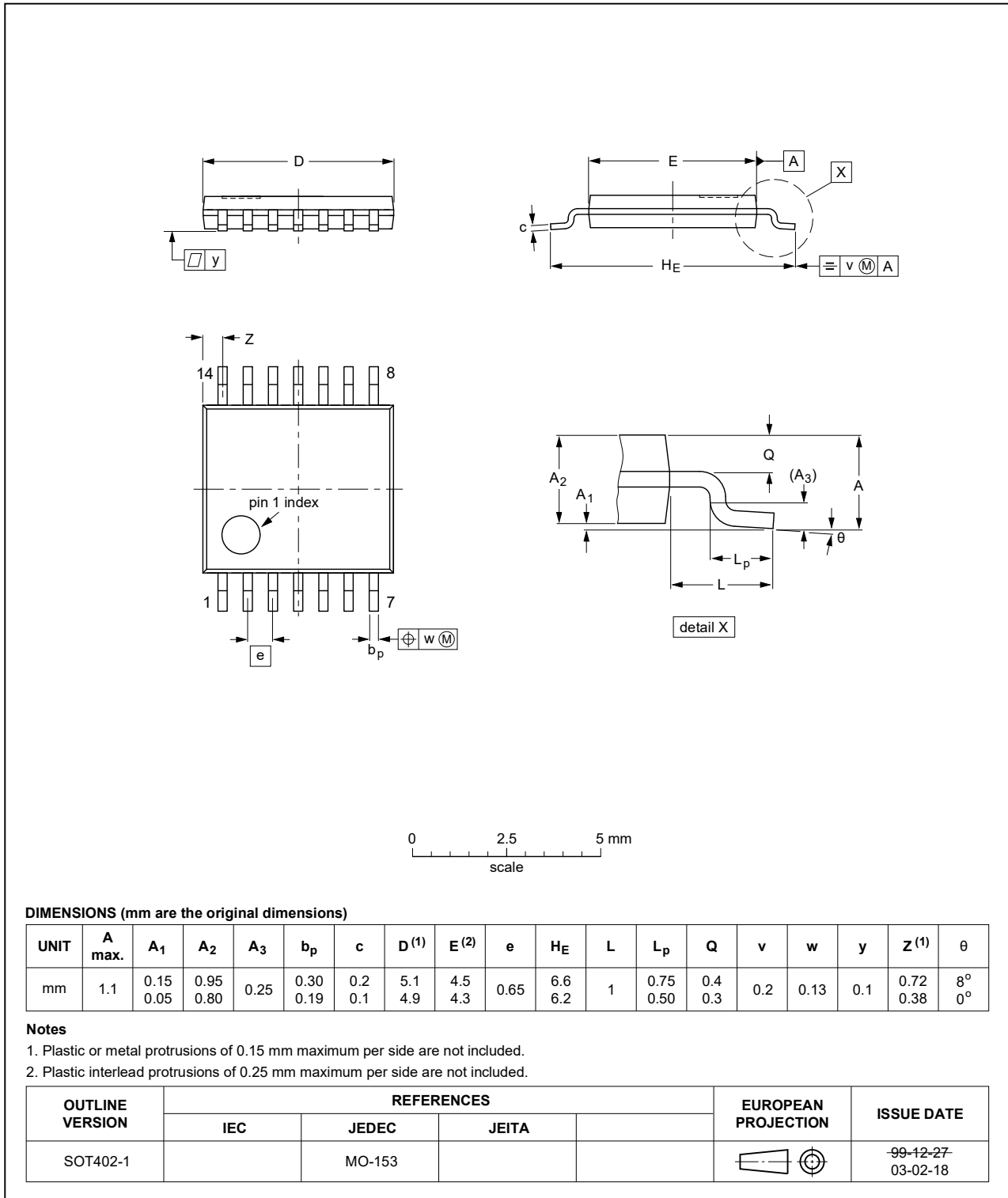


Fig. 9. Package outline SOT402-1 (TSSOP14)



DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

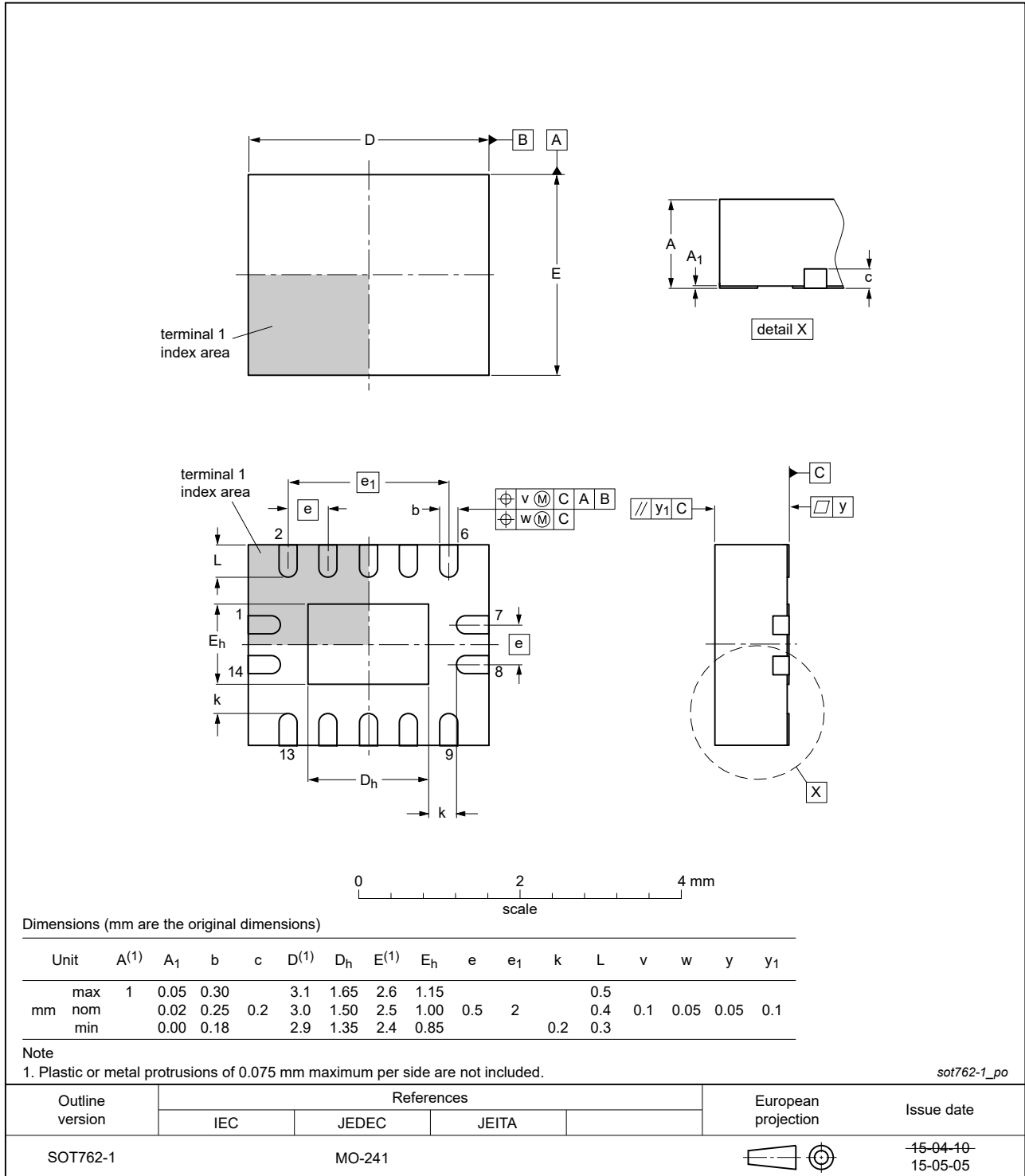


Fig. 10. Package outline SOT762-1 (DHVQFN14)

## 12. Abbreviations

Table 9. Abbreviations

| Acronym | Description                             |
|---------|---|
| CDM     | Charged Device Model                    |
| CMOS    | Complementary Metal Oxide Semiconductor |
| DUT     | Device Under Test                       |
| ESD     | ElectroStatic Discharge                 |
| HBM     | Human Body Model                        |
| MM      | Machine Model                           |
| TTL     | Transistor-Transistor Logic             |

## 13. Revision history

Table 10. Revision history

| Document ID    | Release date  | Data sheet status     | Change notice | Supersedes   |
|----------------|---|-----------------------|---------------|--------------|
| 74LVC00A v.9   | 20210917  | Product data sheet    | -             | 74LVC00A v.8 |
| Modifications: | <ul style="list-style-type: none"> <li>Type number 74LVC00ADB (SOT337-1/SSOP14) removed.</li> <li><a href="#">Section 1</a> updated.</li> </ul>   |                       |               |              |
| 74LVC00A v.8   | 20200824  | Product data sheet    | -             | 74LVC00A v.7 |
| Modifications: | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> <li>Package outline drawing of SOT762-1 (<a href="#">Fig. 10</a>) updated.</li> </ul> |                       |               |              |
| 74LVC00A v.7   | 20120425  | Product data sheet    | -             | 74LVC00A v.6 |
| Modifications: | <ul style="list-style-type: none"> <li><a href="#">Table 2</a>: Errata in pin description corrected.</li> </ul>   |                       |               |              |
| 74LVC00A v.6   | 20120106  | Product data sheet    | -             | 74LVC00A v.5 |
| Modifications: | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a> and <a href="#">Table 8</a>: values added for lower voltage ranges.</li> </ul>         |                       |               |              |
| 74LVC00A v.5   | 20030904  | Product specification | -             | 74LVC00A v.4 |
| 74LVC00A v.4   | 20030507  | Product specification | -             | 74LVC00A v.3 |
| 74LVC00A v.3   | 20020305  | Product specification | -             | 74LVC00A v.2 |
| 74LVC00A v.2   | 19980428  | Product specification | -             | 74LVC00A v.1 |
| 74LVC00A v.1   | 19970811  | Product specification | -             | -            |

## 14. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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