74AHCT244
Octal Buffer/Line Driver with 3-State Outputs

GENERAL DESCRIPTION

The 74AHCT244 is an octal buffer/line driver with non-inverting 3-state outputs, and it is designed for 4.5V to 5.5V V_{CC} operation.

The device can be used as two 4-bit buffers or one 8-bit buffer. The $1\overline{OE}$ and $2\overline{OE}$ are two output enable inputs, and each controls four of the 3-state outputs. When $n\overline{OE}$ is set high, the outputs are in high-impedance state. When $n\overline{OE}$ is set low, data transmits from the nAn inputs to the nYn outputs.

$n\overline{OE}$ should be connected to V_{CC} by using a pull-up resistor to ensure the high-impedance state in the period of power-up or power-down, and the minimum resistance depends on the current-sinking capability of the driver.

FEATURES

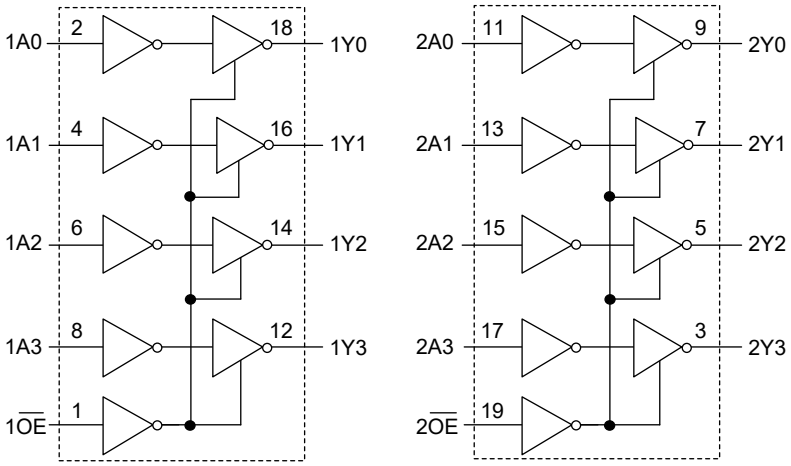
- **Supply Voltage Range: 4.5V to 5.5V**
- **Input Accept Voltages Higher than the Supply Voltage**
- **+8mA/-8mA Output Current**
- **3-State Buffers**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOIC-20 Package**

FUNCTION TABLE

CONTROL INPUT	INPUT	OUTPUT
$n\overline{OE}$	nAn	nYn
L	H	H
L	L	L
H	*X*	Z

H = High Voltage Level
L = Low Voltage Level
Z = High-Impedance State
X = Don't Care

LOGIC DIAGRAM

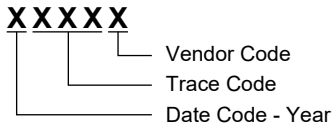


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74AHCT244	SOIC-20	-40℃ to +125℃	74AHCT244XS20G/TR	74AHCT244XS20 XXXXX	Tape and Reel, 1500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 7V
Input Voltage, V_I (2) ..... -0.5V to 7V
Output Voltage, V_O (2)
High-Impedance State ..... -0.5V to 7V
High-State or Low-State..... -0.5V to MIN (7V, V_{CC} + 0.5V)
Input Clamping Current, I_{IK} (V_I < 0V) .....-20mA
Output Clamping Current, I_{OK} (V_O > V_{CC} or V_O < 0V)
..... ±20mA
Output Current, I_O
High-State .....-25mA
Low-State..... 25mA
Supply Current, I_{CC} 75mA
Ground Current, I_{GND}.....-75mA
Junction Temperature (3) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Function Supply Voltage, V_{CC} .....4.5V to 5.5V
Output Voltage, V_O
High-Impedance State .....0V to 5.5V
High-State or Low-State..... 0V to V_{CC}
High-Level Output Current, I_{OH} .....-8mA
Low-Level Output Current, I_{OL}.....8mA
Input Transition Rise and Fall Rate, Δt/ΔV
V_{CC} = 4.5V to 5.5V ..... 10ns/V (MAX)
Operating Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

ESD SENSITIVITY CAUTION

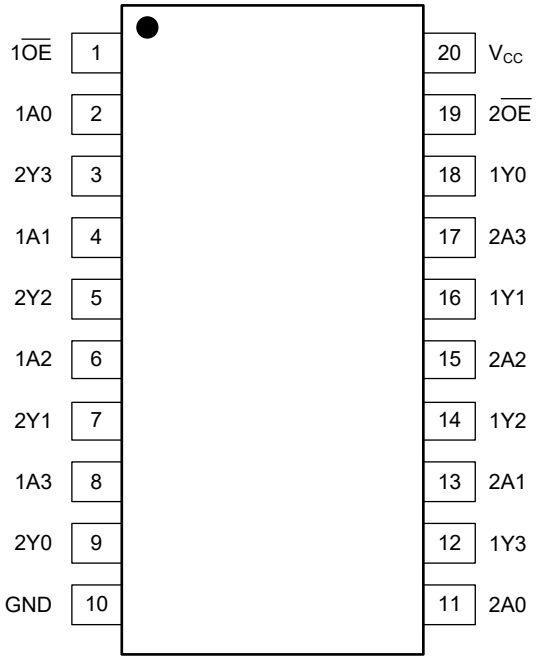
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SOIC-20

PIN DESCRIPTION

PINS	NAME	FUNCTION
1, 19	1$\overline{OE}$, 2$\overline{OE}$	Output Enable Inputs (Active Low).
2, 4, 6, 8	1A0, 1A1, 1A2, 1A3	Data Inputs.
18, 16, 14, 12	1Y0, 1Y1, 1Y2, 1Y3	Data Outputs.
10	GND	Ground.
11, 13, 15, 17	2A0, 2A1, 2A2, 2A3	Data Inputs.
9, 7, 5, 3	2Y0, 2Y1, 2Y2, 2Y3	Data Outputs.
20	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 4.5V to 5.5V		Full	2			V
Low-Level Input Voltage	V_{IL}	V_{CC} = 4.5V to 5.5V		Full			0.8	V
High-Level Output Voltage	V_{OH}	V_{CC} = 4.5V	I_{OH} = -50μA	Full	4.45	4.495		V
			I_{OH} = -8.0mA	Full	4	4.25		
Low-Level Output Voltage	V_{OL}	V_{CC} = 4.5V	I_{OL} = 50μA	Full		0.005	0.05	V
			I_{OL} = 8.0mA	Full		0.25	0.5	
Off-State Output Current	I_{OZ}	V_{CC} = 5.5V, V_O = V_{CC} or GND		Full		0.02	2	μA
Input Leakage Current	I_I	V_{CC} = 0V to 5.5V, V_I = 5.5V or GND		Full		0.02	2	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, V_I = V_{CC} or GND, I_O = 0A		Full		0.02	2	μA
Additional Supply Current	ΔI_{CC}	Per input pin at 3.4V, other pins at V_{CC} or GND, V_{CC} = 5.5V		Full		0.05	0.5	mA
Input Capacitance	C_I	V_{CC} = 5V, V_I = V_{CC} or GND		+25℃		7		pF
Output Capacitance	C_O	V_{CC} = 5V, V_O = V_{CC} or GND		+25℃		5		pF

DYNAMIC CHARACTERISTICS

(For test circuit see Figure 1. Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 5V ± 0.5V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay	t_{PLH}	nAn to nYn	C_L = 15pF	Full	0.5	3.5	8.5	ns
			C_L = 50pF	Full	1	4.5	9.5	
	t_{PHL}	nAn to nYn	C_L = 15pF	Full	1	5	8.5	
			C_L = 50pF	Full	1	5.5	9.5	
Enable Time	t_{PZH}	$n\overline{OE}$ to nYn	C_L = 15pF	Full	1	6	12	ns
			C_L = 50pF	Full	1	7	13	
	t_{PZL}	$n\overline{OE}$ to nYn	C_L = 15pF	Full	1	5.5	12	
			C_L = 50pF	Full	1	6.5	13	
Disable Time	t_{PHZ}	$n\overline{OE}$ to nYn	C_L = 15pF	Full	0.5	5	10	ns
			C_L = 50pF	Full	0.5	8	13	
	t_{PLZ}	$n\overline{OE}$ to nYn	C_L = 15pF	Full	0.5	4	10	
			C_L = 50pF	Full	0.5	7	13	
Power Dissipation Capacitance (2)	C_{PD}	No load, f = 1MHz		+25℃		13		pF

NOTES:

1. Specified by design and characterization, not production tested.
2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

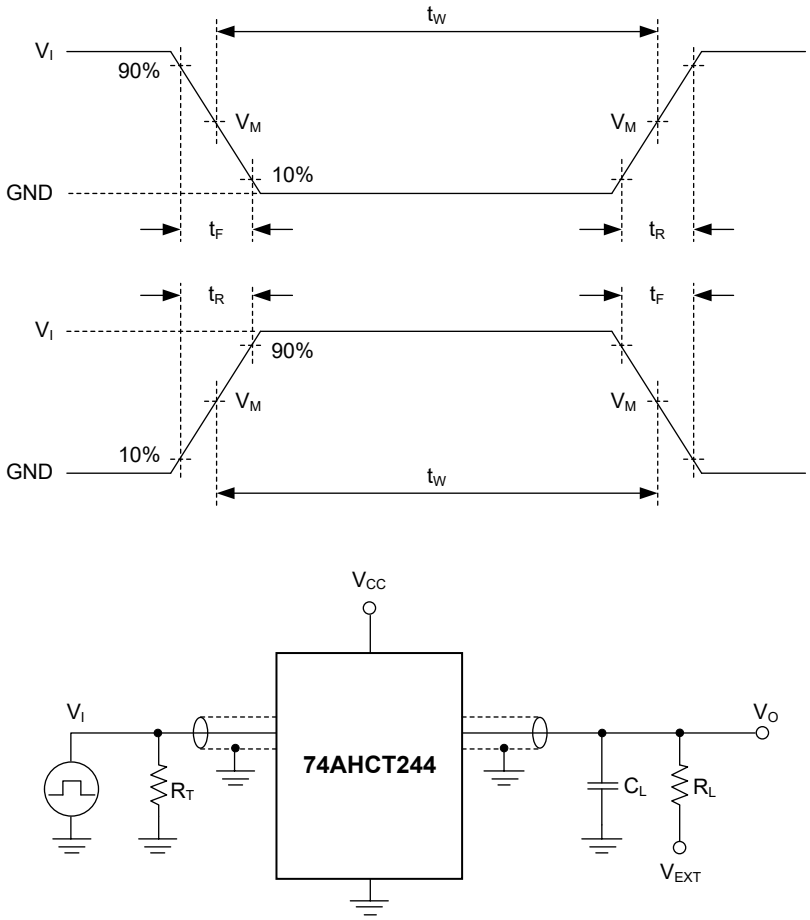
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

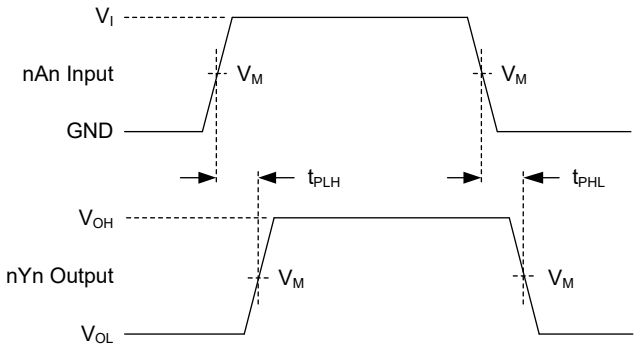
V_{EXT}: External voltage used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

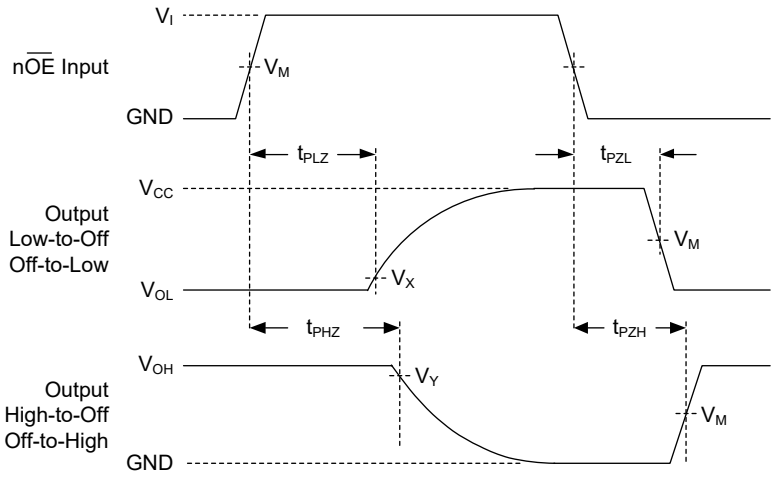
SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
4.5V to 5.5V	V_{CC}	≤ 3ns	15pF, 50pF	1kΩ	Open	V_{CC}	GND

WAVEFORMS



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (nAn) to Output (nYn) Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CC}	V_I	V_M (1)	V_M	V_X	V_Y
4.5V to 5.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3V	V_{OH} - 0.3V

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 3ns.

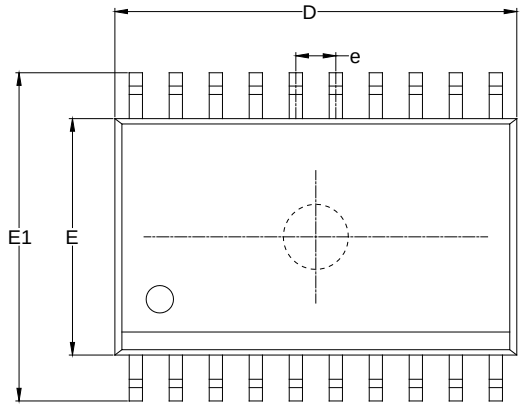
REVISION HISTORY

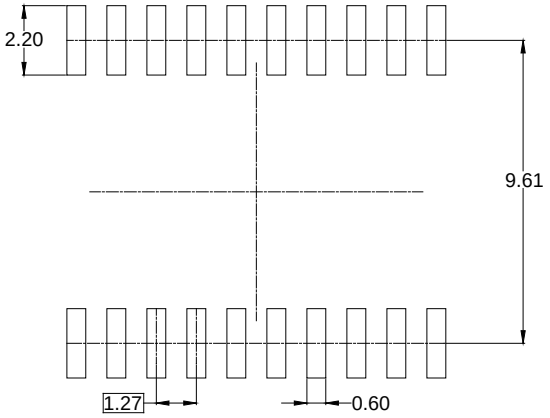
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (OCTOBER 2022) to REV.A	Page
Changed from product preview to production data	All

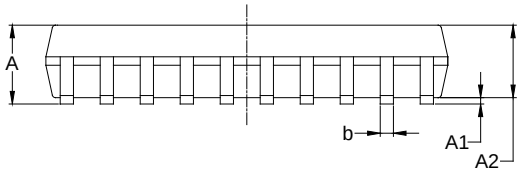
PACKAGE OUTLINE DIMENSIONS

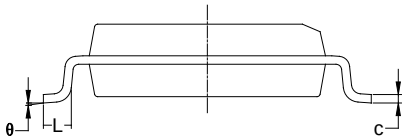
SOIC-20





RECOMMENDED LAND PATTERN (Unit: mm)



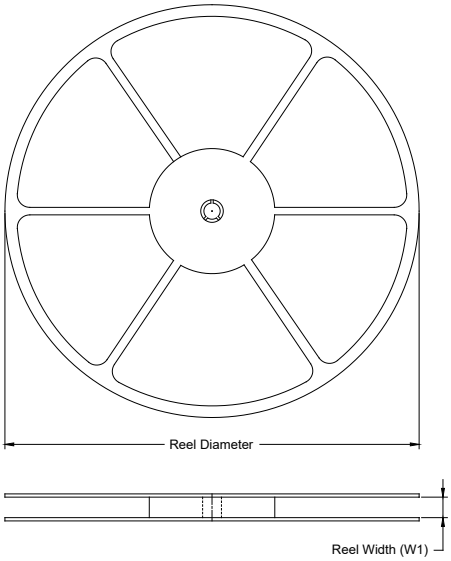


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

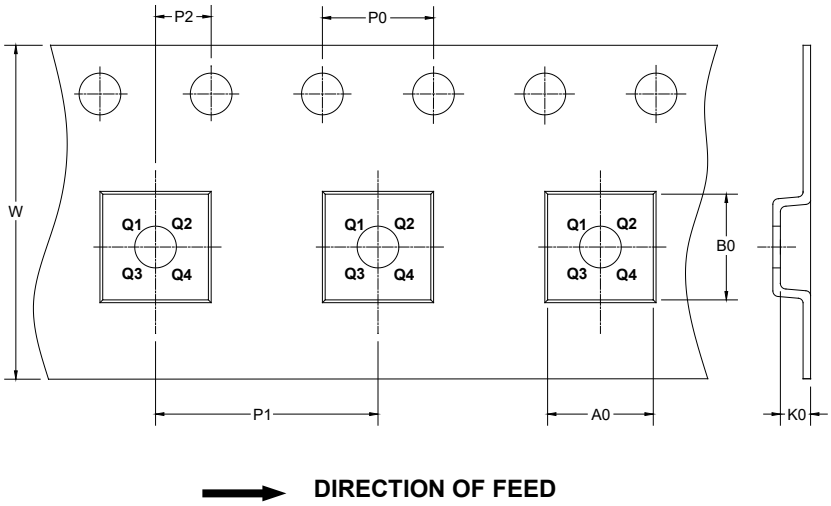
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



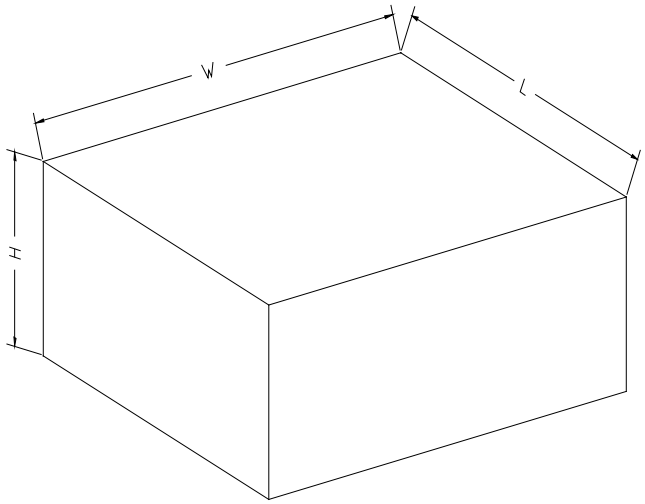
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-20	13"	24.4	10.90	13.30	3.00	4.0	12.0	2.0	24.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002