SGM4551
Dual Bidirectional I²C Bus and SMBus Voltage-Level Translator

GENERAL DESCRIPTION

This dual bidirectional I²C and SMBus voltage-level translator, with an enable (EN) input, is operational from 1.2V to 3.3V V_{REF1} and 1.8V to 5.5V V_{REF2}.

The SGM4551 allows bidirectional voltage translation between 1.2V and 5V, without the use of a direction pin. The low ON-state resistance (R_{ON}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is on, and the SCL1 and SDA1 I/Os are connected to the SCL2 and SDA2 I/Os, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

In I²C applications, the bus capacitance limit of 400pF restricts the number of devices and bus length. Using the SGM4551 enables the system designer to isolate two halves of a bus; thus, more I²C devices or longer trace length can be accommodated.

The SGM4551 also can be used to run two buses, one at 400kHz operating frequency and the other at 100kHz operating frequency. If the two buses are operating at different frequencies, the 100kHz bus must be isolated when the 400kHz operation of the other bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400kHz because of the delays added by the repeater.

As with the standard I²C system, pullup resistors are required to provide the logic high levels on the translator's bus. The SGM4551 has a standard open-drain configuration of the I²C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I²C devices, in addition to SMBus devices. Standard-mode I²C devices only specify 3mA in a generic I²C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.

When the SDA1 or SDA2 port is low, the clamp is in the on state, and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the drain pullup supply voltage (V_{DPU}) by the pullup resistor. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

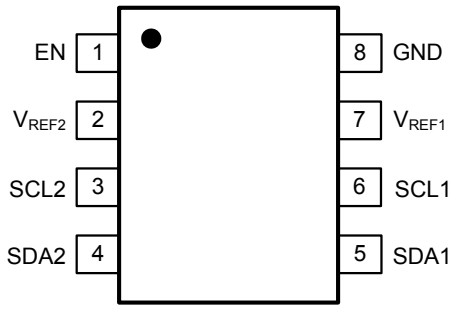
All channels have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower-voltage devices and at the same time protects less ESD-resistant devices.

The SGM4551 is available in Green SOT-23-8 and XTDFN-1.4×1-8L packages. It operates over an ambient temperature range of -40℃ to +85℃.

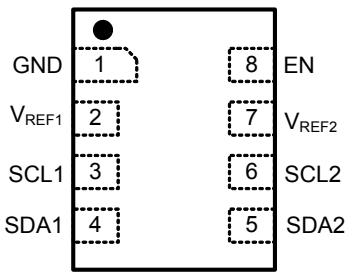
FEATURES

- 2-Bit Bidirectional Translator for SDA and SCL Lines in Mixed-Mode I²C Applications
- I²C and SMBus Compatible
- Less than 5.5ns Propagation Delay to Accommodate Standard-Mode and Fast-Mode I²C Devices and Multiple Masters
- Allows Voltage-Level Translator Between
  1.2V V_{REF1} and 1.8V, 2.5V, 3.3V, or 5V V_{REF2}
  1.8V V_{REF1} and 2.5V, 3.3V, or 5V V_{REF2}
  2.5V V_{REF1} and 3.3V or 5V V_{REF2}
  3.3V V_{REF1} and 5V V_{REF2}
- Provides Bidirectional Voltage Translation with No Direction Pin
- Low 3.5Ω ON-State Connection Between Input and Output Ports Provides Less Signal Distortion
- Open-Drain I²C I/O Ports (SCL1, SDA1, SCL2, and SDA2)
- 5V Tolerant I²C I/O Ports to Support Mixed-Mode Signal Operation
- High-Impedance SCL1, SDA1, SCL2, and SDA2 Pins for EN = Low
- Lock-Up-Free Operation for Isolation When EN = Low
- Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing
- Available in Green SOT-23-8 and XTDFN-1.4×1-8L Packages

PIN CONFIGURATIONS (TOP VIEW)



SOT-23-8



XTDFN-1.4×1-8L

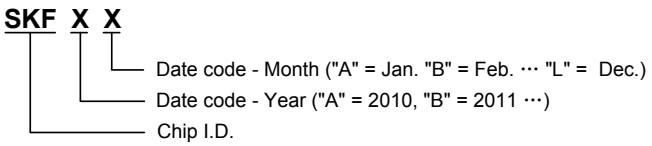
PIN DESCRIPTION

PIN		NAME	FUNCTION
SOT-23-8	XTDFN-1.4×1-8L		
1	8	EN	Switch Enable Input.
2	7	V_{REF2}	High-Voltage Side Reference Supply Voltage for SCL2 and SDA2.
3	6	SCL2	Serial Clock, High-Voltage Side.
4	5	SDA2	Serial Data, High-Voltage Side.
5	4	SDA1	Serial Data, Low-Voltage Side.
6	3	SCL1	Serial Clock, Low-Voltage Side.
7	2	V_{REF1}	Low-Voltage Side Reference Supply Voltage for SCL1 and SDA1.
8	1	GND	Ground, 0V.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM4551	SOT-23-8	SGM4551YN8G/TR	SKFXX	Tape and Reel, 3000
	XTDFN-1.4×1-8L	SGM4551YXDO8G/TR	N0X	Tape and Reel, 5000

NOTE: **X** = Date Code, **XX** = Date Code.



For example: SKFDB (2013, February)

ABSOLUTE MAXIMUM RATINGS

DC Reference Voltage Range, V_{REF1}.....-0.3V to 6V
DC Reference Bias Voltage Range, V_{REF2}..... -0.3V to 6V
Input Voltage Range (2), V_I..... -0.3V to 6V
Input/Output Voltage Range (2), $V_{I/O}$..... -0.3V to 6V
Continuous Channel Current.....64mA
Input Clamp Current, V_I < 0 .....-50mA
Operating Temperature Range..... -40℃ to +85℃
Junction Temperature..... 150℃
Storage Temperature Range.....-65℃ to +150℃
Lead Temperature (Soldering, 10sec)..... 260℃
ESD Susceptibility
HBM.....3000V
MM.....300V

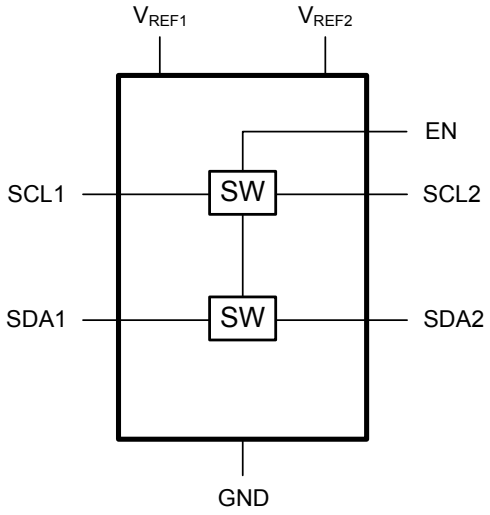
NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The input and input/output negative voltage ratings may be exceeded if the input and output current ratings are observed.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the latest datasheet.

LOGIC DIAGRAM



FUNCTION TABLE

INPUT EN (1)	TRANSLATOR FUNCTION
H	SCL1 = SCL2, SDA1 = SDA2
L	Disconnect

NOTE:
1. The SCL switch conducts if EN is ≥ 1V higher than SCL1 or SCL2. The same is true of SDA. H = HIGH level, L = LOW level.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +85℃, typical values are at T_A = +25℃, unless otherwise specified.)

PARAMETER		CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Input/Output Voltage ($V_{I/O}$)		SCL1, SDA1, SCL2, SDA2		Full	0		5	V
Reference Voltage (V_{REF1})				Full	0		5	V
Reference Voltage (V_{REF2})				Full	0		5	V
Enable Input Voltage (V_{EN})				Full	0		5	V
Pass Switch Current (I_{PASS})				Full			64	mA
Input Clamp Voltage (V_{IK})		I_I = -18mA, EN = 0V		Full			-1.2	V
Input Leakage Current (I_{IH})		V_I = 5V, EN = 0V		Full			8	μA
Enable Leakage Current (I_{EN})		V_I = 5V		Full			1	μA
Input Capacitance ($C_{I(EN)}$)		V_I = 3V or 0V		+25℃		15		pF
Off Capacitance ($C_{IO(OFF)}$)	SCLn, SDAn	V_O = 3V or 0V, EN = 0V		+25℃		8		pF
On Capacitance ($C_{IO(ON)}$)	SCLn, SDAn	V_O = 3V or 0V, EN = 3V		+25℃		7		pF
ON-State Resistance (R_{ON}) (1)	SCLn, SDAn	V_I = 0V, I_O = 64mA	EN = 4.5V	Full		3.5	5.5	Ω
			EN = 3.0V	Full		3.8	6.0	
			EN = 2.3V	Full		4.0	6.0	
			EN = 1.5V	Full		4.5	6.5	
		V_I = 2.4V, I_O = 15mA	EN = 4.5V	Full	1.5	4.5	7.0	
			EN = 3.0V	Full	11	40	65	
		V_I = 1.7V, I_O = 15mA	EN = 2.3V	Full	9	35	58	

NOTE:

1. Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

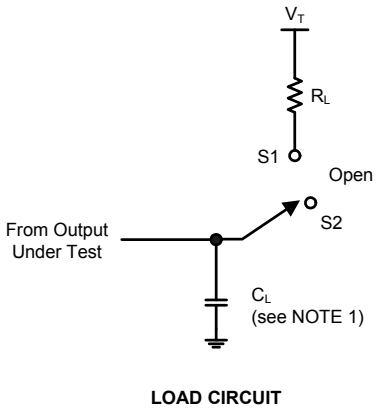
ELECTRICAL CHARACTERISTICS

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50pF	C_L = 30pF	C_L = 15pF	UNITS
AC PERFORMANCE (TRANSLATING DOWN) (2) - Switching Characteristics (Typical values are at T_A = +25℃, EN = 3.3V, V_{IH} = 2.3V, V_{IL} = 0V, V_M = 1.15V, unless otherwise specified.) (See Figure 1)						
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0.9	0.7	0.5	ns
t_{PHL}			0.9	0.7	0.5	
AC PERFORMANCE (TRANSLATING DOWN) (2) - Switching Characteristics (Typical values are at T_A = +25℃, EN = 2.5V, V_{IH} = 1.5V, V_{IL} = 0V, V_M = 0.75V, unless otherwise specified.) (See Figure 1)						
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0.9	0.7	0.5	ns
t_{PHL}			0.9	0.7	0.5	
AC PERFORMANCE (TRANSLATING UP) (3) - Switching Characteristics (Typical values are at T_A = +25℃, EN = 3.3V, V_{IH} = 2.3V, V_{IL} = 0V, V_T = 3.3V, V_M = 1.15V, R_L = 300Ω, unless otherwise specified.) (See Figure 1)						
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	1	0.8	0.6	ns
t_{PHL}			1	0.8	0.6	
AC PERFORMANCE (TRANSLATING UP) (3) - Switching Characteristics (Typical values are at T_A = +25℃, EN = 2.5V, V_{IH} = 1.5V, V_{IL} = 0V, V_T = 2.5V, V_M = 0.75V, R_L = 300Ω, unless otherwise specified.) (See Figure 1)						
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	1	0.8	0.6	ns
t_{PHL}			1	0.8	0.6	

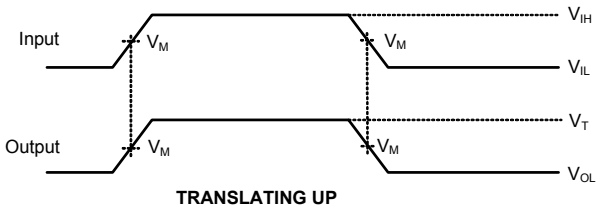
NOTES:
2. TRANSLATING DOWN: The higher voltage side driving toward the lower voltage side.
3. TRANSLATING UP: The lower voltage side driving toward the higher voltage side.

PARAMETER MEASUREMENT INFORMATION

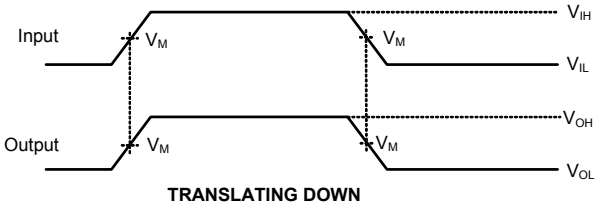
USAGE	SWITCH
Translating up	S1
Translating down	S2



LOAD CIRCUIT



TRANSLATING UP



TRANSLATING DOWN

NOTES:
1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r ≤ 2ns, t_f ≤ 2ns.
3. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit for Outputs

APPLICATION INFORMATION

General Applications of I²C

In I²C applications, the bus capacitance limit of 400pF restricts the number of devices and bus length. Using the SGM4551 enables the system designer to isolate two halves of a bus; thus, more I²C devices or longer trace length can be accommodated.

The SGM4551 also can be used to run two buses, one at 400kHz operating frequency and the other at 100kHz operating frequency. If the two buses are operating at different frequencies, the 100kHz bus must be isolated when the 400kHz operation of the other bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400kHz because of the delays added by the repeater.

As with the standard I²C system, pullup resistors are required to provide the logic high levels on the translator's bus. The SGM4551 has a standard open-drain configuration of the I²C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I²C devices, in addition to SMBus devices. Standard-mode I²C devices only specify 3mA in a generic I²C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.

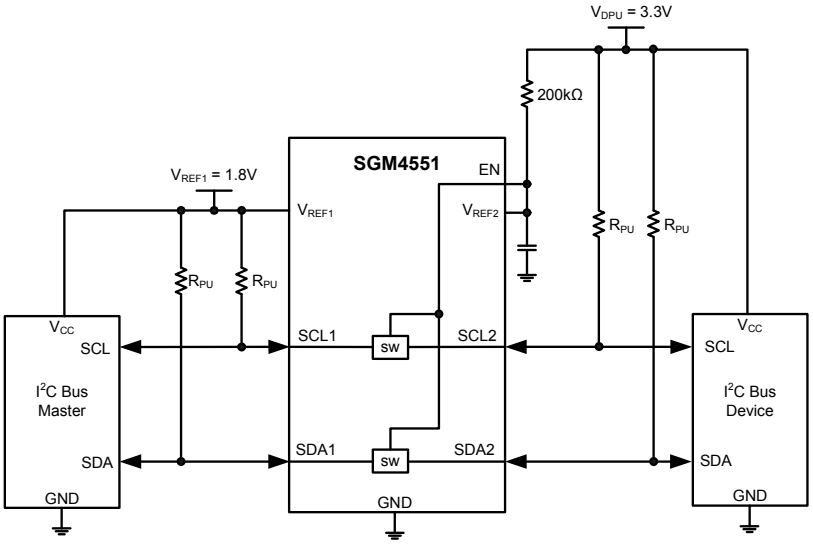


Figure 2. Typical Application Circuit (Switch Always Enabled)

Table 1. Application Operating Conditions (1)

PARAMETER	MIN	TYP	MAX	UNITS
Reference Voltage (V_{REF2})	V_{REF1} + 0.6	2.1	5	V
Enable Input Voltage (V_{EN})	V_{REF1} + 0.6	2.1	5	V
Reference Voltage (V_{REF1})	0	1.5	4.4	V
Pass Switch Current (I_{PASS})		14		mA
Reference-Transistor Current (I_{REF})		5		μA
Operating Temperature Range (T_A)	-40		85	℃

NOTE:

1. All typical values are at T_A = +25℃.

APPLICATION INFORMATION

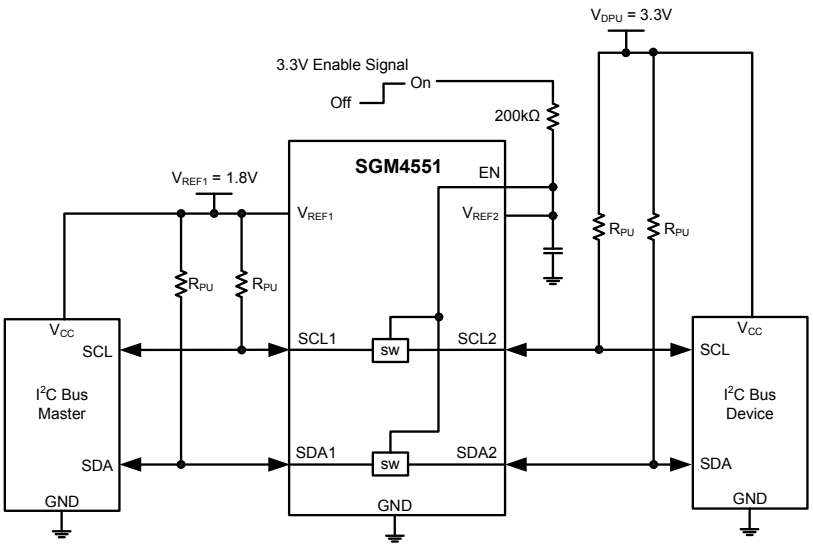


Figure 3. Typical Application Circuit (Switch Enable Control)

Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200kΩ). This allows V_{REF2} to regulate the EN input. A filter capacitor on V_{REF2} is recommended. The I^2C bus master output can be totem pole or open drain (pullup resistors may be required) and the I^2C bus device output can be totem pole or open drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open drain, no direction control is needed.

The reference supply voltage (V_{REF1}) is connected to the processor core power-supply voltage.

Sizing Pullup Resistor

The pullup resistor value needs to limit the current through the pass transistor, when it is in the on state, to about 15mA. This ensures a pass voltage of 260mV to 350mV. If the current through the pass transistor is higher than 15mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15mA, the pullup resistor value is calculated as:

$$R_{PU} = \frac{V_{DPU} - 0.35V}{0.015A}$$

Table 2 summarizes resistor values, reference voltages, and currents at 15mA, 10mA, and 3mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350mV or less. The external driver must be able to sink the total current from the resistors on both sides of the SGM4551 device at 0.175V, although the 15mA applies only to current flowing through the SGM4551 device.

APPLICATION INFORMATION

Table 2. Pullup Resistor Values (1) (2)

PULLUP RESISTOR VALUE (Ω)						
V_{DPU}	15mA		10mA		3mA	
	NOMINAL	+10% (3)	NOMINAL	+10% (3)	NOMINAL	+10% (3)
5V	310	341	465	512	1550	1705
3.3V	197	217	295	325	983	1082
2.5V	143	158	215	237	717	788
1.8V	97	106	145	160	483	532
1.5V	77	85	115	127	383	422
1.2V	57	63	85	94	283	312

NOTES:
1. Calculated for V_{OL} = 0.35V.
2. Assumes output driver V_{OL} = 0.175V at stated current.
3. +10% to compensate for V_{DD} range and resistor tolerance.

SGM4551 Bandwidth

The maximum frequency of the SGM4551 is dependent on the application. The device can operate at speeds of > 100MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application. The SGM4551 behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

The -3dB point of the SGM4551 is about 500MHz. However, this measurement is an analog type of measurement. For digital applications the signal should not degrade up to the fifth harmonic of the digital signal. As a rule of thumb, the frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the SGM4551, digital clock frequency of > 100MHz can be achieved.

The SGM4551 does not provide any drive capability. Therefore, higher frequency applications will require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3V) if the SGM4551 is being driven by standard CMOS totem pole output driver. Ideally, it is best to minimize the trace length from the SGM4551 on the sink side (1.8V) to minimize signal degradation.

You can then use a simple formula to compute the maximum “practical” frequency component, or the “knee” frequency (f_{knee}). All fast edges have an infinite spectrum of frequency components. However, there is an inflection (or “knee”) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate f_{knee}:

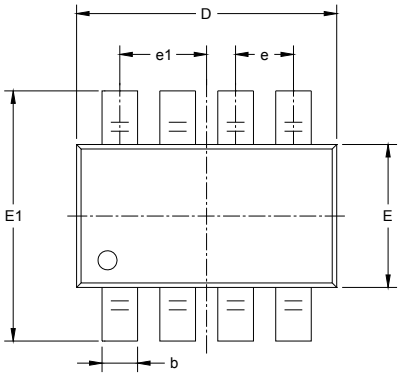
f_{knee} = 0.5/RT(10 - 90%)
f_{knee} = 0.4/RT(20 - 80%)

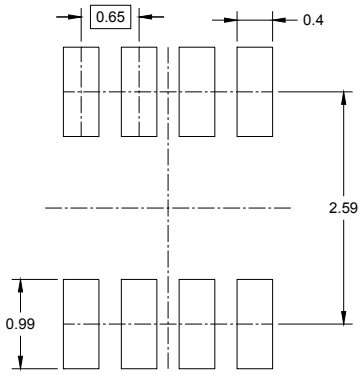
For signals with rise time characteristics based on 10 to 90 percent thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20 to 80 percent thresholds, which is very common in many of today's device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that will help maximize the performance of the device:
1. Keep trace length to a minimum by placing the SGM4551 close to the I²C output of the processor.
2. The trace length should be less than half the time of flight to reduce ringing and line reflections or non monotonic behavior in the switching region.
3. To reduce overshoots, a pullup resistor can be added on the 1.8V side; be aware that a slower fall time is to be expected.

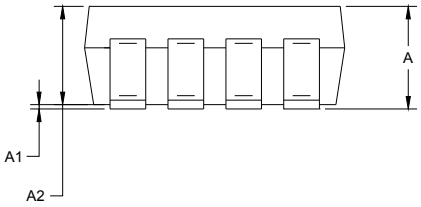
PACKAGE OUTLINE DIMENSIONS

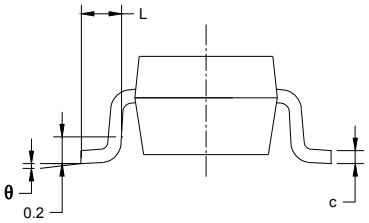
SOT-23-8





RECOMMENDED LAND PATTERN (Unit: mm)

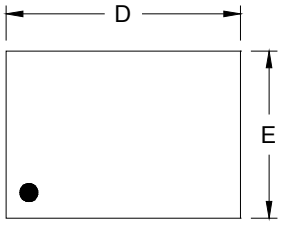




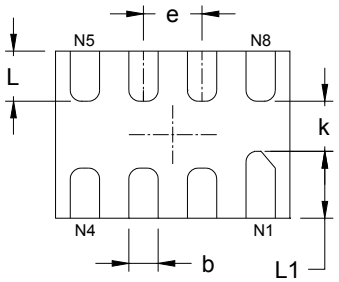
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.650 BSC		0.026 BSC	
e1	0.975 BSC		0.038 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

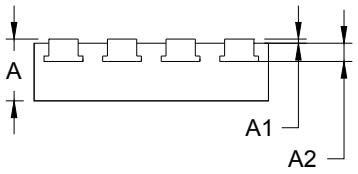
XTDFN-1.4×1-8L



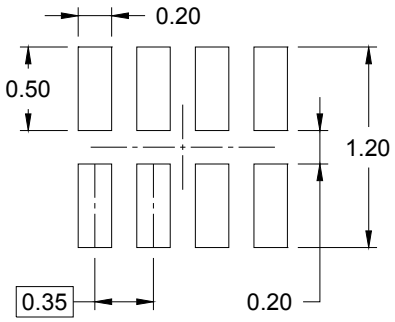
TOP VIEW



BOTTOM VIEW



SIDE VIEW

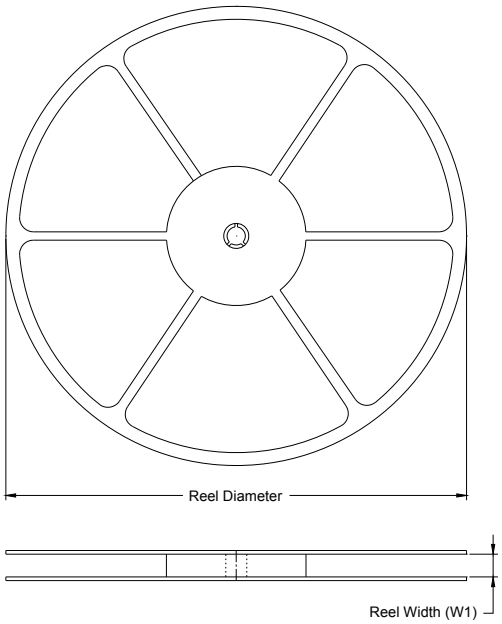


RECOMMENDED LAND PATTERN (Unit: mm)

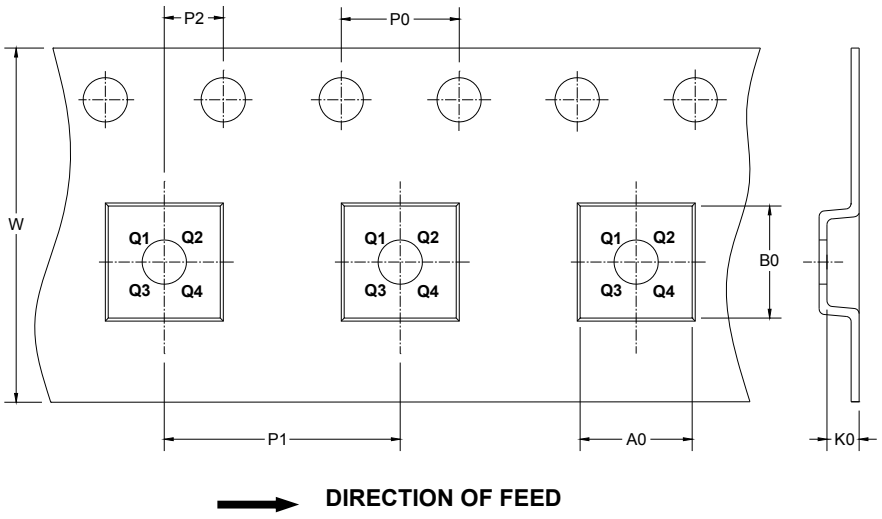
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.340	0.400	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.110 REF		0.004 REF	
D	1.350	1.450	0.053	0.057
E	0.950	1.050	0.037	0.041
k	0.200 MIN		0.008 MIN	
b	0.150	0.200	0.006	0.008
e	0.350 TYP		0.014 TYP	
L	0.250	0.350	0.010	0.014
L1	0.350	0.450	0.014	0.018

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS

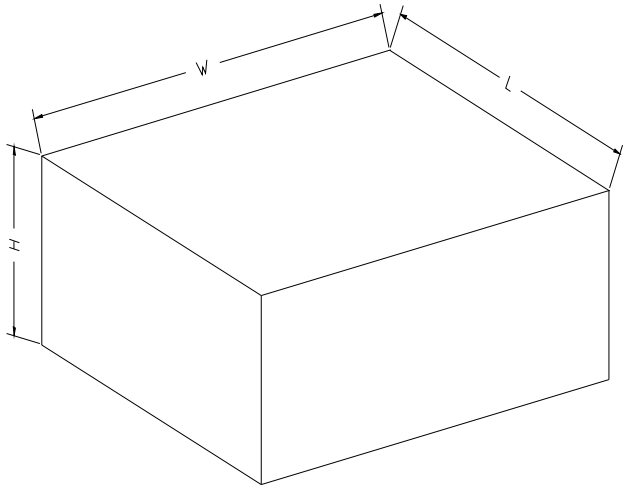


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-8	7″	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3
XTDFN-1.4×1-8L	7″	9.5	1.15	1.6	0.5	4.0	4.0	2.0	8.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18