BQ25713 / 713B I²C Narrow VDC Buck-Boost Battery Charge Controller With System Power Monitor and Processor Hot Monitor

1 Features

- Pin-to-pin and software compatible to BQ25703A
- Charge 1s to 4s battery from wide range of input source
  - 3.5-V to 24-V Input operating voltage
  - Supports USB2.0, USB 3.0, USB 3.1 (Type C), and USB Power Delivery (USB-PD) input current settings
  - Seamless transition among buck, buck-boost and boost operations
  - Input current and voltage regulation (IDPM and VDPM) against source overload
- Power/current monitor for CPU throttling
  - Comprehensive $\overline{\text{PROCHOT}}$ profile, IMVP8/ IMVP9 compliant
  - Input and battery current monitor
  - System power monitor, IMVP8/IMVP9 compliant
- Narrow voltage DC (NVDC) power path management
  - Instant-on with no battery or depleted battery
  - Battery supplements system when adapter is fully-loaded
  - Battery MOSFET ideal diode operation in supplement mode
- Power up USB port from battery (USB OTG)
  - 3-V to 20.8-V VOTG With 8-mV resolution
  - Output current limit up to 6.4 A with 50-mA resolution
- TI patented Pass Through Mode (PTM) for system power efficiency improvement and battery fast charging
- When system is powered by battery only, Vmin Active Protection (VAP) mode supplements battery from input capacitors during system peak power spike
- Input Current Optimizer (ICO) to extract max input power
- 800-kHz or 1.2-MHz Programmable switching frequency for 2.2-µH or 1.0-µH inductor
- Host control interface for flexible system configuration
  - I²C Port optimal system performance and status reporting
  - Hardware pin to set input current limit without EC control
- Integrated ADC to monitor voltage, current and power
- High accuracy for the regulation and monitor
  - ±0.5% Charge voltage regulation
  - ±2% Input/charge current regulation
  - ±2% Input/charge current monitor
  - ±4% Power monitor
- Safety
  - Thermal shutdown
  - Input, system, battery overvoltage protection
  - Input, MOSFET, inductor overcurrent protection
- Safety-Related Certifications:
  - IEC 62368-1 CB Certification
- Low battery quiescent current
- Package: 32-Pin 4 × 4 WQFN

2 Applications

- Drones, Bluetooth speakers, IP cameras, detachable, tablet PCs and power bank
- Industrial and medical equipment
- Portable equipment with rechargeable batteries

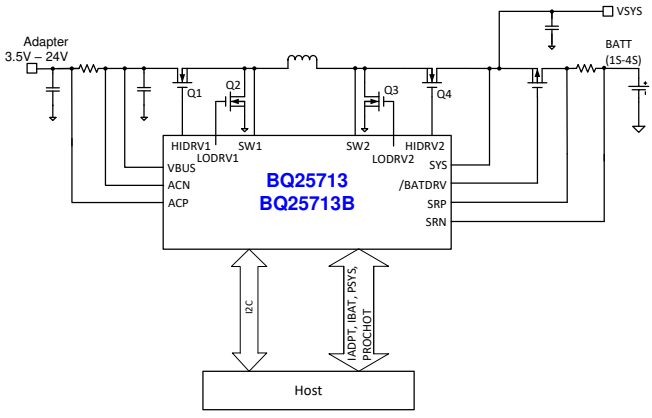
3 Description

This device is a synchronous NVDC buck-boost battery charge controller, offering a low component count, high efficiency solution for space constrained, 1s-4s battery charging applications.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
BQ25713, BQ25713B	WQFN (32)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Application Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2018) to Revision B (February 2021)	Page
• Added Safety-Related Certifications: IEC 62368-1 CB Certification to Features	1
• Changed units of measure for several parameters in Electrical Characteristics	10
• Changed in Timing Requirements	18
• Added bullet 2 in Power-Up from DC Source	24
• Changed 3.25A in Input Voltage and Current Limit Setup	25
• Changed in USB On-The-Go (OTG)	25
• Added in System Short Hiccup Mode	31
• Changed in I^2C Serial Interface	32
• Changed in ChargeOption0 Register	37
• Changed in ChargeOption2 Register	41
• Changed in ProchotOption0 Register	45
• Changed in ProchotStatus Register	52
• Changed in Input Current Registers	59
• Changed in IIN_DPM Register With 10-mΩ Sense Resistor	61
• Changed in ADCIINCMPIN Register	67
• Updated Typical Application Diagram	70
• Updated ACP-ACN Input Filter Diagram	71
• Updated Input Capacitor	72
• Updated Output Capacitor	72
• Changed in Layout Guidelines	79
• Added detailed layout reference in Layout Example	80

Changes from Revision * (June 2018) to Revision A (July 2018) **Page**

- Changed BQ25713 from Advance Information to Production Data and added BQ25713B 1

5 Description (continued)

The NVDC configuration allows the system to be regulated at battery voltage, but not drop below system minimum voltage. The system keeps operating even when the battery is completely discharged or removed. When load power exceeds input source rating, the battery goes into supplement mode and prevents the system from crashing.

BQ25713/BQ25713B charges battery from a wide range of input sources including USB adapter, high voltage USB PD sources and traditional adapters.

During power up, the charger sets converter to buck, boost or buck-boost configuration based on input source and battery conditions. The charger automatically transits among buck, boost and buck-boost configuration without host control.

In the absence of an input source, BQ25713/BQ25713B supports USB On-the-Go (OTG) function from 1- to 4-cell battery to generate adjustable 3 V to 20.8 V on VBUS with 8 mV resolution. The OTG output voltage transition slew rate can be configurable, which is complied with the USB PD 3.0 PPS specifications.

When only battery powers the system and no external load is connected to the USB OTG port, BQ25713/BQ25713B supports the Vmin Active Protection (VAP) feature, in which the device charges up the VBUS voltage from the battery to store some energy in the input decoupling capacitors. During the system peak power spike, the huge current drawing from the battery creates a larger voltage drop across the impedance from the battery to the system. The energy stored in the input capacitors will supplement the system, to prevent the system voltage from dropping below the minimum system voltage and causing the system crash. This Vmin Active Protection (VAP) is designed to absorb system power peaks during periods of SOC high power demand, which is highly recommended by Intel for the platforms with 1S~2S battery.

BQ25713/BQ25713B monitors adapter current, battery current and system power. The flexibly programmed $\overline{\text{PROCHOT}}$ output goes directly to CPU for throttle back when needed.

6 Device Comparison Table

	BQ25700A	BQ25703A	BQ25708	BQ25710	BQ25718	BQ25713	BQ25713B
Interface	SMBus	I2C	SMBus	SMBus	SMBus	I2C	I2C
Device Address	09h	6Bh	09h	09h	09h	6Bh	6Ah
VAP for IMVP9	No	No	No	Yes	Yes	Yes	Yes
Pass Through Mode	No	No	No	Yes	Yes	Yes	Yes
OTG Mode	Yes	Yes	No	Yes	No	Yes	Yes
OTG Voltage Range	4.48V-20.8V	4.48V-20.8V	N/A	3.0V-20.8V	N/A	3.0V-20.8V	3.0V-20.8V
OTG Voltage Resolution	64mV	64mV	N/A	8mV	N/A	8mV	8mV
Charging Voltage Resolution	16mV	16mV	16mV	8mV	8mV	8mV	8mV

7 Pin Configuration and Functions

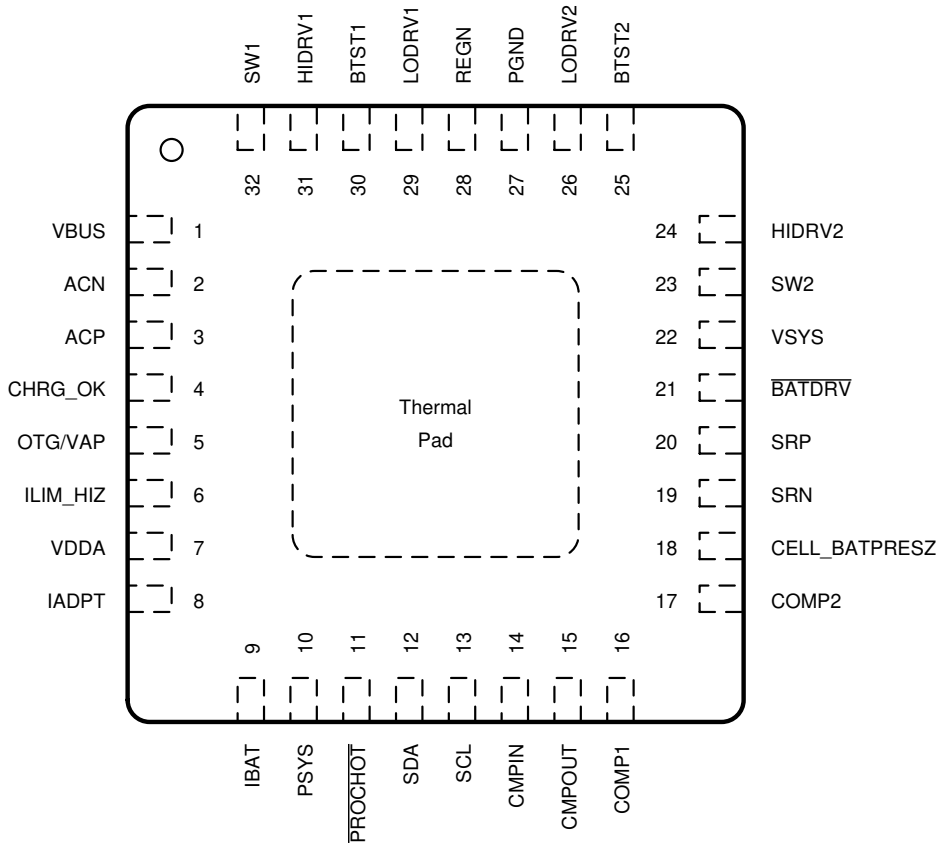


Figure 7-1. RSN Package 32-Pin WQFN Top View

Table 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ACN	2	PWR	Input current sense resistor negative input. The leakage on ACP and ACN are matched. A R-C low-pass filter is required to be placed between the sense resistor and the ACN pin to suppress the high frequency noise in the input current signal. Refer to Section 10 for ACP/ACN filter design.
ACP	3	PWR	Input current sense resistor positive input. The leakage on ACP and ACN are matched. A R-C low-pass filter is required to be placed between the sense resistor and the ACP pin to suppress the high frequency noise in the input current signal. Refer to Section 10 for ACP/ACN filter design.
$\overline{\text{BATDRV}}$	21	O	P-channel battery FET (BATFET) gate driver output. It is shorted to VSYS to turn off the BATFET. It goes 10 V below VSYS to fully turn on BATFET. BATFET is in linear mode to regulate VSYS at minimum system voltage when battery is depleted. BATFET is fully on during fast charge and works as an ideal-diode in supplement mode.
BTST1	30	PWR	Buck mode high side power MOSFET driver power supply. Connect a 0.047-µF capacitor between SW1 and BTST1. The bootstrap diode between REGN and BTST1 is integrated.
BTST2	25	PWR	Boost mode high side power MOSFET driver power supply. Connect a 0.047-µF capacitor between SW2 and BTST2. The bootstrap diode between REGN and BTST2 is integrated.
CELL_BATPRESZ	18	I	Battery cell selection pin for 1–4 cell battery setting. CELL_BATPRESZ pin is biased from VDDA. CELL_BATPRESZ pin also sets SYSOVP thresholds to 5 V for 1-cell, 12 V for 2-cell, and 19.5 V for 3-cell/4-cell. CELL_BATPRESZ pin is pulled below $V_{CELL\_BATPRESZ\_FALL}$ to indicate battery removal. The device exits LEARN mode, and disables charge. The charge voltage register REG0x05/04() goes back to default.

Table 7-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
CHRG_OK	4	O	Open drain active high indicator to inform the system good power source is connected to the charger input. Connect to the pullup rail via 10-kΩ resistor. When VBUS rises above 3.5V or falls below 24.5V, CHRG_OK is HIGH after 50ms deglitch time. When VBUS falls below 3.2 V or rises above 26 V, CHRG_OK is LOW. When any fault occurs, CHRG_OK is asserted LOW.
CMPIN	14	I	Input of independent comparator. The independent comparator compares the voltage sensed on CMPIN pin with internal reference, and its output is on CMPOUT pin. Internal reference, output polarity and deglitch time is selectable by the I^2C host. With polarity HIGH (REG0x30[6] = 1), place a resistor between CMPIN and CMPOUT to program hysteresis. With polarity LOW (REG0x30[6] = 0), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN to ground.
CMPOUT	15	O	Open-drain output of independent comparator. Place pullup resistor from CMPOUT to pullup supply rail. Internal reference, output polarity and deglitch time are selectable by the I^2C host.
COMP2	17	I	Buck boost converter compensation pin 2. Refer to BQ2571X EVM schematic for COMP2 pin RC network.
COMP1	16	I	Buck boost converter compensation pin 1. Refer to BQ2571X EVM schematic for COMP1 pin RC network.
OTG/VAP	5	I	Active HIGH to enable OTG or VAP modes. When REG0x34[5]=1, pulling high OTG/VAP pin and setting REG0x35[4]=1 can enable OTG mode. When REG0x34[5]=0, pulling high OTG/VAP pin is to enable VAP mode.
HIDRV1	31	O	Buck mode high side power MOSFET (Q1) driver. Connect to high side n-channel MOSFET gate.
HIDRV2	24	O	Boost mode high side power MOSFET(Q4) driver. Connect to high side n-channel MOSFET gate.
IADPT	8	O	The adapter current monitoring output pin. $V_{(IADPT)}$ = 20 or 40 × ($V_{(ACP)}$ – $V_{(ACN)}$) with ratio selectable in REG0x00[4]. Place a resistor from the IADPT pin to ground corresponding to the inductance in use. For a 2.2 µH inductance, the resistor is 137 kΩ. Place a 100-pF or less ceramic decoupling capacitor from IADPT pin to ground. IADPT output voltage is clamped below 3.3 V.
IBAT	9	O	The battery current monitoring output pin. $V_{(IBAT)}$ = 8 or 16 × ($V_{(SRP)}$ – $V_{(SRN)}$) for charge current, or $V_{(IBAT)}$ = 8 or 16 × ($V_{(SRN)}$ – $V_{(SRP)}$) for discharge current, with ratio selectable in REG0x00[3]. Place a 100-pF or less ceramic decoupling capacitor from IBAT pin to ground. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V.
ILIM_HIZ	6	I	Input current limit setting pin. Program ILIM_HIZ voltage by connecting a resistor divider from supply rail to ILIM_HIZ pin to ground. The pin voltage is calculated as: $V_{(ILIM\_HIZ)}$ = 1 V + 40 × IDPM × RAC, in which IDPM is the target input current. The input current limit used by the charger is the lower setting of ILIM_HIZ pin and REG0x0F/0E(). When the pin voltage is below 0.4 V, the device enters Hi-Z mode with low quiescent current. When the pin voltage is above 0.8 V, the device is out of Hi-Z mode.
LODRV1	29	O	Buck mode low side power MOSFET (Q2) driver. Connect to low side n-channel MOSFET gate.
LODRV2	26	O	Boost mode low side power MOSFET (Q3) driver. Connect to low side n-channel MOSFET gate.
PGND	27	GND	Device power ground.
$\overline{\text{PROCHOT}}$	11	O	Active low open drain output of processor hot indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the $\overline{\text{PROCHOT}}$ profile is triggered, a pulse is asserted. The minimum pulse width is adjustable in REG0x23[6:3].
PSYS	10	O	Current mode system power monitor. The output current is proportional to the total power from the adapter and the battery. The gain is selectable through I^2C. Place a resistor from PSYS to ground to generate output voltage. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V. Place a capacitor in parallel with the resistor for filtering.
REGN	28	PWR	6-V linear regulator output supplied from VBUS or VSYS. The LDO is active when VBUS above V_{VBUS_CONVEN} . Connect a 2.2- or 3.3-µF ceramic capacitor from REGN to power ground. REGN pin output is for power stage gate drive.
SCL	13	I	I^2C clock input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to I^2C specifications.

Table 7-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SDA	12	I/O	I^2C open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to I^2C specifications.
SRN	19	PWR	Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN pin with optional 0.1-µF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-µF ceramic capacitor from SRP to SRN to provide differential mode filtering. The leakage current on SRP and SRN are matched.
SRP	20	PWR	Charge current sense resistor positive input. Connect SRP pin with optional 0.1-uF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-µF ceramic capacitor from SRP to SRN to provide differential mode filtering. The leakage current on SRP and SRN are matched.
SW1	32	PWR	Buck mode high side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.
SW2	23	PWR	Boost mode high side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.
VBUS	1	PWR	Charger input voltage. An input low pass filter of 1Ω and 0.47 µF (minimum) is recommended.
VDDA	7	PWR	Internal reference bias pin. Connect a 10-Ω resistor from REGN to VDDA and a 1-µF ceramic capacitor from VDDA to power ground.
VSYS	22	PWR	Charger system voltage sensing. The system voltage regulation limit is programmed in REG0x05/04() and REG0X0D/0C().
Thermal pad	–	–	Exposed pad beneath the IC. Always solder thermal pad to the board, and have vias on the thermal pad plane connecting to power ground planes. It serves as a thermal pad to dissipate the heat.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Voltage	SRN, SRP, ACN, ACP, VBUS, VSYS	–0.3	30	V
	SW1, SW2	–2	30	
	BTST1, BTST2, HIDRV1, HIDRV2, /BATDRV	–0.3	36	
	LODRV1, LODRV2 (25nS)	–4	7	
	HIDRV1, HIDRV2 (25nS)	–4	36	
	SW1, SW2 (25nS)	–4	30	
	SDA, SCL, REGN, PSYS, CHRG_OK, OTG/VAP, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP1, COMP2, CMPIN, CMPOUT	–0.3	7	
	/PROCHOT	–0.3	5.5	
	IADPT, IBAT, PSYS	–0.3	3.6	
Differential Voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	–0.3	7	V
	SRP-SRN, ACP-ACN	–0.5	0.5	
Temperature	Junction temperature range, T_J	–40	155	°C
	Storage temperature, T_{stg}	–40	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	ACN, ACP, VBUS	0	24	V
	SRN, SRP, VSYS	0	19.2	
	SW1, SW2	–2	24	
	BTST1, BTST2, HIDRV1, HIDRV2, /BATDRV	0	30	
	SDA, SCL, REGN, PSYS, CHRG_OK, OTG/VAP, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP1, COMP2, CMPIN, CMPOUT	0	6.5	
	/PROCHOT	0	5.3	
	IADPT, IBAT, PSYS	0	3.3	
Differential Voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	0	6.5	V
	SRP-SRN, ACP-ACN	–0.5	0.5	
Junction temperature range, T_J		–20	125	°C

8.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating free-air temperature range, T_J	–40	85	°C

8.4 Thermal Information

THERMAL METRIC[1]		BQ25713/BQ25713B RSN (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

over T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INPUT_OP}	Input voltage operating range		3.5		26	V
REGULATION ACCURACY						
MAX SYSTEM VOLTAGE REGULATION						
V_{SYSMAX_RNG}	System Voltage Regulation, measured on V_{SYS} (charge disabled)		1.024		19.2	V
V_{SYSMAX_ACC}	System voltage regulation accuracy (charge disabled)	REG0x05/04() = 0x41A0H (16.800 V)		V_{SRN} + 160 mV		V
			–2%		2%	
		REG0x05/04() = 0x3138H (12.600 V)		V_{SRN} + 160 mV		V
			–2%		2%	
		REG0x05/04() = 0x20D0H (8.400 V)		V_{SRN} + 160 mV		V
			–3%		3%	
		REG0x05/04() = 0x1068H (4.200 V)		V_{SRN} + 160 mV		V
			–3%		3%	
MINIMUM SYSTEM VOLTAGE REGULATION						
V_{SYSMIN_RNG}	System Voltage Regulation, measured on V_{SYS}		1.024		19.2	V

8.5 Electrical Characteristics (continued)

over T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SYSMIN\_REG\_ACC}$	Minimum System Voltage Regulation Accuracy (VBAT below REG0x0D/0C() setting)	REG0x0D/0C() = 0x3000H		12.288		V
			–2%		2%	
		REG0x0D/0C() = 0x2400H		9.216		V
			–2%		2%	
		REG0x0D/0C() = 0x1800H		6.144		V
			–3%		3%	
		REG0x0D/0C() = 0x0E00H		3.584		V
			–3%		3%	
CHARGE VOLTAGE REGULATION						
V_{BAT_RNG}	Battery voltage regulation		1.024		19.2	V
$V_{BAT\_REG\_ACC}$	Battery voltage regulation accuracy (charge enable) (0°C to 85°C)	REG0x05/04() = 0x41A0H		16.8		V
			–0.5%		0.5%	
		REG0x05/04() = 0x3138H		12.6		V
			–0.5%		0.5%	
		REG0x05/04() = 0x20D0H		8.4		V
			–0.6%		0.6%	
		REG0x05/04() = 0x1068H		4.2		V
			–1.1%		1.2%	
CHARGE CURRENT REGULATION IN FAST CHARGE						
$V_{IREG\_CHG\_RNG}$	Charge current regulation differential voltage range	$V_{IREG\_CHG} = V_{SRP} - V_{SRN}$	0		81.28	mV
$I_{CHRG\_REG\_ACC}$	Charge current regulation accuracy 10-mΩ sensing resistor, VBAT above REG0x0D/0C() setting (0°C to 85°C)	REG0x03/02() = 0x1000H		4096		mA
			–3%		2%	
		REG0x03/02() = 0x0800H		2048		mA
			–4%		3%	
		REG0x03/02() = 0x0400H		1024		mA
			–5%		6%	
		REG0x03/02() = 0x0200H		512		mA
			–12%		12%	
CHARGE CURRENT REGULATION IN LDO MODE						
I_{CLAMP}	Pre-charge current clamp	CELL 2s-4s		384		mA
		CELL 1 s, VSRN < 3 V		384		mA
		CELL 1 s, 3 V < VSRN < VSYSMIN		2		A
$I_{PRECHRG\_REG\_ACC}$	Pre-charge current regulation accuracy with 10-mΩ SRP/SRN series resistor, VBAT below REG0x0D/0C() setting (0°C to 85°C)	REG0x03/02() = 0x0180H		384		mA
		2S-4S	–15%		15%	
		1S	–25%		25%	
		REG0x03/02() = 0x0100H		256		mA
		2S-4S	–20%		20%	
		1S	–35%		35%	
		REG0x03/02() = 0x00C0H		192		mA
		2S-4S	–25%		25%	
		1S	–50%		50%	
		REG0x03/02() = 0x0080H		128		mA
		2S-4S	–30%		30%	

8.5 Electrical Characteristics (continued)

over T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAK\_SRP\_SRN}$	SRP, SRN leakage current mismatch (0°C to 85°C)		–12		10	µA
INPUT CURRENT REGULATION						
$V_{IREG\_DPM\_RNG}$	Input current regulation differential voltage range	$V_{IREG\_DPM} = V_{ACP} – V_{ACN}$	0.5		64	mV
$I_{DPM\_REG\_ACC}$	Input current regulation accuracy (-40°C to 105°C) with 10-mΩ ACP/ACN series resistor	REG0x0F/0E() = 0x5000H	3800	3900	4000	mA
		REG0x0F/0E() = 0x3C00H	2800	2900	3000	mA
		REG0x0F/0E() = 0x1E00H	1300	1400	1500	mA
		REG0x0F/0E() = 0x0A00H	300	400	500	mA
$I_{LEAK\_ACP\_ACN}$	ACP, ACN leakage current mismatch (-40°C to 105°C)		–16		10	µA
$V_{IREG\_DPM\_RNG\_ILIM}$	Voltage range for input current regulation (ILIM_HIZ Pin)		1.15		4	V
$I_{DPM\_REG\_ACC\_ILIM}$	Input Current Regulation Accuracy on ILIM_HIZ pin V_{ILIM_HIZ} = 1 V + 40 × I_{DPM} × R_{AC}, with 10-mΩ ACP/ACN series resistor	V_{ILIM_HIZ} = 2.6 V	3800	4000	4200	mA
		V_{ILIM_HIZ} = 2.2 V	2800	3000	3200	mA
		V_{ILIM_HIZ} = 1.6 V	1300	1500	1700	mA
		V_{ILIM_HIZ} = 1.2 V	300	500	700	mA
I_{LEAK_ILIM}	ILIM_HIZ pin leakage current		–1		1	µA
INPUT VOLTAGE REGULATION						
$V_{IREG\_DPM\_RNG}$	Input voltage regulation range	Voltage on VBUS	3.2		19.52	V
$V_{DPM\_REG\_ACC}$	Input voltage regulation accuracy	REG0x0B/0A()=0x3C80H		18688		mV
			–3%		2%	
		REG0x0B/0A()=0x1E00H		10880		mV
			–4%		2.5%	
		REG0x0B/0A()=0x0500H		4480		mV
			–5%		5%	
OTG CURRENT REGULATION						
$V_{IOTG\_REG\_RNG}$	OTG output current regulation differential voltage range	$V_{IOTG\_REG} = V_{ACP} – V_{AC}N$	0		81.28	mV
I_{OTG_ACC}	OTG output current regulation accuracy with 50-mA LSB and 10-mΩ ACP/ACN series resistor	REG0x09/08() = 0x3C00H	2800	3000	3200	mA
		REG0x09/08() = 0x1E00H	1300	1500	1700	mA
		REG0x09/08() = 0x0A00H	300	500	700	mA
OTG VOLTAGE REGULATION						
$V_{OTG\_REG\_RNG}$	OTG voltage regulation range	Voltage on VBUS	3		20.8	V
$V_{OTG\_REG\_ACC}$	OTG voltage regulation accuracy	REG0x07/06() = 0x23F8H REG0x34[2] = 0		20.002		V
			–2%		2%	
		REG0x07/06() = 0x1710H REG0x34[2] = 1		12.004		V
			–2%		2%	
		REG0x07/06() = 0x099CH REG0x34[2] = 1		5.002		V
			–3%		3%	
REFERENCE AND BUFFER						
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage (0 mA – 60 mA)	V_{VBUS} = 10 V	5.7	6	6.3	V

8.5 Electrical Characteristics (continued)

over T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DROPOUT}$	REGN voltage in drop out mode	V_{VBUS} = 5 V, I_{LOAD} = 20 mA	3.8	4.3	4.6	V
$I_{REGN\_LIM\_Charging}$	REGN current limit when converter is enabled	V_{VBUS} = 10 V, force V_{REGN} =4 V	50	65		mA
C_{REGN}	REGN output capacitor required for stability	I_{LOAD} = 100 µA to 50 mA	2.2			µF
C_{VDDA}	REGN output capacitor required for stability	I_{LOAD} = 100 µA to 50 mA	1			µF
QUIESCENT CURRENT						
$I_{BAT\_BATFET\_ON}$	System powered by battery. BATFET on. I_{SRN} + I_{SRP} + I_{SW2} + I_{BTST2} + I_{SW1} + I_{BTST1} + I_{ACP} + I_{ACN} + I_{VBUS} + I_{VSYS}	VBAT = 18 V, REG0x01[7] = 1, in low power mode		22	45	µA
		VBAT = 18 V, REG0x01[7] = 1, REG0x31[5] = 1, REGN off		125	195	µA
		VBAT = 18 V, REG0x01[7] = 0, REG0x31[4] = 0, REGN on, DIS_PSYS		880	1170	µA
		VBAT = 18 V, REG0x01[7] = 0, REG0x31[4] = 1, REGN on, EN_PSYS		980	1270	µA
$I_{AC\_SW\_LIGHT\_buck}$	Input current during PFM in buck mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST} + I_{SW2} + I_{BTST2}	VIN = 20 V, VBAT = 12.6 V, 3s, REG0x01[2] = 0; MOSFET Qg = 4 nC		2.2		mA
$I_{AC\_SW\_LIGHT\_boost}$	Input current during PFM in boost mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST2} + I_{SW2} + I_{BTST2}	VIN = 5 V, VBAT = 8.4 V, 2s, REG0x01[2] = 0; MOSFET Qg = 4 nC		2.7		mA
$I_{AC\_SW\_LIGHT\_buckboost}$	Input current during PFM in buck boost mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	VIN = 12 V, VBAT = 12 V, REG0x01[2] = 0; MOSFET Qg = 4 nC		2.4		mA
$I_{OTG\_STANDBY}$	Quiescent current during PFM in OTG mode I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST2} + I_{SW2} + I_{BTST2}	VBAT = 8.4 V, VBUS = 5 V, 800 kHz switching frequency, MOSFET Qg = 4nC		3		mA
		VBAT = 8.4 V, VBUS = 12 V, 800 kHz switching frequency, MOSFET Qg = 4nC		4.2		mA
		VBAT = 8.4 V, VBUS = 20 V, 800 kHz switching frequency, MOSFET Qg = 4nC		6.2		mA
V_{ACP/N_OP}	Input common mode range	Voltage on ACP/ACN	3.8		26	V
V_{IADPT_CLAMP}	I_{ADPT} output clamp voltage		3.1	3.2	3.3	V
I_{IADPT}	I_{ADPT} output current				1	mA
A_{IADPT}	Input current sensing gain	$V_{(IADPT)}$ / $V_{(ACP-ACN)}$, REG0x00[4] = 0		20		V/V
		$V_{(IADPT)}$ / $V_{(ACP-ACN)}$, REG0x00[4] = 1		40		V/V
V_{IADPT_ACC}	Input current monitor accuracy	$V_{(ACP-ACN)}$ = 40.96 mV	–2%		2%	
		$V_{(ACP-ACN)}$ = 20.48 mV	–3%		3%	
		$V_{(ACP-ACN)}$ =10.24 mV	–6%		6%	
		$V_{(ACP-ACN)}$ = 5.12 mV	–10%		10%	
C_{IADPT_MAX}	Maximum capacitance at IADPT Pin				100	pF
V_{SRP/N_OP}	Battery common mode range	Voltage on SRP/SRN	2.5		18	V

8.5 Electrical Characteristics (continued)

over T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IBAT_CLAMP}	IBAT output clamp voltage		3.05	3.2	3.3	V
I_{IBAT}	IBAT output current				1	mA
A_{IBAT}	Charge and discharge current sensing gain on IBAT pin	$V_{(IBAT)}$ / $V_{(SRN-SRP)}$, REG0x00[3] = 0,		8		V/V
		$V_{(IBAT)}$ / $V_{(SRN-SRP)}$, REG0x00[3] = 1,		16		V/V
$I_{IBAT\_CHG\_ACC}$	Charge and discharge current monitor accuracy on IBAT pin	$V_{(SRN-SRP)}$ = 40.96 mV	–2%		2%	
		$V_{(SRN-SRP)}$ = 20.48 mV	–4%		4%	
		$V_{(SRN-SRP)}$ =10.24 mV	–7%		7%	
		$V_{(SRN-SRP)}$ = 5.12 mV	–15%		15%	
C_{IBAT_MAX}	Maximum capacitance at IBAT Pin				100	pF
SYSTEM POWER SENSE AMPLIFIER						
V_{PSYS}	PSYS output voltage range		0		3.3	V
I_{PSYS}	PSYS output current		0		160	µA
A_{PSYS}	PSYS system gain	$V_{(PSYS)}$ / ($P_{(IN)}$ +$P_{(BAT)}$), REG0x31[1] = 1		1		µA/W
V_{PSYS_ACC}	PSYS gain accuracy (REG0x31[1] = 1)	Adapter only with system power = 19.5 V / 45 W, TA = -40°C to 85°C	–4%		4%	
		Battery only with system power = 11 V / 44 W, TA = –40°C to 85°C	–3%		3%	
V_{PSYS_CLAMP}	PSYS clamp voltage		3		3.3	V
COMPARATOR						
VBUS UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{VBUS_UVLOZ}	VBUS undervoltage rising threshold	VBUS rising	2.30	2.55	2.80	V
V_{VBUS_UVLO}	VBUS undervoltage falling threshold	VBUS falling	2.18	2.40	2.62	V
$V_{VBUS\_UVLO\_HYST}$	VBUS undervoltage hysteresis			150		mV
V_{VBUS_CONVEN}	VBUS converter enable rising threshold	VBUS rising	3.2	3.5	3.9	V
$V_{VBUS\_CONVENZ}$	VBUS converter enable falling threshold	VBUS falling	2.9	3.2	3.5	V
$V_{VBUS\_CONVEN\_HYST}$	VBUS converter enable hysteresis			400		mV
BATTERY UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{VBAT_UVLOZ}	VBAT undervoltage rising threshold	VSRN rising	2.35	2.55	2.75	V
V_{VBAT_UVLO}	VBAT undervoltage falling threshold	VSRN falling	2.2	2.4	2.6	V
$V_{VBAT\_UVLO\_HYST}$	VBAT undervoltage hysteresis			150		mV
V_{VBAT_OTGEN}	VBAT OTG enable rising threshold	VSRN rising	3.25	3.55	3.85	V
V_{VBAT_OTGENZ}	VBAT OTG enable falling threshold	VSRN falling	2.2	2.4	2.6	V
$V_{VBAT\_OTGEN\_HYST}$	VBAT OTG enable hysteresis			1100		mV
VBUS UNDER VOLTAGE COMPARATOR (OTG MODE)						
$V_{VBUS\_OTG\_UV}$	VBUS undervoltage falling threshold	As percentage of REG0x07/06()		85		%

8.5 Electrical Characteristics (continued)

over T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{VBUS\_OTG\_UV}$	VBUS time undervoltage deglitch			7		ms
VBUS OVER VOLTAGE COMPARATOR (OTG MODE)						
$V_{VBUS\_OTG\_OV}$	VBUS overvoltage rising threshold	As percentage of REG0x07/06()		110		%
$t_{VBUS\_OTG\_OV}$	VBUS Time Over-Voltage Deglitch			10		ms
PRE-CHARGE to FAST CHARGE TRANSITION						
$V_{BAT\_SYSMIN\_RISE}$	LDO mode to fast charge mode threshold, VSRN rising	as percentage of 0x0D/0C()	98	100	102	%
$V_{BAT\_SYSMIN\_FALL}$	LDO mode to fast charge mode threshold, VSRN falling	as percentage of 0x0D/0C()		97.5		%
$V_{BAT\_SYSMIN\_HYST}$	Fast charge mode to LDO mode threshold hysteresis	as percentage of 0x0D/0C()		2.5		%
BATTERY LOWV COMPARATOR (Pre-charge to Fast Charge Threshold for 1S)						
V_{BATLV_FALL}	BATLOWV falling threshold	1 s		2.8		V
V_{BATLV_RISE}	BATLOWV rising threshold			3		V
V_{BATLV_RHYST}	BATLOWV hysteresis			200		mV
INPUT OVER-VOLTAGE COMPARATOR (ACOVP)						
V_{ACOV_RISE}	VBUS overvoltage rising threshold	VBUS rising	25	26	27	V
V_{ACOV_FALL}	VBUS overvoltage falling threshold	VBUS falling	23.5	24.5	25	V
V_{ACOV_HYST}	VBUS overvoltage hysteresis			1.5		V
$t_{ACOV\_RISE\_DEG}$	VBUS deglitch overvoltage rising	VBUS converter rising to stop converter		100		µs
$t_{ACOV\_FALL\_DEG}$	VBUS deglitch overvoltage falling	VBUS converter falling to start converter		1		ms
INPUT OVER CURRENT COMPARATOR (ACOC)						
V_{ACOC}	ACP to ACN rising threshold, w.r.t. ILIM2 in REG0x37[7:4]	Voltage across input sense resistor rising, REG0x32[2] = 1	1.8	2	2.2	
V_{ACOC_FLOOR}	Measure between ACP and ACN	Set IDPM to minimum	44	50	56	mV
$V_{ACOC\_CEILING}$	Measure between ACP and ACN	Set IDPM to maximum	172	180	188	mV
$t_{ACOC\_DEG\_RISE}$	Rising deglitch time	Deglitch time to trigger ACOC		250		µs
t_{ACOC_RELAX}	Relax time	Relax time before converter starts again		250		ms
SYSTEM OVER-VOLTAGE COMPARATOR (SYSOVP)						
V_{SYSOVP_RISE}	System overvoltage rising threshold to turn off converter	1 s	4.85	5	5.1	V
		2 s	11.7	12	12.2	V
		3 s, 4 s	19	19.5	20	V
V_{SYSOVP_FALL}	System overvoltage falling threshold	1 s		4.8		V
		2 s		11.5		V
		3 s, 4 s		19		V
I_{SYSOVP}	Discharge current when SYSOVP stop switching was triggered	on SYS		20		mA
BAT OVER-VOLTAGE COMPARATOR (BATOVP)						
V_{BATOVP_RISE}	Overvoltage rising threshold as percentage of VBAT_REG in REG0x05/04()	1 s, 4.2 V	102.5	104	106	%
		2 s - 4 s	102.5	104	105	%

8.5 Electrical Characteristics (continued)

over T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATOVP_FALL}	Overvoltage falling threshold as percentage of VBAT_REG in REG0x05/04()	1 s	100	102	104	%
		2 s - 4 s	100	102	103	%
V_{BATOVP_HYST}	Overvoltage hysteresis as percentage of VBAT_REG in REG0x05/04()	1 s		2		%
		2 s - 4 s		2		%
I_{BATOVP}	Discharge current during BATOVP	on VSYS pin		20		mA
t_{BATOVP_RISE}	Overvoltage rising deglitch to turn off BATDRV to disable charge			20		ms
CONVERTER OVER-CURRENT COMPARATOR (Q2)						
VOCP_limit_Q2	Converter Over-Current Limit	REG0x32[5]=1		150		mV
		REG0x32[5]=0		210		mV
VOCP_limit_SYSSHORT_Q2	System Short or SRN < 2.4 V	REG0x32[5]=1		45		mV
		REG0x32[5]=0		60		mV
CONVERTER OVER-CURRENT COMPARATOR (ACX)						
VOCP_limit_ACX	Converter Over-Current Limit	REG0x32[4]=1		150		mV
		REG0x32[4]=0		280		mV
VOCP_limit_SYSSHORT_ACX	System Short or SRN < 2.4 V	REG0x32[4]=1		90		mV
		REG0x32[4]=0		150		mV
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT_RISE}	Thermal shutdown rising temperature	Temperature increasing		155		°C
T_{SHUTF_FALL}	Thermal shutdown falling temperature	Temperature reducing		135		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			20		°C
t_{SHUT_RDEG}	Thermal deglitch shutdown rising			100		µs
t_{SHUT_FHYS}	Thermal deglitch shutdown falling			12		ms
VSYS PROCHOT COMPARATOR						
VSYS_TH1	VSYS_TH1 comparator falling threshold	REG0x36[7:4] = 0111, 2-4 s		6.6		V
		REG0x36[7:4] = 0100, 1 s		3.5		V
VSYS_TH2	VSYS_TH2 comparator falling threshold	REG0x36[3:2] = 10, 2-4 s		6.5		V
		REG0x36[3:2] = 10, 1 s		3.5		V
$t_{SYS\_PRO\_falling\_DEG}$	V_{SYS} falling deglitch for throttling			4		µs
ICRIT PROCHOT COMPARATOR						
V_{ICRIT_PRO}	Input current rising threshold for throttling as 10% above ILIM2 (REG0x37[7:3])	Only when ILIM2 setting is higher than 2A	105	110	117	%
INOM PROCHOT COMPARATOR						
V_{INOM_PRO}	INOM rising threshold as 10% above IIN (REG0x0F/0E())		105	110	116	%
IDCHG PROCHOT COMPARATOR						
V_{IDCHG_PRO}	IDCHG threshold for throttling for IDSCHG of 6 A	REG0x39[7:2] = 001100		6272		mA
			95		103	%
INDEPENDENT COMPARATOR						

8.5 Electrical Characteristics (continued)

over T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INDEP_CMP}	Independent comparator threshold	REG0x30[7] = 1, CMPIN falling	1.17	1.2	1.23	V
		REG0x30[7] = 0, CMPIN falling	2.27	2.3	2.33	V
$V_{INDEP\_CMP\_HYS}$	Independent comparator hysteresis	REG0x30[7] = 0, CMPIN falling		100		mV
POWER MOSFET DRIVER						
PWM OSCILLATOR AND RAMP						
F_{SW}	PWM switching frequency	REG0x01[1] = 0	1020	1200	1380	kHz
		REG0x01[1] = 1	680	800	920	kHz
BATFET GATE DRIVER (BATDRV)						
V_{BATDRV_ON}	Gate drive voltage on BATFET		8.5	10	11.5	V
V_{BATDRV_DIODE}	Drain-source voltage on BATFET during ideal diode operation			30		mV
R_{BATDRV_ON}	Measured by sourcing 10 µA current to BATDRV		2.5	4	6	kΩ
R_{BATDRV_OFF}	Measured by sinking 10 µA current from BATDRV			1.2	2.1	kΩ
PWM HIGH SIDE DRIVER (HIDRV Q1)						
$R_{DS\_HI\_ON\_Q1}$	High side driver (HSD) turn on resistance	V_{BTST1} - V_{SW1} = 5 V		6		Ω
$R_{DS\_HI\_OFF\_Q1}$	High side driver turn off resistance	V_{BTST1} - V_{SW1} = 5 V		1.3	2.2	Ω
$V_{BTST1\_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	V_{BTST1} - V_{SW1} when low side refresh pulse is requested	3.2	3.7	4.6	V
PWM HIGH SIDE DRIVER (HIDRV Q4)						
$R_{DS\_HI\_ON\_Q4}$	High side driver (HSD) turn on resistance	V_{BTST2} - V_{SW2} = 5 V		6		Ω
$R_{DS\_HI\_OFF\_Q4}$	High side driver turn off resistance	V_{BTST2} - V_{SW2} = 5 V		1.5	2.4	Ω
$V_{BTST2\_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	V_{BTST2} - V_{SW2} when low side refresh pulse is requested	3.1	3.7	4.5	V
PWM LOW SIDE DRIVER (LODRV Q2)						
$R_{DS\_LO\_ON\_Q2}$	Low side driver (LSD) turn on resistance	V_{BTST1} - V_{SW1} = 5.5 V		6		Ω
$R_{DS\_LO\_OFF\_Q2}$	Low side driver turn off resistance	V_{BTST1} - V_{SW1} = 5.5 V		1.7	2.6	Ω
PWM LOW SIDE DRIVER (LODRV Q3)						
$R_{DS\_LO\_ON\_Q3}$	Low side driver (LSD) turn on resistance	V_{BTST2} - V_{SW2} = 5.5 V		7.6		Ω
$R_{DS\_LO\_OFF\_Q3}$	Low side driver turn off resistance	V_{BTST2} - V_{SW2} = 5.5 V		2.9	4.6	Ω
INTERNAL SOFT START During Charge Enable						
SSSTEP_DAC	Soft Start Step Size			64		mA
SSSTEP_DAC	Soft Start Step Time			8		µs
INTEGRATED BTST DIODE (D1)						
V_{F_D1}	Forward bias voltage	IF = 20 mA at 25°C		0.8		V
V_{R_D1}	Reverse breakdown voltage	IR = 2 µA at 25°C			20	V
INTEGRATED BTST DIODE (D2)						
V_{F_D2}	Forward bias voltage	IF = 20 mA at 25°C		0.8		V
V_{R_D2}	Reverse breakdown voltage	IR = 2 µA at 25°C			20	V
INTERFACE						

8.5 Electrical Characteristics (continued)

over T_J = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT (SDA, SCL, OTG/VAP)						
V_{IN_LO}	Input low threshold	I2C			0.4	V
V_{IN_HI}	Input high threshold	I2C	1.3			V
LOGIC OUTPUT OPEN DRAIN (SDA, CHRG_OK, CMPOUT)						
V_{OUT_LO}	Output saturation voltage	5 mA drain current			0.4	V
V_{OUT_LEAK}	Leakage current	V = 7 V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN SDA						
$V_{OUT\_LO\_SDA}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT\_LEAK\_SDA}$	Leakage Current	V = 7V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN CHRG_OK						
$V_{OUT\_LO\_CHRG\_OK}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT\_LEAK\_CHRG\_OK}$	Leakage Current	V = 7V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN CMPOUT						
$V_{OUT\_LO\_CMPOUT}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT\_LEAK\_CMPOUT}$	Leakage Current	V = 7V	–1		1	µA
LOGIC OUTPUT OPEN DRAIN (PROCHOT)						
$V_{OUT\_LO\_PROCHOT}$	Output saturation voltage	50 Ω pullup to 1.05 V / 5-mA			300	mV
$V_{OUT\_LEAK\_PROCHOT}$	Leakage current	V = 5.5 V	–1		1	µA
ANALOG INPUT (ILIM_HIZ)						
V_{HIZ_LO}	Voltage to get out of HIZ mode	ILIM_HIZ pin rising	0.8			V
V_{HIZ_HIGH}	Voltage to enable HIZ mode	ILIM_HIZ pin falling			0.4	V
ANALOG INPUT (CELL_BATPRESZ)						
V_{CELL_4S}	4S	REGN of REGN = 6 V, as percentage	68.4	75		%
V_{CELL_3S}	3S	REGN of REGN = 6 V, as percentage	51.7	55	65	%
V_{CELL_2S}	2S	REGN of REGN = 6 V, as percentage	35	40	49.1	%
V_{CELL_1S}	1S	REGN of REGN = 6 V, as percentage	18.4	25	31.6	%
$V_{CELL\_BATPRESZ\_RISE}$	Battery is present	CELL_BATPRESZ rising	18			%
$V_{CELL\_BATPRESZ\_FALL}$	Battery is removed	CELL_BATPRESZ falling			15	%

8.6 Timing Requirements

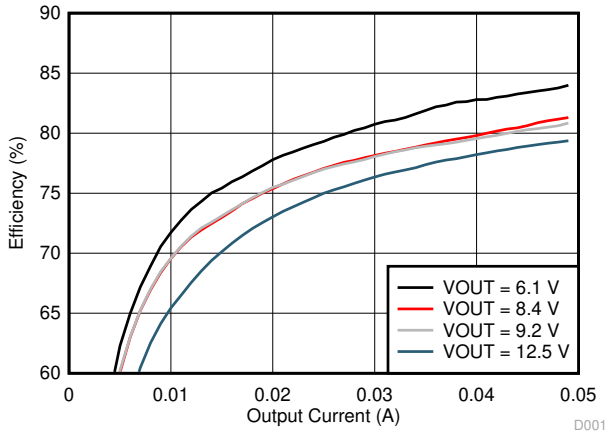
		MIN	NOM	MAX	UNIT
I2C TIMING CHARACTERISTICS					
t_r	SCLK/SDATA rise time			300	ns
t_f	SCLK/SDATA fall time			300	ns
$t_{W(H)}$	SCLK pulse width high	0.6		50	µs
$t_{W(L)}$	SCLK Pulse Width Low	1.3			µs
$t_{SU(STA)}$	Setup time for START condition	0.6			µs
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated	0.6			µs
$t_{SU(DAT)}$	Data setup time	100			ns
$t_{H(DAT)}$	Data hold time	300			ns
$t_{SU(STOP)}$	Setup time for STOP condition	0.6			µs

		MIN	NOM	MAX	UNIT
$t_{(BUF)}$	Bus free time between START and STOP condition	1.3			µs
$F_{S(CL)}$	Clock Frequency	10		400	kHz
HOST COMMUNICATION FAILURE					
$t_{timeout}$	I2C bus release timeout(1)	25		35	ms
t_{Deg_WD}	Deglitch for watchdog reset signal	10			ms
t_{WDI}	Watchdog timeout period, ChargeOption() bit [14:13] = 01(2)	4	5.5	7	s
	Watchdog timeout period, ChargeOption() bit bit [14:13] = 10(2)	70	88	105	s
	Watchdog timeout period, ChargeOption() bit bit [14:13] = 11(2)	140	175	210	s

(1) Devices participating in a transfer will timeout when any clock low exceeds the 25ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35 ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10 ms) and a slave (25 ms).

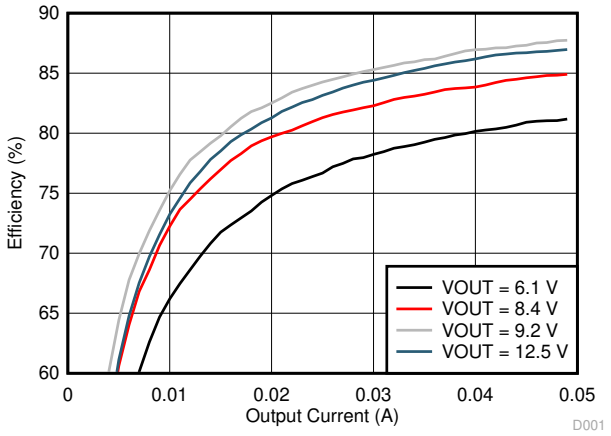
(2) User can adjust threshold via I2C ChargeOption() REG0x01/00().

8.7 Typical Characteristics



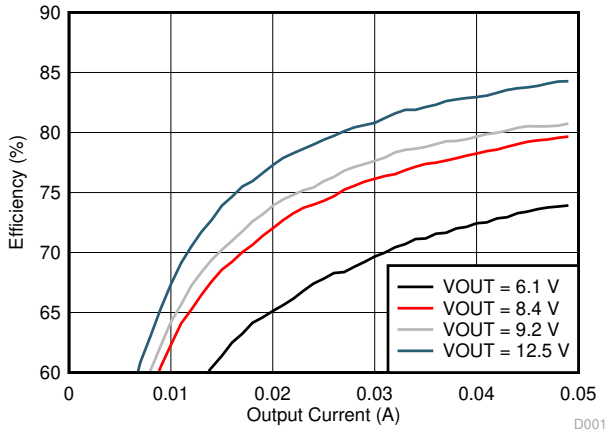
VIN = 5 V

Figure 8-1. Light Load Efficiency



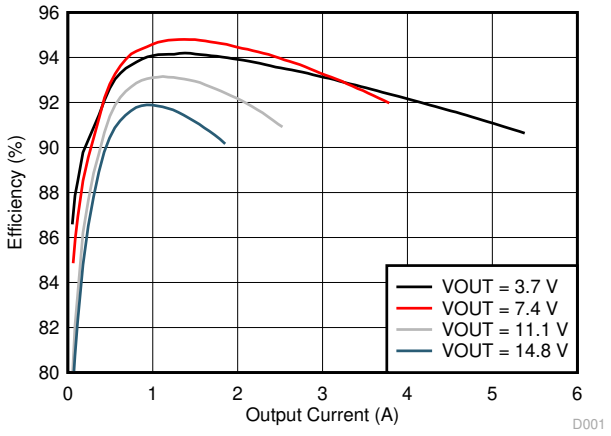
VIN = 12 V

Figure 8-2. Light Load Efficiency



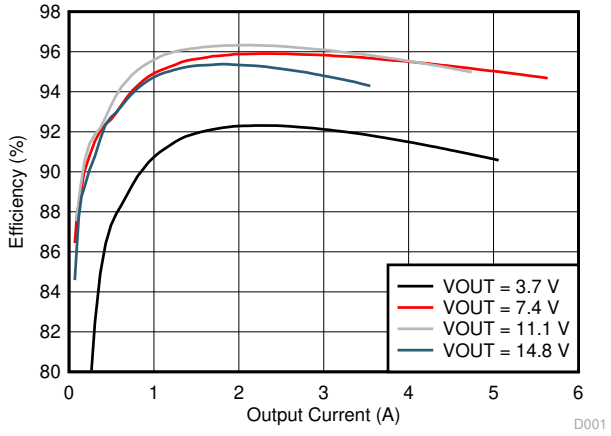
VIN = 20 V

Figure 8-3. Light Load Efficiency



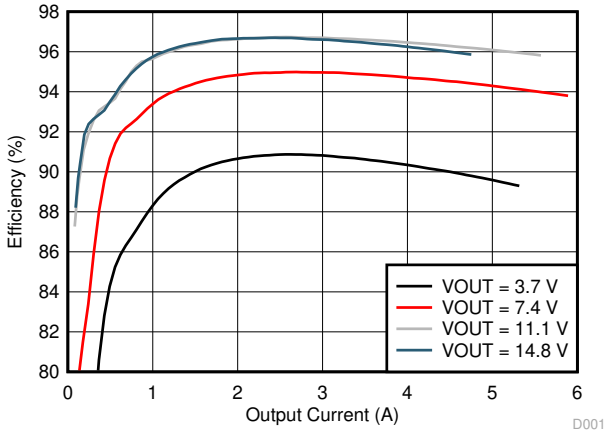
VIN = 5 V

Figure 8-4. System Efficiency



VIN = 9 V

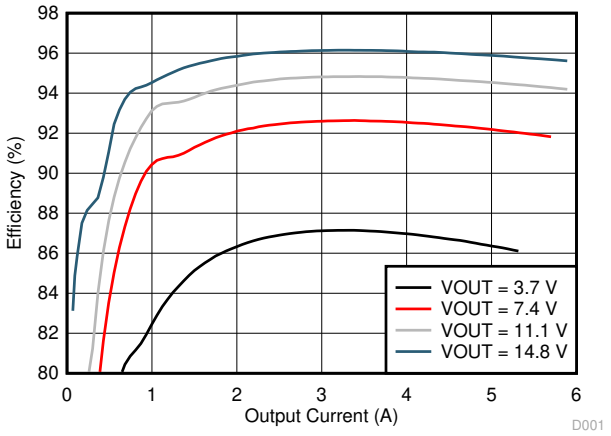
Figure 8-5. System Efficiency



VIN = 12 V

Figure 8-6. System Efficiency

8.7 Typical Characteristics (continued)



VIN = 20 V

Figure 8-7. System Efficiency

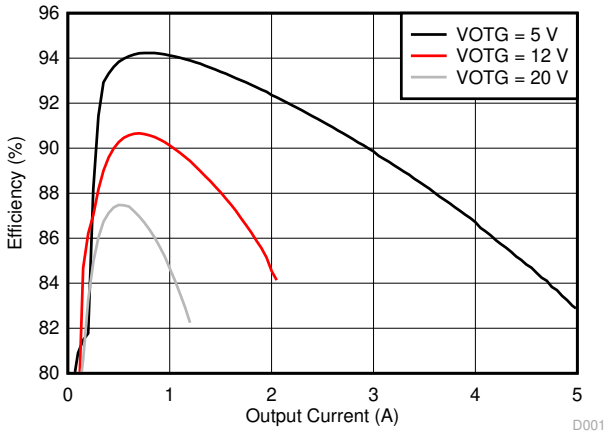


Figure 8-8. OTG Efficiency with 1S Battery

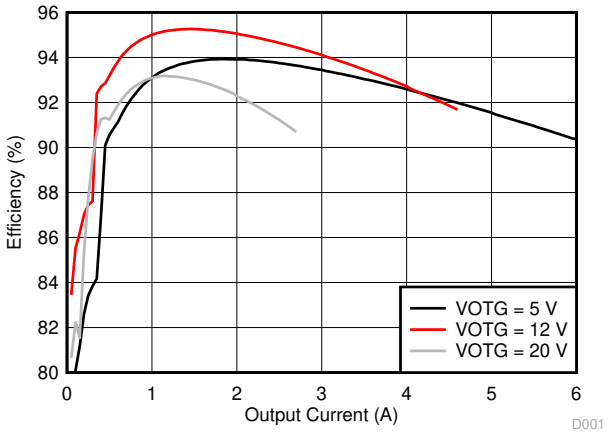


Figure 8-9. OTG Efficiency with 2S Battery

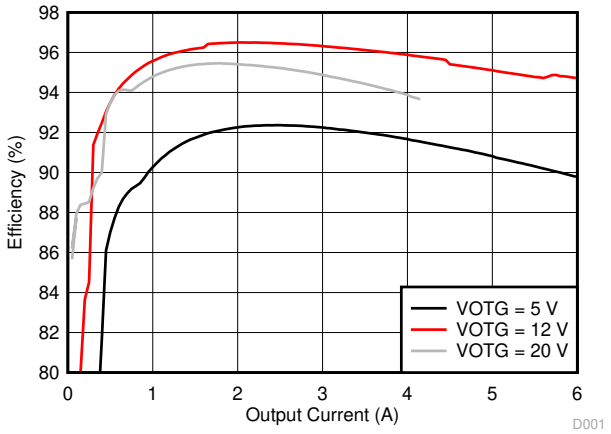


Figure 8-10. OTG Efficiency with 3S Battery

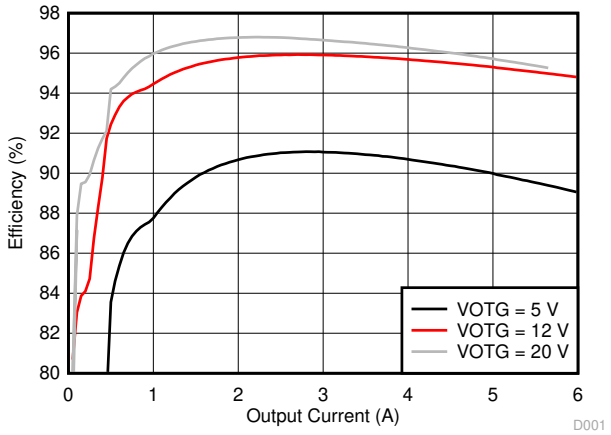


Figure 8-11. OTG Efficiency with 4S Battery

9 Detailed Description

9.1 Overview

The BQ25713/BQ25713B is a Narrow VDC buck-boost charger controller for portable electronics such as notebook, detachable, ultrabook, tablet and other mobile devices with rechargeable batteries. It provides seamless transition among different converter operation modes (buck, boost, or buck boost), fast transient response, and high light load efficiency.

BQ25713/BQ25713B supports wide range of power sources, including USB PD ports, legacy USB ports, traditional ACDC adapters, etc. It takes input voltage from 3.5 V to 24 V, and charges battery of 1-4 series. In the absence of an input source, BQ25713/BQ25713B supports USB On-the-Go (OTG) function from 1-4 cell battery to generate adjustable 3 V ~ 20.8 V at USB port with 8mV resolution. The OTG output voltage transition slew rate can be configurable, which complies with the USB Power Delivery 3.0 PPS specifications.

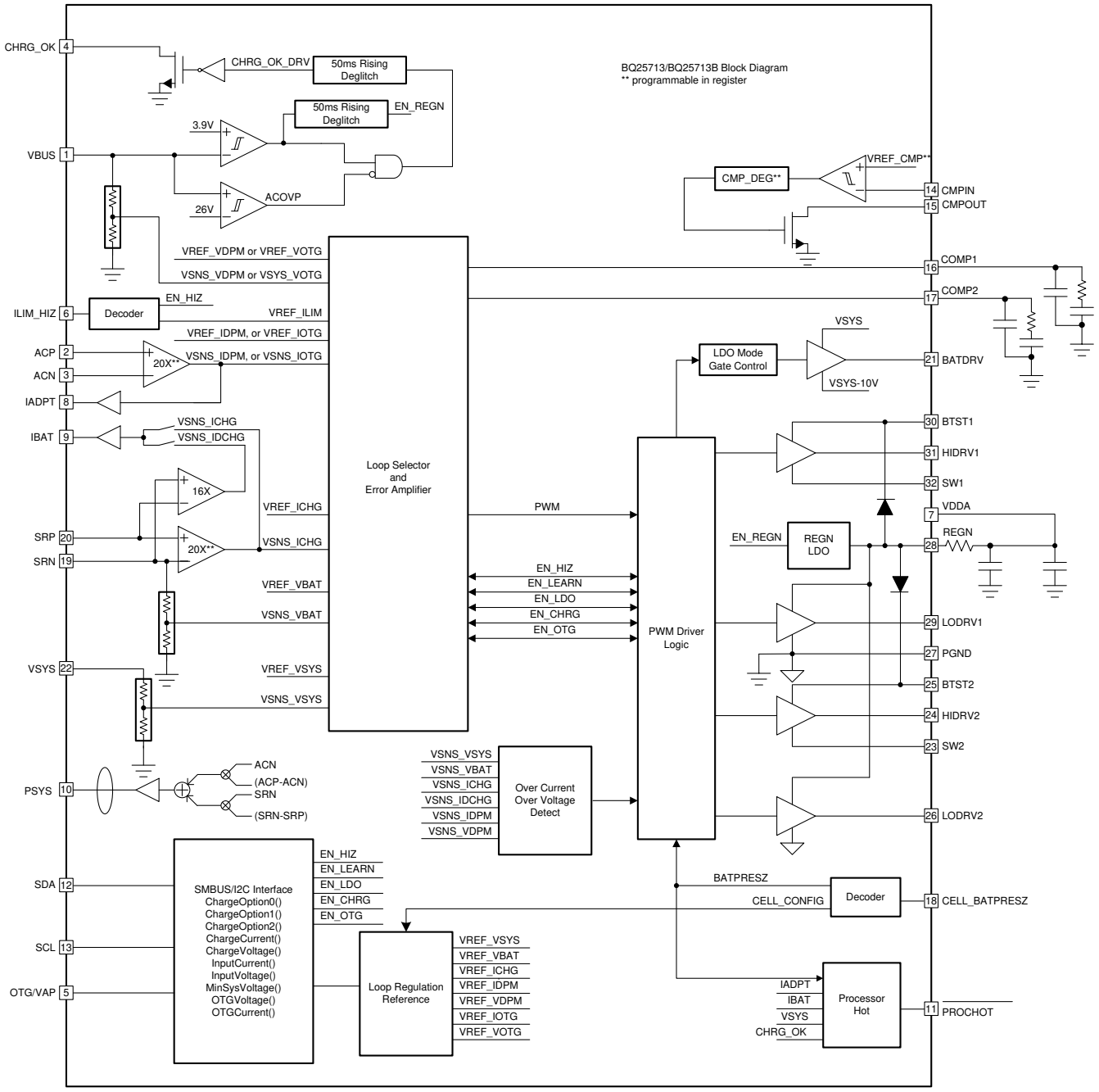
When only the battery powers the system and no external load is connected to the USB OTG port, BQ25713/BQ25713B provides the Vmin Active Protection (VAP) feature. In the VAP operation, BQ25713/BQ25713B first charges up the voltage of the input decoupling capacitors at VBUS to store a certain amount of energy. During the system peak power spike, the huge current drawn from the battery introduces a larger voltage drop across the impedance from the battery to the system. Then the energy stored in the input capacitors will supplement the system, to prevent the system voltage from drooping below the minimum system voltage and leading the system to black screen. This VAP is designed to absorb system power peaks during the periods of high demand to improve the system turbo performance, which is highly recommended by Intel for the platforms with 1S~2S battery.

BQ25713/BQ25713B features Dynamic Power Management (DPM) to limit the input power and avoid AC adapter overloading. During battery charging, as the system power increases, the charging current will reduce to maintain total input current below adapter rating. If system power demand temporarily exceeds adapter rating, BQ25713/BQ25713B supports NVDC architecture to allow battery discharge energy to supplement system power. For details, refer to Section 9.6.5.1.

In order to be compliant with an Intel IMVP8 / IMVP9 compliant system, BQ25713/BQ25713B includes PSYS function to monitor the total platform power from adapter and battery. Besides PSYS, it provides both an independent input current buffer (IADPT) and a battery current buffer (IBAT) with highly accurate current sense amplifiers. If the platform power exceeds the available power from adapter and battery, a $\overline{\text{PROCHOT}}$ signal is asserted to CPU so that the CPU optimizes its performance to the power available to the system.

The I^2C controls input current, charge current and charge voltage registers with high resolution, high accuracy regulation limits. It also sets the $\overline{\text{PROCHOT}}$ timing and threshold profile to meet system requirements.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-Up from Battery Without DC Source

If only battery is present and the voltage is above V_{VBAT_UVLOZ}, the BATFET turns on and connects battery to system. By default, the charger is in low power mode (REG0x01[7] = 1) with lowest quiescent current. The LDO stays off. When device moves to performance mode (REG0x01[7] = 0), The host can enable IBAT buffer through I^2C to monitor discharge current. The PSYS, $\overline{PROCHOT}$ or independent comparator also can be enabled by the host through the I^2C commands. In performance mode, the REGN LDO is always available to provide an accurate reference for the other features.

9.3.2 Vmin Active Protection (VAP) when Battery only Mode

In VAP mode operation, the buck-boost charger delivers the energy from the battery to charge the voltage of the input decoupling capacitors (VBUS) as high as possible (like 20V). The system peak power pulse for a 2S1P or 1S2P system can be as high as 100W if the SoC and motherboard systems spikes coincide. These spikes are expected to be very rare, but possible. During these high power spikes, the charger is expected to supplement the battery (drawing the power from the charger's input decoupling capacitors) to prevent the system voltage from drooping. VAP allows the SoC to set much higher peak power levels to the SoC, thus provides for much better Turbo performance.

Follows the steps below to enter VAP operation.:

1. Set the voltage limit to charge VBUS in REG0x07/06().
2. Set the current limit to charge VBUS in REG0x09/08() and REG0x39[7:2].
3. Set the system voltage regulation point in REG0x0D[5:0], when the input cap supplements battery, the VSYS_MIN regulation loop will maintain VSYS at this regulation point.
4. Set the PROCHOT_VSYS_TH1 threshold to trigger the VAP discharging VBUS in REG0x36[7:4].
5. Set the PROCHOT_VSYS_TH2 threshold to assert /PROCHOT active low signal to throttle SoC in REG0x36[3:2].
6. Enable the VAP mode by setting REG0x34[5] = 0, REG0x35[4] = 0, and pulling the OTG/VAP pin to high.

To exit VAP mode, the host should write either REG0x34[5] = 1 or pull low the OTG/VAP pin to low.

Any regular fault conditions of the charger in VAP mode will reset REG0x34[5] = 1, and the charger will exit VAP mode automatically.

9.3.3 Power-Up From DC Source

When an input source plugs in, the charger checks the input source voltage to turn on LDO and all the bias circuits. It sets the input current limit before the converter starts.

The power-up sequence from DC source is as follows:

1. 50 ms after VBUS above V_{VBUS_CONVEN}, enable 6 V LDO and CHRG_OK goes HIGH
2. VBUS qualification is executed 50 ms after VBUS first rises above VVBUS_UVLOZ. If

   V_{VBUS_UVLOZ} < VBUS < V_{VBUS_CONVEN} then charger fails VBUS qualification, and the charger will re-qualify VBUS every 2s.
3. Input voltage and current limit setup
4. Battery CELL configuration
5. 150 ms after VBUS above V_{VBUS_CONVEN}, converter powers up.

9.3.3.1 CHRG_OK Indicator

CHRG_OK is an active HIGH open drain indicator. It indicates the charger is in normal operation when the following conditions are valid:

- VBUS is above V_{VBUS_CONVEN}
- VBUS is below V_{ACOV}
- No MOSFET/inductor, or over-voltage, over-current, thermal shutdown fault

9.3.3.2 Input Voltage and Current Limit Setup

After CHRG_OK goes HIGH, the charger sets default input current limit in REG0x0F/0E() to 3.25 A. The actual input current limit being adopted by the device is the lower setting of REG0x0F/0E() and ILIM_HIZ pin.

Charger initiates a VBUS voltage measurement without any load (VBUS at no load) right before the converter is enabled. The default VINDPM threshold is VBUS at no load – 1.28 V.

After input current and voltage limits are set, the charger device is ready to power up. The host can always program the input current and voltage limit after the charger being powered up, based on the input source type.

9.3.3.3 Battery Cell Configuration

CELL_BATPRESZ pin is biased with a resistor divider from REGN to CELL_BATPRESZ to GND. After VDDA LDO is activated, the device detects the battery configuration through CELL_BATPRESZ pin bias voltage. Refer to Table 9-1 for cell setting thresholds.

Table 9-1. Battery Cell Configuration

CELL COUNT	PIN VOLTAGE w.r.t. VDDA	BATTERY VOLTAGE (REG0x05/04)	SYSOVP
4S	75%	16.800 V	19.5 V
3S	55%	12.592 V	19.5 V
2S	40%	8.400 V	12 V
1S	25%	4.192 V	5 V

9.3.3.4 Device Hi-Z State

The charger enters Hi-Z mode when ILIM_HIZ pin voltage is below 0.4 V or REG0x35[7] is set to 1. During Hi-Z mode, the input source is present, and the charger is in the low quiescent current mode with REGN LDO enabled.

9.3.4 USB On-The-Go (OTG)

The device supports USB OTG operation to deliver power from the battery to other portable devices through USB port. The OTG mode output voltage is set in REG0x07/06(). The OTG mode output current is set in REG0x09/08(). The OTG operation can be enabled if the conditions are valid:

- Valid battery voltage is set REG0x05/04(), the battery voltage should not trip the BATOVP threshold, otherwise, the converter will stop switching.
- OTG output voltage is set in REG0x07/06() and REG0x34[2], if REG0x34[2] = 0, the VOTG digital DAC is offset by 1.28V to achieve higher range from 4.28V~20.8V, if REG0x34[2] = 1, the VOTG digital DAC is from 3V to 19.52V.
- OTG output current is set in REG0x09/08().
- EN_OTG pin is HIGH, REG0x35[4] = 1 and REG0x34[5] = 1.
- VBUS is below $V_{VBUS\_CONVENZ}$.
- 10 ms after the above conditions are valid, converter starts and VBUS ramps up to target voltage. CHRG_OK pin goes HIGH if REG0x01[3] = 1.

9.3.5 Converter Operation

The charger employs a synchronous buck-boost converter that allows charging from a standard 5-V or a high-voltage power source. The charger operates in buck, buck-boost and boost mode. The buck-boost can operate uninterruptedly and continuously across the three operation modes.

Table 9-2. MOSFET Operation

MODE	BUCK	BUCK-BOOST	BOOST
Q1	Switching	Switching	ON
Q2	Switching	Switching	OFF
Q3	OFF	Switching	Switching

Table 9-2. MOSFET Operation (continued)

MODE	BUCK	BUCK-BOOST	BOOST
Q4	ON	Switching	Switching

9.3.5.1 Inductance Detection through IADPT Pin

The charger reads the inductance value through the resistance tied to IADPT pin before the converter starts up. The resistances recommended for 1uH, 2.2uH and 3.3uH inductance are 93kΩ, 137kΩ and 169kΩ, respectively. A surface mount chip resistor with ±3% or better tolerance must to be used for an accurate inductance detection.

Table 9-3. Inductor Detection through IADPT Resistance

INDUCTOR IN USE	RESISTOR ON IADPT PIN
1 µH	93 kΩ
2.2 µH	137 kΩ
3.3 µH	169 kΩ

9.3.5.2 Continuous Conduction Mode (CCM)

With sufficient charge or system current, the inductor current does not cross 0 A, which is defined as CCM. The controller starts a new cycle with ramp coming up from 200 mV. As long as the error amplifier output voltage is above the ramp voltage, the high-side MOSFET (HSFET) stays on. When the ramp voltage exceeds error amplifier output voltage, HSFET turns off and low-side MOSFET (LSFET) turns on. At the end of the cycle, ramp gets reset and LSFET turns off, ready for the next cycle. There is always break-before-make logic during transition to prevent cross-conduction and shoot-through. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM, the inductor current always flows and creates a fixed two-pole system. Having the LSFET turn-on when the HSFET is off keeps the power dissipation low and allows safe charging at high currents.

9.3.5.3 Pulse Frequency Modulation (PFM)

In order to improve converter light-load efficiency, BQ25713/BQ25713B switches to PFM operation at light load. The effective switching frequency will decrease accordingly when system load decreases. The minimum frequency can be limit to 25 kHz when the OOA feature is enabled (ChargeOption0() bit[10]=1).

9.3.6 Current and Power Monitor

9.3.6.1 High-Accuracy Current Sense Amplifier (IADPT and IBAT)

As an industry standard, a high-accuracy current sense amplifier (CSA) is used to monitor the charger input current during forward charging mode, or output current during OTG mode (IADPT) and the battery charge/discharge current (IBAT). IADPT voltage is 20× or 40× the differential voltage across ACP and ACN. IBAT voltage is 8x/16× (during charging), or 8×/16× (during discharging) of the differential across SRP and SRN. After input voltage or battery voltage is above UVLO, IADPT output becomes valid. To lower the voltage on current monitoring, a resistor divider from CSA output to GND can be used and accuracy over temperature can still be achieved.

- $V_{(IADPT)}$ = 20 or 40 × ($V_{(ACP)}$ – $V_{(ACN)}$) during forward mode, or 20 or 40 × ($V_{(ACN)}$ – $V_{(ACP)}$) during reverse OTG mode.
- $V_{(IBAT)}$ = 8 or 16 × ($V_{(SRP)}$ – $V_{(SRN)}$) for battery charging current.
- $V_{(IBAT)}$ = 8 or 16 × ($V_{(SRN)}$ – $V_{(SRP)}$) for battery discharging current.

A maximum 100-pF capacitor is recommended to connect on the output for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay. The CSA output voltage is clamped at 3.3 V.

9.3.6.2 High-Accuracy Power Sense Amplifier (PSYS)

The charger monitors total system power. During forward mode, the input adapter powers system. During reverse OTG mode, the battery powers the system and VBUS output. The ratio of PSYS pin output current and total system power, K_{PSYS}, can be programmed in REG0x31[1] with default 1 µA/W. The input and charge sense

resistors (RAC and RSR) are selected in REG0x31[3:2]. PSYS voltage can be calculated with Equation 1, where I_{IN}>0 I_{BAT}<0 when the charger is in forward charging with an adapter connected, and I_{BAT}>0 when the battery is in discharging mode.

$$V_{PSYS} \quad R_{PSYS} \times K_{PSYS} (V_{ACP} \times I_{IN} + V_{BAT} \times I_{BAT}) \tag{1}$$

For proper PSYS functionality, RAC and RSR values are limited to 10 mΩ and 20 mΩ.

To minimize the quiescent current, the PSYS function is disabled by default. It can be enabled by setting REG0x31[4] = 1.

9.3.7 Input Source Dynamic Power Manage

Refer to Section 9.6.6.

9.3.8 Two-Level Adapter Current Limit (Peak Power Mode)

Usually adapter can supply current higher than DC rating for a few milliseconds to tens of milliseconds. The charger employs two-level input current limit, or peak power mode, to fully utilize the overloading capability and minimize battery discharge during CPU turbo mode. Peak power mode is enabled in REG0x33[5:4]. The DC current limit, or I_{LIM1}, is the same as adapter DC current, set in REG0x0F/0E(). The overloading current, or I_{LIM2}, is set in REG0x37[7:3], as a percentage of I_{LIM1}.

When the charger detects input current surge and battery discharge due to load transient (both the adapter and battery support the system together), or when the charger detects the system voltage starts to drop due to load transient (only the adapter supports the system), the charger will first apply I_{LIM2} for T_{OVLD} in REG0x33[7:6], and then I_{LIM1} for up to T_{MAX} – T_{OVLD} time. T_{MAX} is programmed in REG0x33[1:0]. After T_{MAX}, if the load is still high, another peak power cycle starts. Charging is disabled during T_{MAX},; once T_{MAX}, expires, charging continues. If T_{OVLD} is programmed to be equal to T_{MAX}, then peak power mode is always on.

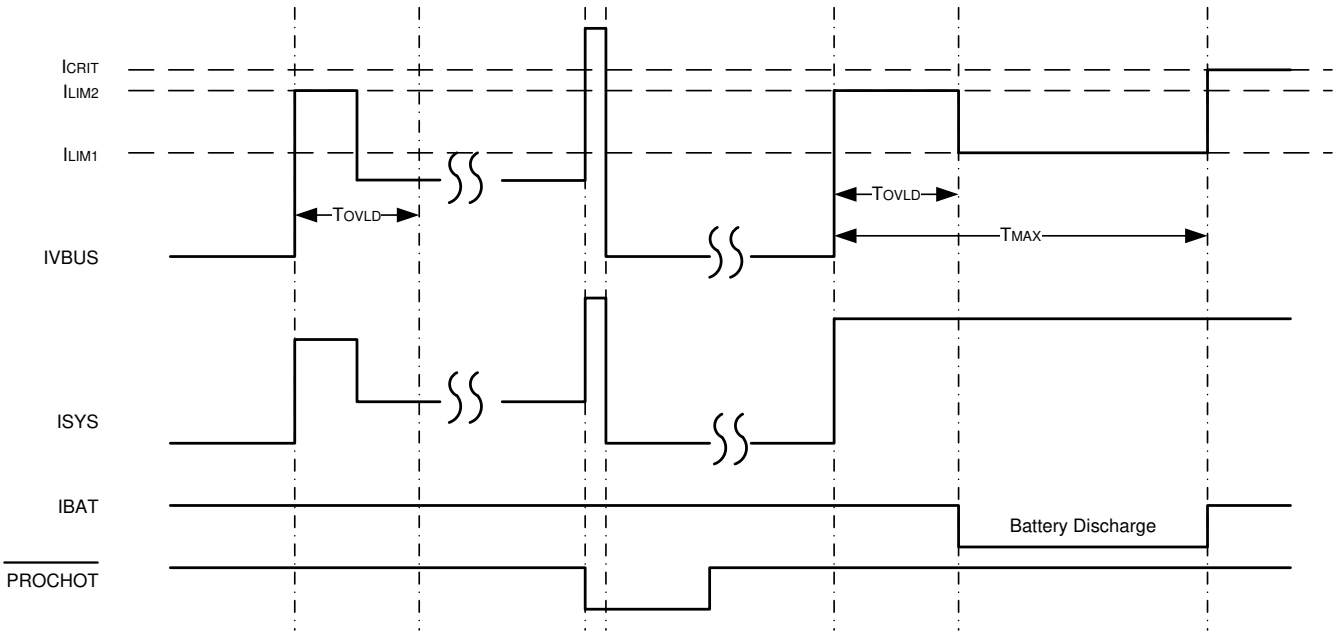


Figure 9-1. Two-Level Adapter Current Limit Timing Diagram

9.3.9 Processor Hot Indication

When CPU is running turbo mode, the system peak power may exceed available power from adapter and battery together. The adapter current and battery discharge peak current, or system voltage drop is an indication that system power is too high. The charger processor hot function monitors these events, and $\overline{\text{PROCHOT}}$ pulse is asserted if the system power is too high. Once CPU receives $\overline{\text{PROCHOT}}$ pulse from charger, it slows down to reduce system power. The events monitored by the processor hot function includes:

- ICRIT: adapter peak current, as 110% of I_{LIM2}
- INOM: adapter average current (110% of input current limit)
- IDCHG: battery discharge current
- VSYS: system voltage on VSYS
- Adapter Removal: upon adapter removal (CHRG_OK pin HIGH to LOW)
- Battery Removal: upon battery removal (CELL_BATPRESZ pin goes LOW)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW)
- VDPM: VBUS lower than 80%/90%/100% of VINDPM threshold.
- EXIT_VAP: Every time when the charger exits VAP mode.

The threshold of ICRIT, IDCHG, VSYS or VDPM, and the deglitch time of ICRIT, INOM, IDCHG or CMPOUT are programmable through I^2C. Except the PROCHOT_EXIT_VAP is always enabled, the other triggering events can be individually enabled in REG0x38[7:0]. When any enabled event in $\overline{\text{PROCHOT}}$ profile is triggered, $\overline{\text{PROCHOT}}$ is asserted low for a single pulse with minimal width programmable in REG0x23[5:4]. At the end of the single pulse, if the $\overline{\text{PROCHOT}}$ event is still active, the pulse gets extended until the event is removed.

If the $\overline{\text{PROCHOT}}$ pulse extension mode is enabled by setting REG0x23[6] = 1, the $\overline{\text{PROCHOT}}$ pin will be kept as low until host writes REG0x23[3]21[11] = 0, even if the triggering event has been removed.

If the PROCHOT_VDPM or PROCHOT_EXIT_VAP is triggered, $\overline{\text{PROCHOT}}$ pin will always stay low until the host clears it, no matter the $\overline{\text{PROCHOT}}$ is in one pulse mod or in extended mode.

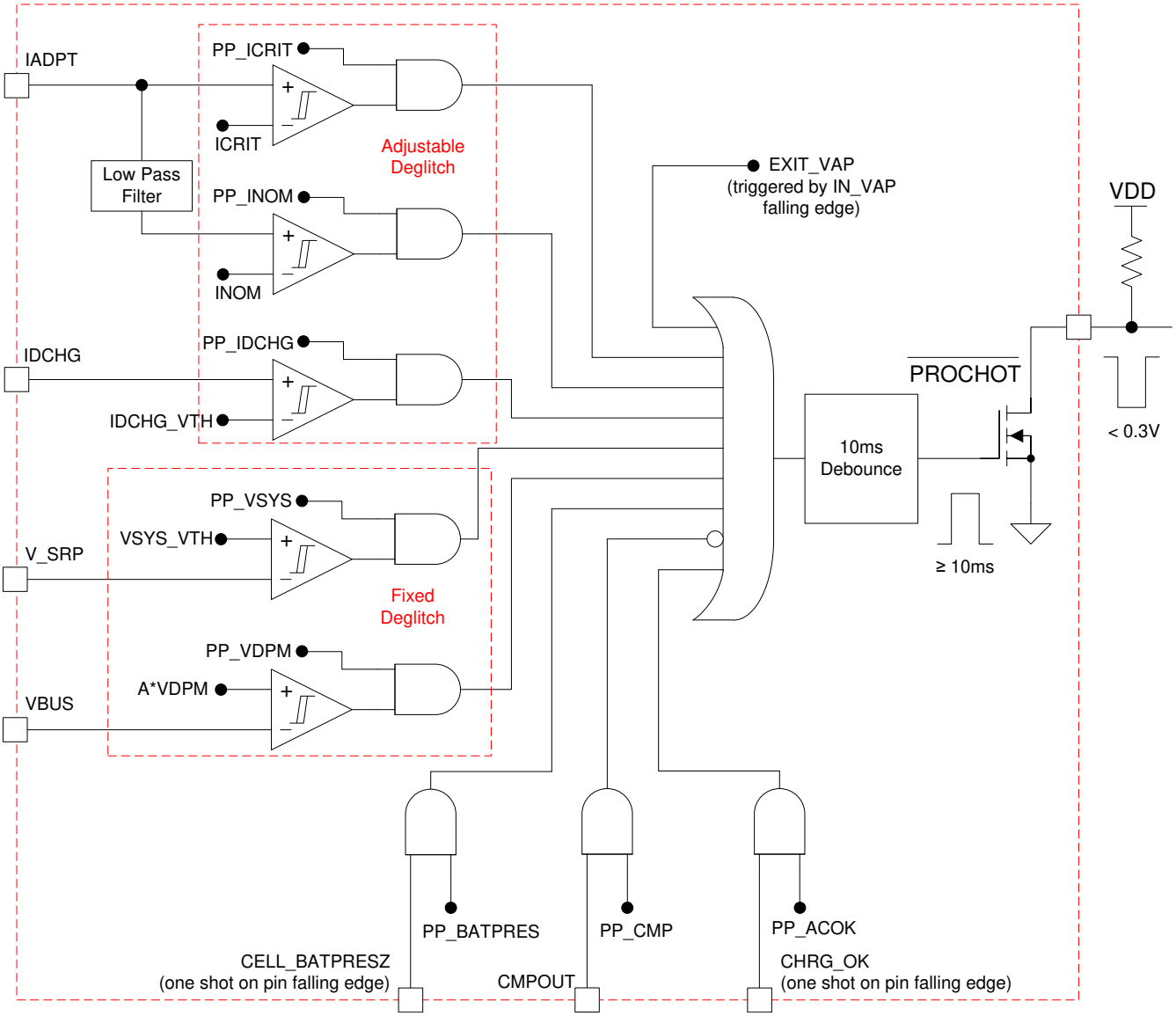


Figure 9-2. $\overline{\text{PROCHOT}}$ Profile

9.3.9.1 $\overline{\text{PROCHOT}}$ During Low Power Mode

During low power mode (REG0x01[7] = 1), the charger offers a low power $\overline{\text{PROCHOT}}$ function with very low quiescent current consumption (~150uA), which uses the independent comparator to monitor the system voltage, and assert $\overline{\text{PROCHOT}}$ to CPU if the system power is too high.

Below lists the register setting to enable $\overline{\text{PROCHOT}}$ monitoring system voltage in low power mode.

- REG0x01[7] = 1 to enable charger low power mode.
- REG0x38[7:0] = 00h
- REG0x30[6:4] = 100
- Independent comparator threshold is always 1.2 V
- When REG0x31[5] = 1, charger monitors system voltage. Connect CMPIN to voltage proportional to system. $\overline{\text{PROCHOT}}$ triggers from HIGH to LOW when CMPIN voltage rises above 1.2 V.

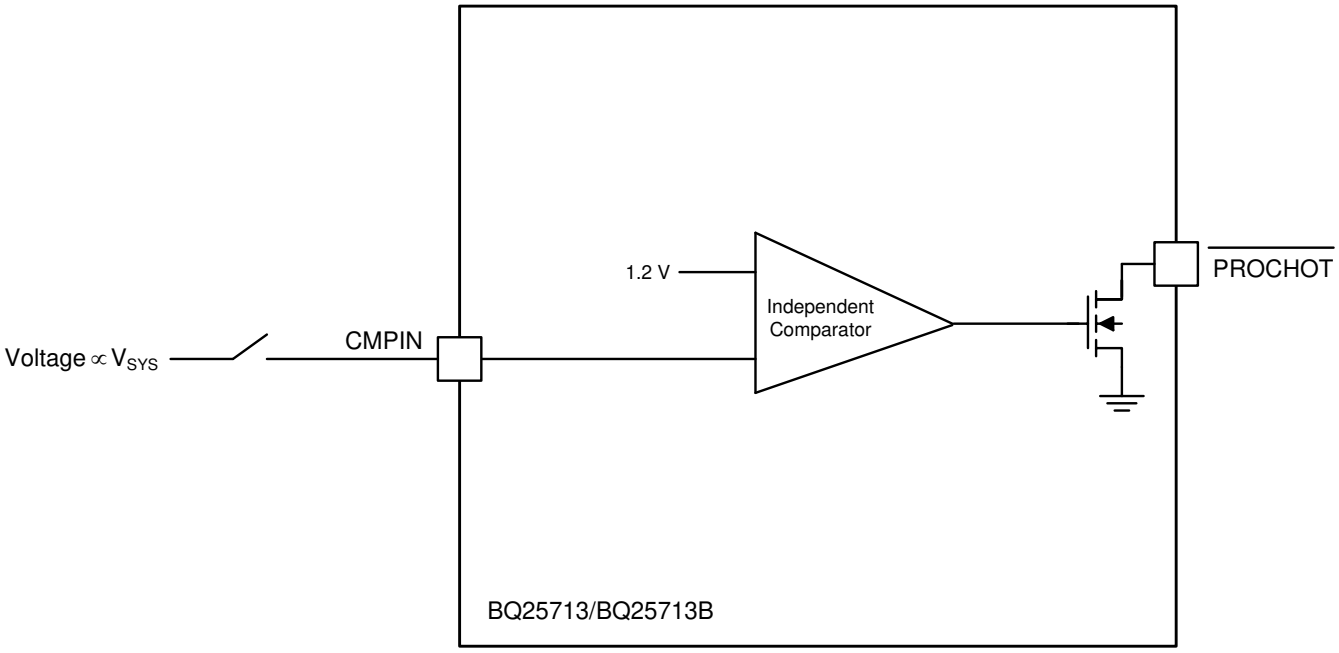


Figure 9-3. $\overline{\text{PROCHOT}}$ Low Power Mode Implementation

9.3.9.2 $\overline{\text{PROCHOT}}$ Status

REG0x22[7:0] and REG0x23[0] reports which event in the profile triggers $\overline{\text{PROCHOT}}$ if the corresponding bit is set to 1. The status bit can be reset back to 0 after it is read by host, when the current $\overline{\text{PROCHOT}}$ event is not active any more.

Assume there are two $\overline{\text{PROCHOT}}$ events, event A and event B. Event A triggers $\overline{\text{PROCHOT}}$ first, but event B is also active. Both status bits will be HIGH. At the end of the 10 ms $\overline{\text{PROCHOT}}$ pulse, if any of the $\overline{\text{PROCHOT}}$ event is still active (either A or B), the $\overline{\text{PROCHOT}}$ pulse is extended.

9.3.10 Device Protection

9.3.10.1 Watchdog Timer

The charger includes watchdog timer to terminate charging if the charger does not receive a write MaxChargeVoltage() or write ChargeCurrent() command within 175 s (adjustable via REG0x01[6:5]). When watchdog timeout occurs, all register values are kept unchanged except ChargeCurrent() resets to zero. Battery charging is suspended. Write MaxChargeVoltage() or write ChargeCurrent() commands must be re-sent to reset watchdog timer and resume charging. Writing REG0x01[6:5] = 00 to disable watchdog timer also resumes charging.

9.3.10.2 Input Overvoltage Protection (ACOV)

The charger has fixed ACOV voltage. When VBUS pin voltage is higher than ACOV, it is considered as adapter over voltage. CHRG_OK will be pulled low, and converter will be disabled. As system falls below battery voltage, BATFET will be turned on. When VBUS pin voltage falls below ACOV, it is considered as adapter voltage returns back to normal voltage. CHRG_OK is pulled high by external pull up resistor. The converter resumes if enable conditions are valid.

9.3.10.3 Input Overcurrent Protection (ACOC)

If the input current exceeds the 1.33× or 2× (REG0x32[2]) of I_{LIM2_VTH} (REG0x37[7:3]) set point, converter stops switching. After 300 ms, converter starts switching again.

9.3.10.4 System Overvoltage Protection (SYSOVP)

When the converter starts up, BQ25713/BQ25713B reads CELL pin configuration and sets MaxChargeVoltage() and SYSOVP threshold (1s – 5 V, 2s – 12 V, 3s/4s – 19.5 V). Before REGx05/04() is written by the host, the

battery configuration will change with CELL pin voltage. When SYSOVP happens, the device latches off the converter. REG0x20[4] is set to 1. The user can clear latch-off by either writing 0 to the SYSOVP bit or removing and plugging in the adapter again. After latch-off is cleared, the converter starts again.

9.3.10.5 Battery Overvoltage Protection (BATOVP)

Battery over-voltage may happen when battery is removed during charging or the user plugs in a wrong battery. The BATOVP threshold is 104% (1 s) or 102% (2 s to 4 s) of regulation voltage set in REG0x05/04().

9.3.10.6 Battery Short

If BAT voltage falls below SYSMIN during charging, the maximum current is limited to 384 mA.

9.3.10.7 System Short Hiccup Mode

VSYS pin is monitoring the system voltage, when Vsys is lower than 2.4V, after 2ms deglitch time, the charger will be shut down for 500ms. The charger will restart for 10ms and measure Vsys again, if it is still lower than 2.4V, the charger will be shut down again. This hiccup mode will be tried continuously, if the charger restart is failed for 7 times in 90 second, the charger will be latched off. REG0x20[3] will be set to 1 to report a system short fault. The charger only can be enabled again once the host writes REG0x20[3]= 0.

The charger system short hiccup mode can be disabled by writing REG0x00[6]= 1.

9.3.10.8 Thermal Shutdown (TSHUT)

The WQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As added level of protection, the charger converter turns off for self-protection whenever the junction temperature exceeds the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shut down, the LDO current limit is reduced to 16 mA and REGN LDO stays off. When the temperature falls below 135°C, charge can be resumed with soft start.

9.4 Device Functional Modes

9.4.1 Forward Mode

When input source is connected to VBUS, BQ25713/BQ25713B is in forward mode to regulate system and charge battery.

9.4.1.1 System Voltage Regulation with Narrow VDC Architecture

BQ25713/BQ25713B employs Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by MinSystemVoltage(). Even with a deeply depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode).

As the battery voltage rises above the minimum system voltage, BATFET is fully on when charging or in supplement mode and the voltage difference between the system and battery is the VDS of BATFET. System voltage is regulated 160 mV above battery voltage when BATFET is off (no charging or no supplement current).

The $\overline{\text{BATDRV}}$ pin is only able to drive a battery MOSFET with Ciss lower than 5nF. The Ciss in the range of 1nF~3nF is recommended.

See Section 9.6.5.1 for details on system voltage regulation and register programming.

9.4.1.2 Battery Charging

BQ25713/BQ25713B charges 1-4 cell battery in constant current (CC), and constant voltage (CV) mode. Based on CELL_BATPREZ pin setting, the charger sets default battery voltage 4.2V/cell to ChargeVoltage(), or REG0x05/04(). According to battery capacity, the host programs appropriate charge current to ChargeCurrent(), or REG0x03/02(). When battery is full or battery is not in good condition to charge, host terminates charge by setting REG0x00[0] to 1, or setting ChargeCurrent() to zero.

See Section 9.3 for details on register programming.

9.4.2 USB On-The-Go

BQ25713/BQ25713B supports USB OTG functionality to deliver power from the battery to other portable devices through USB port (reverse mode). The OTG output voltage is compliant with USB PD specification, including 5 V, 9 V, 15 V, and 20 V. The output current regulation is compliant with USB type C specification, including 500 mA, 1.5 A, 3 A and 5 A.

Similar to forward operation, the device switches from PWM operation to PFM operation at light load to improve efficiency.

9.4.3 Pass Through Mode (PTM)

When the system is in the sleep mode or light load condition, the charger can be operated in the pass through mode to improve the light load efficiency. In TI patented pass through mode (PTM), the Buck and Boost high side FETs are both turned on, while the Buck and Boost low side FETs are both turned off. The input power is directly passed through the charger to the system. The switching losses of MOSFETs and the inductor core loss are saved.

Device will be transition from normal Buck-Boost operation to PTM operation by:

- Set REG0x32[7] = 0, to disable the EN_EXITILIM.
- Set REG0x31[0] = 1.
- Set REG0x30[2] = 1.
- Ground ILIM_HIZ pin.

Device will transition out of PTM mode with host control by:

- Set REG0x30[2] = 0.
- Pull ILIM_HIZ pin to high.
- Device exits PTM to buck-boost operation if tripping VINDPM.
- Device exits PTM to buck-boost operation under fault conditions

9.5 Programming

The charger supports battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Section 9.5.1. The I2C address is D6h. The ManufacturerID and DeviceID registers are assigned identify the charger device. The ManufacturerID register command always returns 40h.

9.5.1 I^2C Serial Interface

The BQ25713/BQ25713B uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address D6h, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG3A. The I^2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

9.5.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

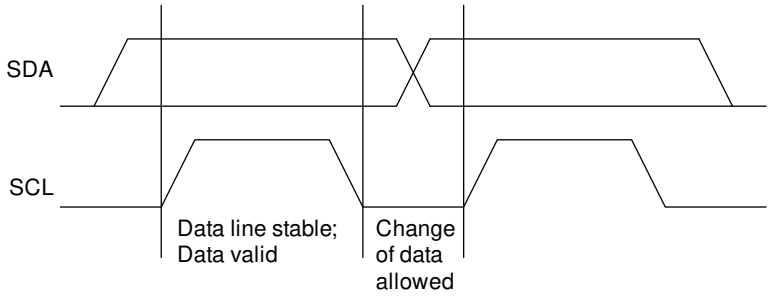


Figure 9-4. Bit Transfer on the I²C Bus

9.5.1.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

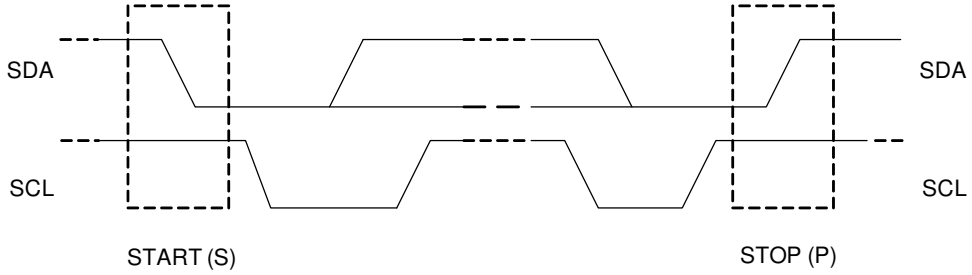


Figure 9-5. START and STOP Conditions

9.5.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

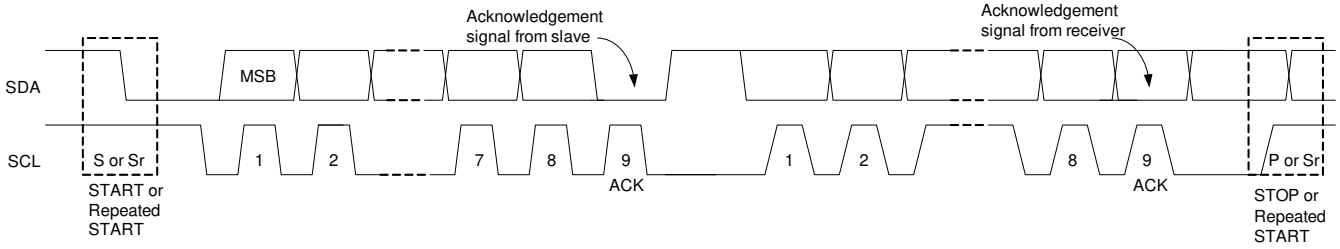


Figure 9-6. Data Transfer on the I²C Bus

9.5.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

9.5.1.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

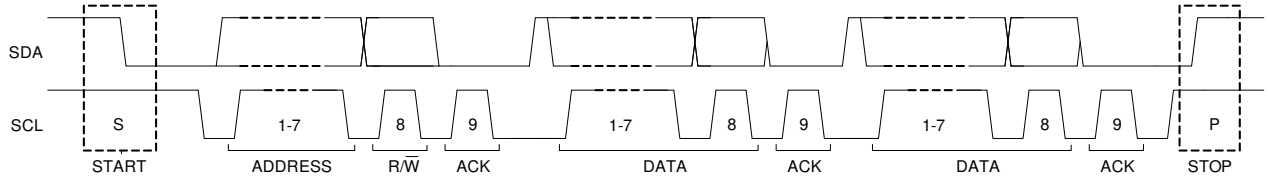


Figure 9-7. Complete Data Transfer

9.5.1.6 Single Read and Write

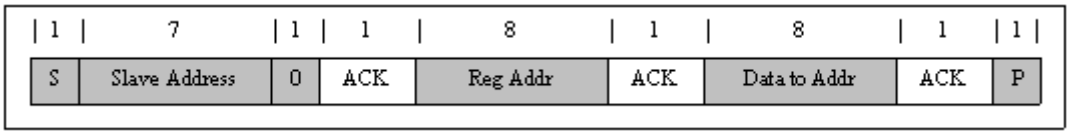


Figure 9-8. Single Write

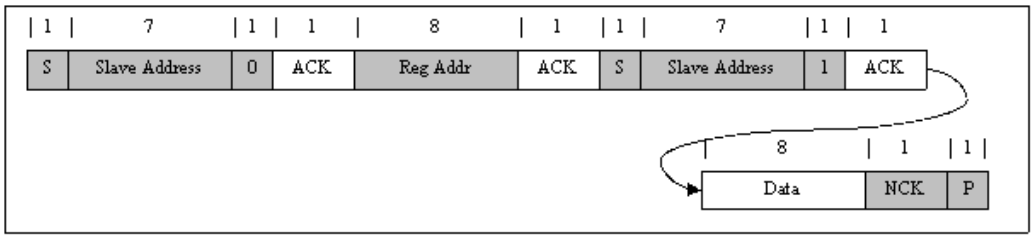


Figure 9-9. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

9.5.1.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write.

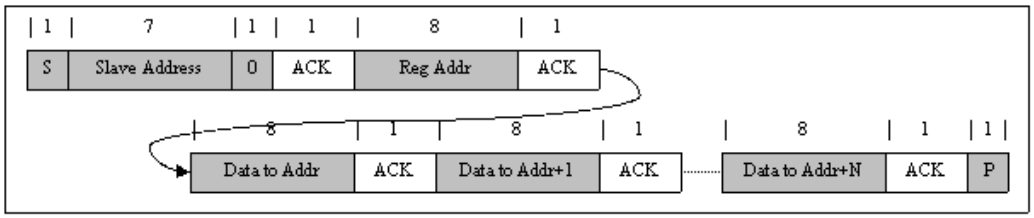


Figure 9-10. Multi Write

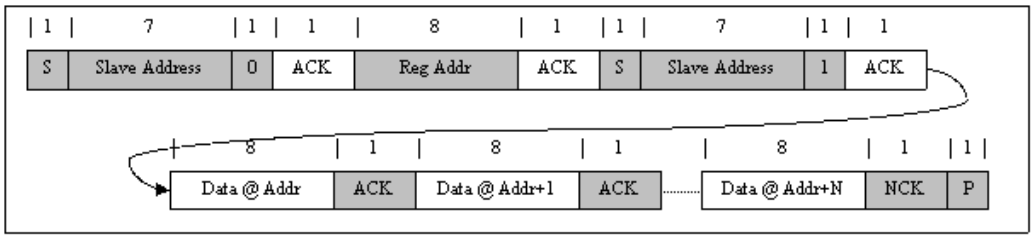


Figure 9-11. Multi Read

9.5.1.8 Write 2-Byte I²C Commands

A few I²C commands combine two 8-bit registers together to form a complete value. These commands include:

- ChargeCurrent()
- MaxChargeVoltage()
- IIN_DPM()
- OTGVoltage()
- InputVoltage()

Host has to write LSB command followed by MSB command. No other command can be inserted in between these two writes. The charger waits for the complete write to the two registers to decide whether to accept or ignore the new value.

After the completion of LSB and MSB bytes, the two bytes will be updated at the same time. If host writes MSB byte first, the command will be ignored. If the time between write of LSB and MSB bytes exceeds watchdog timer, both the LSB and MSB commands will be ignored.

9.6 Register Map

Table 9-4. Charger Command Summary

I²C ADDR (MSB/LSB)	REGISTER NAME	TYPE	DESCRIPTION	LINKS
01/00h	ChargeOption0()	R/W	Charge Option 0	Go
03/02h	ChargeCurrent()	R/W	7-bit charge current setting LSB 64 mA, Range 0 mA – 8128 mA	Go
05/04h	MaxChargeVoltage()	R/W	12-bit charge voltage setting LSB 8 mV, Default: 1S-4200mV, 2S-8400mV, 3S-12600mV, 4S-16800mV	Go
31/30h	ChargeOption1()	R/W	Charge Option 1	Go
33/32h	ChargeOption2()	R/W	Charge Option 2	Go
35/34h	ChargeOption3()	R/W	Charge Option 3	Go
37/36h	ProchotOption0()	R/W	$\overline{\text{PROCHOT}}$ Option 0	Go
39/38h	ProchotOption1()	R/W	$\overline{\text{PROCHOT}}$ Option 1	Go
3B/3Ah	ADCOption()	R/W	ADC Option	Go
21/20h	ChargerStatus()	R	Charger Status	Go
23/22h	ProchotStatus()	R	Prochot Status	Go
25/24h	IIN_DPM()	R	7-bit input current limit in use LSB: 50 mA, Range: 50 mA - 6400 mA	Go
27/26h	ADCVBUS/PSYS()	R	8-bit digital output of input voltage, 8-bit digital output of system power PSYS: Full range: 3.06 V, LSB: 12 mV VBUS: Full range: 3.2 V - 19.52 V, LSB 64 mV	Go
29/28h	ADCIBAT()	R	8-bit digital output of battery charge current, 8-bit digital output of battery discharge current ICHG: Full range 8.128 A, LSB 64 mA IDCHG: Full range: 32.512 A, LSB: 256 mA	Go

Table 9-4. Charger Command Summary (continued)

I²C ADDR (MSB/LSB)	REGISTER NAME	TYPE	DESCRIPTION	LINKS
2B/2Ah	ADCIINCMPIN()	R	8-bit digital output of input current, 8-bit digital output of CMPIN voltage POR State - IIN: Full range: 12.75 A, LSB 50 mA CMPIN: Full range 3.06 V, LSB: 12 mV	Go
2D/2Ch	ADCVSYSVBAT()	R	8-bit digital output of system voltage, 8-bit digital output of battery voltage VSYS: Full range: 2.88 V - 19.2 V, LSB: 64 mV VBAT: Full range : 2.88 V - 19.2 V, LSB 64 mV	Go
07/06h	OTGVoltage()	R/W	12-bit OTG voltage setting LSB 8 mV, Range: 3000 mV – 20800 mV	Go
09/08h	OTGCurrent()	R/W	7-bit OTG output current setting LSB 50 mA, Range: 0 A – 6350 mA	Go
0B/0Ah	InputVoltage()	R/W	8-bit input voltage setting LSB 64 mV, Range: 3200 mV – 19520 mV	Go
0D/0Ch	MinSystemVoltage()	R/W	6-Bit minimum system voltage setting LSB: 256 mV, Range: 1024 mV - 16182 mV Default: 1S-3.584V, 2S-6.144V, 3S-9.216V, 4S-12.288V	Go
0F/0Eh	IIN_HOST()	R/W	6-bit Input current limit set by host LSB: 50-mA, Range: 50 mA - 6400 mA	Go
2Eh	ManufacturerID()	R	Manufacturer ID - 0x0040H	Go
2Fh	DeviceID()	R	Device ID	Go

9.6.1 Setting Charge and $\overline{\text{PROCHOT}}$ Options

9.6.1.1 ChargeOption0 Register (I²C address = 01/00h) [reset = E70Eh]

Figure 9-12. ChargeOption0 Register (I²C address = 01/00h) [reset = E70Eh]

7	6	5	4	3	2	1	0
EN_LWPWR	WDTMR_ADJ		IDPM_AUTO_ DISABLE	OTG_ON_ CHRGOK	EN_OOA	PWM_FREQ	PTM_LL_EFF
R/W	R/W		R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved	SYS_SHORT DISABLE	EN_LEARN	IADPT_GAIN	IBAT_GAIN	EN_LDO	EN_IDPM	CHRG_INHIBIT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-5. ChargeOption0 Register (I²C address = 01h) Field Descriptions

I²C 01h	FIELD	TYPE	RESET	DESCRIPTION
7	EN_LWPWR	R/W	1b	Low Power Mode Enable 0b: Disable Low Power Mode. Device in performance mode with battery only. The $\overline{\text{PROCHOT}}$, current/power monitor buffer and comparator follow register setting. 1b: Enable Low Power Mode. Device in low power mode with battery only for lowest quiescent current. The LDO is off. The $\overline{\text{PROCHOT}}$, discharge current monitor buffer, power monitor buffer and independent comparator are disabled. ADC is not available in Low Power Mode.Independent comparator can be enabled by setting either REG0X31()[6] or [5] to 1. <default at POR>
6-5	WDTMR_ADJ	R/W	11b	WATCHDOG Timer Adjust Set maximum delay between consecutive I²C write of charge voltage or charge current command. If device does not receive a write on the REG0x05/04() or the REG0x03/02() within the watchdog time period, the charger will be suspended by setting the REG0x03/02() to 0 mA. After expiration, the timer will resume upon the write of REG0x03/02(), REG0x05/04() or REG0x01[6:5]. The charger will resume if the values are valid. 00b: Disable Watchdog Timer 01b: Enabled, 5 sec 10b: Enabled, 88 sec 11b: Enable Watchdog Timer, 175 sec <default at POR>
4	IDPM_AUTO_ DISABLE	R/W	0b	IDPM Auto Disable When CELL_BATPRESZ pin is LOW, the charger automatically disables the IDPM function by setting EN_IDPM (REG0x00[1]) to 0. The host can enable IDPM function later by writing EN_IDPM bit (REG0x00[1]) to 1. 0b: Disable this function. IDPM is not disabled when CELL_BATPRESZ goes LOW. <default at POR> 1b: Enable this function. IDPM is disabled when CELL_BATPRESZ goes LOW.
3	OTG_ON_ CHRGOK	R/W	0b	Add OTG to CHRG_OK Drive CHRG_OK to HIGH when the device is in OTG mode. 0b: Disable <default at POR> 1b: Enable
2	EN_OOA	R/W	1b	Out-of-Audio Enable 0b: No limit of PFM burst frequency 1b: Set minimum PFM burst frequency to above 25 kHz to avoid audio noise <default at POR>

Table 9-5. ChargeOption0 Register (I²C address = 01h) Field Descriptions (continued)

I²C 01h	FIELD	TYPE	RESET	DESCRIPTION
1	PWM_FREQ	R/W	1b	Switching Frequency Two converter switching frequencies. One for small inductor and the other for big inductor. Recommend 800 kHz with 2.2 µH or 3.3 µH, and 1.2 MHz with 1 µH or 1.5 µH. Host has to set the right PWM frequency after device POR. 0b: 1200 kHz 1b: 800 kHz <default at POR>
0	LOW_PTM_ RIPPLE	R/W	1b	PTM mode input voltage and current ripple reduction 0b: Disable 1b: Enable <default at POR>

Table 9-6. ChargeOption0 Register (I²C address = 00h) Field Descriptions

I²C 00h	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Reserved
6	SYS_SHORT_DISABLE	R/W	0b	To disable the hiccup mode during the system short protection. 0b: When VSYS is short to lower than 2.4V, the charger enters hiccup mode <default at POR> 1b: The charger hiccup mode is disabled during system short fault
5	EN_LEARN	R/W	0b	LEARN function allows the battery to discharge while the adapter is present. It calibrates the battery gas gauge over a complete discharge/charge cycle. When the battery voltage is below battery depletion threshold, the system switches back to adapter input by the host. When CELL_BATPRESZ pin is LOW, the device exits LEARN mode and this bit is set back to 0. 0b: Disable LEARN Mode <default at POR> 1b: Enable LEARN Mode
4	IADPT_GAIN	R/W	0b	IADPT Amplifier Ratio The ratio of voltage on IADPT and voltage across ACP and ACN. 0b: 20× <default at POR> 1b: 40×
3	IBAT_GAIN	R/W	1b	IBAT Amplifier Ratio The ratio of voltage on IBAT and voltage across SRP and SRN 0b: 8× 1b: 16× <default at POR>
2	EN_LDO	R/W	1b	LDO Mode Enable When battery voltage is below minimum system voltage (REG0x0D/0C()), the charger is in pre-charge with LDO mode enabled. 0b: Disable LDO mode, BATFET fully ON. Precharge current is set by battery pack internal resistor. The system is regulated by the MaxChargeVoltage register. 1b: Enable LDO mode, Precharge current is set by the ChargeCurrent register and clamped below 384 mA (2 cell – 4 cell) or 2A (1 cell). The system is regulated by the MinSystemVoltage register. <default at POR>
1	EN_IDPM	R/W	1b	IDPM Enable Host writes this bit to enable IDPM regulation loop. When the IDPM is disabled by the charger (refer to IDPM_AUTO_DISABLE), this bit goes LOW. 0b: IDPM disabled 1b: IDPM enabled <default at POR>
0	CHRG_INHIBIT	R/W	0b	Charge Inhibit When this bit is 0, battery charging will start with valid values in the MaxChargeVoltage register and the ChargeCurrent register. 0b: Enable Charge <default at POR> 1b: Inhibit Charge

9.6.1.2 ChargeOption1 Register (I²C address = 31/30h) [reset = 0211h]

Figure 9-13. ChargeOption1 Register (I²C address = 31/30h) [reset = 0211h]

7	6	5	4	3	2	1	0
EN_IBAT	EN_PROCHOT_LPWR		EN_PSYS	RSNS_RAC	RSNS_RSR	PSYS_RATIO	PTM_PINSEL
R/W	R/W		R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
CMP_REF	CMP_POL	CMP_DEG		FORCE_ LATCHOFF	EN_PTM	EN_SHIP_ DCHG	AUTO_ WAKEUP_EN
R/W	R/W	R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-7. ChargeOption1 Register (I²C address = 31h) Field Descriptions

I²C 31h	FIELD	TYPE	RESET	DESCRIPTION
7	EN_IBAT	R/W	0b	IBAT Enable Enable the IBAT output buffer. In low power mode (REG0x01[7] = 1), IBAT buffer is always disabled regardless of this bit value. 0b Turn off IBAT buffer to minimize Iq <default at POR> 1b: Turn on IBAT buffer
6-5	EN_PROCHOT _LPWR	R/W	00b	Enable $\overline{\text{PROCHOT}}$ during battery only low power mode With battery only, enable VSYS in $\overline{\text{PROCHOT}}$ with low power consumption. Do not enable this function with adapter present. Refer to Section 9.3.9.1 for more details. 00b: Disable low power $\overline{\text{PROCHOT}}$ <default at POR> 01b: Reserved 10b: Enable VSYS low power $\overline{\text{PROCHOT}}$ 11b: Reserved
4	EN_PSYS	R/W	0b	PSYS Enable Enable PSYS sensing circuit and output buffer (whole PSYS circuit). In low power mode (REG0x01[7] = 1), PSYS sensing and buffer are always disabled regardless of this bit value. 0b: Turn off PSYS buffer to minimize Iq <default at POR> 1b: Turn on PSYS buffer
3	RSNS_RAC	R/W	0b	Input sense resistor RAC 0b: 10 mΩ <default at POR> 1b: 20 mΩ
2	RSNS_RSR	R/W	0b	Charge sense resistor RSR 0b: 10 mΩ <default at POR> 1b: 20 mΩ
1	PSYS_RATIO	R/W	1b	PSYS Gain Ratio of PSYS output current vs total input and battery power with 10-mΩ sense resistor. 0b: 0.25 µA/W 1b: 1 µA/W <default at POR>
0	PTM_PINSEL	R/W	0b	Select the ILIM_HIZ pin function 0b: charger enters HIZ mode when pull low the ILIM_HIZ pin. <default at POR> 1b: charger enters PTM when pull low the ILIM_HIZ pin.

Table 9-8. ChargeOption1 Register (I²C address = 30h) Field Descriptions

I²C 30h	FIELD	TYPE	RESET	DESCRIPTION
7	CMP_REF	R/W	0b	Independent Comparator Internal Reference. 0b: 2.3 V <default at POR> 1b: 1.2 V

Table 9-8. ChargeOption1 Register (I²C address = 30h) Field Descriptions (continued)

I²C 30h	FIELD	TYPE	RESET	DESCRIPTION
6	CMP_POL	R/W	0b	Independent Comparator Output Polarity 0b: When CMPIN is above internal threshold, CMPOUT is LOW (internal hysteresis) <default at POR> 1b: When CMPIN is below internal threshold, CMPOUT is LOW (external hysteresis)
5-4	CMP_DEG	R/W	01b	Independent Comparator Deglitch Time, only applied to the falling edge of CMPOUT (HIGH → LOW). 00b: Independent comparator is disabled 01b: Independent comparator is enabled with output deglitch time 1 µs <default at POR> 10b: Independent comparator is enabled with output deglitch time of 2 ms 11b: Independent comparator is enabled with output deglitch time of 5 sec
3	FORCE_LATCHOFF	R/W	0b	Force Power Path Off When independent comparator triggers, charger turns off Q1 and Q4 (same as disable converter) so that the system is disconnected from the input source. At the same time, CHRG_OK signal goes to LOW to notify the system. 0b: Disable this function <default at POR> 1b: Enable this function
2	EN_PTM	R/W	0b	PTM enable register bit 0b: disable PTM. <default at POR> 1b: enable PTM.
1	EN_SHIP_DCHG	R/W	0b	Discharge SRN for Shipping Mode When this bit is 1, discharge SRN pin down below 3.8 V in 140 ms. When 140 ms is over, this bit is reset to 0. 0b: Disable shipping mode <default at POR> 1b: Enable shipping mode
0	AUTO_WAKEUP_EN	R/W	1b	Auto Wakeup Enable When this bit is HIGH, if the battery is below minimum system voltage (REG0x0D/0C()), the device will automatically enable 128 mA charging current for 30 mins. When the battery is charged up above minimum system voltage, charge will terminate and the bit is reset to LOW. 0b: Disable 1b: Enable <default at POR>

9.6.1.3 ChargeOption2 Register (I²C address = 33/32h) [reset = 02B7h]

Figure 9-14. ChargeOption2 Register (I²C address = 33/32h) [reset = 02B7h]

7	6	5	4	3	2	1	0
PKPWR_TOVLD_DEG		EN_PKPWR_IDPM	EN_PKPWR_VSYS	PKPWR_OVLD_STAT	PKPWR_RELAX_STAT	PKPWR_TMAX[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	
7	6	5	4	3	2	1	0
EN_EXTILIM	EN_ICHG_IDCHG	Q2_OCP	ACX_OCP	EN_ACOC	ACOC_VTH	EN_	_VTH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-9. ChargeOption2 Register (I²C address = 33h) Field Descriptions

I²C 33h	FIELD	TYPE	RESET	DESCRIPTION
7-6	PKPWR_TOVLD_DEG	R/W	00b	Input Overload time in Peak Power Mode 00b: 1 ms <default at POR> 01b: 2 ms 10b: 10 ms 11b: 20 ms
5	EN_PKPWR_IDPM	R/W	0b	Enable Peak Power Mode triggered by input current overshoot If REG0x33[5:4] are 00b, peak power mode is disabled. Upon adapter removal, the bits are reset to 00b. 0b: Disable peak power mode triggered by input current overshoot <default at POR> 1b: Enable peak power mode triggered by input current overshoot.
4	EN_PKPWR_VSYS	R/W	0b	Enable Peak Power Mode triggered by system voltage under-shoot If REG0x33[5:4] are 00b, peak power mode is disabled. Upon adapter removal, the bits are reset to 00b. 0b: Disable peak power mode triggered by system voltage under-shoot <default at POR> 1b: Enable peak power mode triggered by system voltage under-shoot.
3	PKPWR_OVLD_STAT	R/W	0b	Indicator that the device is in overloading cycle. Write 0 to get out of overloading cycle. 0b: Not in peak power mode. <default at POR> 1b: In peak power mode.
2	PKPWR_RELAX_STAT	R/W	0b	Indicator that the device is in relaxation cycle. Write 0 to get out of relaxation cycle. 0b: Not in relaxation cycle. <default at POR> 1b: In relaxation mode.
1-0	PKPWR_TMAX[1:0]	R/W	10b	Peak power mode overload and relax cycle time. When REG0x33[7:6] is programmed longer than REG0x33[1:0], there is no relax time. 00b: 5 ms 01b: 10 ms 10b: 20 ms <default at POR> 11b: 40 ms

Table 9-10. ChargeOption2 Register (I²C address = 32h) Field Descriptions

I²C 32h	FIELD	TYPE	RESET	DESCRIPTION
7	EN_EXTILIM	R/W	1b	Enable ILIM_HIZ pin to set input current limit 0b: Input current limit is set by REG0x0F/0E. 1b: Input current limit is set by the lower value of ILIM_HIZ pin and REG0x0F/0E. <default at POR>
6	EN_ICHG_IDCHG	R/W	0b	0b: IBAT pin as discharge current. <default at POR> 1b: IBAT pin as charge current.

Table 9-10. ChargeOption2 Register (I^2C address = 32h) Field Descriptions (continued)

I^2C 32h	FIELD	TYPE	RESET	DESCRIPTION
5	Q2_OCP	R/W	1b	Q2 OCP threshold by sensing Q2 VDS 0b: 210 mV 1b: 150 mV <default at POR>
4	ACX_OCP	R/W	1b	Input current OCP threshold by sensing ACP-ACN. 0b: 280 mV 1b: 150 mV <default at POR>
3	EN_ACOC	R/W	0b	ACOC Enable Input overcurrent (ACOC) protection by sensing the voltage across ACP and ACN. Upon ACOC (after 100-µs blank-out time), converter is disabled. 0b: Disable ACOC <default at POR> 1b: ACOC threshold 133% or 200% ILIM2
2	ACOC_VTH	R/W	1b	ACOC Limit Set MOSFET OCP threshold as percentage of IDPM with current sensed from $R_{AC.}$ 0b: 133% of ILIM2 1b: 200% of ILIM2 <default at POR>
1	EN_BATOC	R/W	1b	BATOC Enable Battery discharge overcurrent (BATOC) protection by sensing the voltage across SRN and SRP. Upon BATOC, converter is disabled. 0b: Disable BATOC 1b: BATOC threshold 133% or 200% $\overline{\text{PROCHOT}}$ IDCHG <default at POR>
0	BATOC_VTH	R/W	1b	Set battery discharge overcurrent threshold as percentage of $\overline{\text{PROCHOT}}$ battery discharge current limit. 0b: 133% of $\overline{\text{PROCHOT}}$ IDCHG 1b: 200% of $\overline{\text{PROCHOT}}$ IDCHG <default at POR>

9.6.1.4 ChargeOption3 Register (I²C address = 35/34h) [reset = 0030h]

Figure 9-15. ChargeOption3 Register (I²C address = 35/34h) [reset = 0030h]

7	6	5	4	3	2	1	0
EN_HIZ	RESET_REG	RESET_ VINDPM	EN_OTG	EN_ICO MODE	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W		
7	6	5	4	3	2	1	0
Reserved	EN_CONS VAP	OTG_VAP _MODE	IL_AVG		OTG_RANGE _LOW	BATFETOFF_ HIZ	PSYS_OTG_ IDCHG
R/W	R/W	R/W	R/W		R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-11. ChargeOption3 Register (I²C address = 35h) Field Descriptions

I²C 35h	FIELD	TYPE	RESET	DESCRIPTION
7	EN_HIZ	R/W	0b	Device Hi-Z Mode Enable When the charger is in Hi-Z mode, the device draws minimal quiescent current. With VBUS above UVLO. REGN LDO stays on, and system powers from battery. 0b: Device not in Hi-Z mode <default at POR> 1b: Device in Hi-Z mode
6	RESET_REG	R/W	0b	Reset Registers All the registers go back to the default setting except the VINDPM register. VSYS_MIN will always go back to 1S default setting (3.584V), and the charging voltage goes back to the default values according to the cell pin setting. 0b: Idle <default at POR> 1b: Reset all the registers to default values. After reset, this bit goes back to 0. When the battery voltage is lower than minimal system voltage, or the battery is removed, it is NOT recommended to use this bit to reset the registers to default values.
5	RESET_VINDPM	R/W	0b	Reset VINDPM Threshold 0b: Idle 1b: Converter is disabled to measure VINDPM threshold. After VINDPM measurement is done, this bit goes back to 0 and converter starts.
4	EN_OTG	R/W	0b	OTG Mode Enable Enable device in OTG mode when EN_OTG pin is HIGH. 0b: Disable OTG <default at POR> 1b: Enable OTG mode to supply VBUS from battery.
3	EN_ICO_MODE	R/W	0b	Enable ICO Algorithm 0b: Disable ICO algorithm. <default at POR> 1b: Enable ICO algorithm.
2-0	Reserved	R/W	0b	Reserved

Table 9-12. ChargeOption3 Register (I²C address = 34h) Field Descriptions

I²C 34h	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Reserved
6	EN_CON_VAP	R/W	0b	Enable the conservative VAP mode. 0b: Disabled <default at POR> 1b: Enabled
5	OTG_VAP_MODE	R/W	1b	The selection of the external OTG/VAP pin control. 0b: the external OTG/VAP pin controls the EN/DIS VAP mode 1b: the external OTG/VAP pin controls the EN/DIS OTG mode <default at POR>

Table 9-12. ChargeOption3 Register (I²C address = 34h) Field Descriptions (continued)

I²C 34h	FIELD	TYPE	RESET	DESCRIPTION
4-3	IL_AVG	R/W	10b	4 levels inductor average current clamp. 00b: 6A 01b: 10A 10b: 15A <default at POR> 11b: Disabled
2	OTG_RANGE_LOW	R/W	0b	Selection of the different OTG output voltage range. 0b: VOTG high range 4.28 V - 20.8 V <default at POR> 1b: VOTG low range 3 V - 19.52 V
1	BATFETOFF_ HIZ	R/W	0b	Control BATFET during HIZ mode. 0b: BATFET on during Hi-Z <default at POR> 1b: BATFET off during Hi-Z
0	PSYS_OTG_ IDCHG	R/W	0b	PSYS function during OTG mode. 0b: PSYS as battery discharge power minus OTG output power <default at POR> 1b: PSYS as battery discharge power only

9.6.1.5 ProchotOption0 Register (I²C address = 37/36h) [reset = 04A65h]

Figure 9-16. ProchotOption0 Register (I²C address = 37/36h) [reset = 04A65h]

7-3	2-1	0
ILIM2_VTH	ICRIT_DEG	PROCHOT_ VDPM_80_90
R/W	R/W	R/W

7-4	3-2	1	0
VSYS_TH1	VSYS_TH2	INOM_DEG	LOWER_ PROCHOT _VDPM
R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-13. ProchotOption0 Register (I²C address = 37h) Field Descriptions

I²C 37h	FIELD	TYPE	RESET	DESCRIPTION
7-3	ILIM2_VTH	R/W	01001b	I_{LIM2} Threshold 5 bits, percentage of IDPM in 0x0F/0EH. Measure current between ACP and ACN. Trigger when the current is above this threshold: 00001b - 11001b: 110% - 230%, step 5% 11010b - 11110b: 250% - 450%, step 50% 11111b: Out of Range (Ignored) Default 150%, or 01001
2-1	ICRIT_DEG	R/W	01b	ICRIT Deglitch time ICRIT is set to be 110% of I_{ILIM2}. Typical ICRIT deglitch time to trigger $\overline{\text{PROCHOT}}$. 00b: 15 µs 01b: 100 µs <default at POR> 10b: 400 µs (max 500 us) 11b: 800 µs (max 1 ms)
0	PROCHOT_ VDPM_80_90	R/W	0b	Lower threshold of the PROCHOT_VDPM comparator When REG0x36[0]=1, the threshold of the PROCHOT_VDPM comparator is determined by this bit setting. 0b: 80% of VinDPM threshold <default at POR>. 1b: 90% of VinDPM threshold

Table 9-14. ProchotOption0 Register (I²C address = 36h) Field Descriptions

I²C 36h	FIELD	TYPE	RESET	DESCRIPTION
7-4	VSYS_TH1	R/W	0110b	VSYS Threshold to trigger discharging VBUS in VAP mode. Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. 2S - 4S battery 0000b - 1111b: 5.9 V - 7.4V with 0.1 V step size. 1S battery 0000b - 0111b: 3.1 V - 3.8 V with 0.1 V step size. 1000b - 1111b: 3.1 V - 3.8 V with 0.1 V step size.
3-2	VSYS_TH2	R/W	01b	VSYS Threshold to assert /PROCHOT_VSYS. Measure on VSYS with fixed 5-µs deglitch time. Trigger when SYS pin voltage is below the thresholds. 2S - 4S battery 00b: 5.9V; 01b: 6.2V <default at POR>; 10b: 6.5V; 11b: 6.8V. 1S battery 00b: 3.1V; 01b: 3.3V <default at POR>; 10b: 3.5V; 11b: 3.7V.

Table 9-14. ProchotOption0 Register (I^2C address = 36h) Field Descriptions (continued)

I^2C 36h	FIELD	TYPE	RESET	DESCRIPTION
1	INOM_DEG	R/W	0b	INOM Deglitch Time INOM is always 10% above IDPM in 0x0F/0EH. Measure current between ACP and ACN. Trigger when the current is above this threshold. 0b: 1 ms (must be max) <default at POR> 1b: 50 ms (max 60 ms)
0	LOWER_ PROCHOT _VDPM	R/W	1b	Enable the lower threshold of the PROCHOT_VDPM comparator 0b: the threshold of the PROCHOT_VDPM comparator follows the same VinDPM REG0x0A/0B() setting. 1b: the threshold of the PROCHOT_VDPM comparator is lower and determined by REG0x37[0] setting. <default at POR>

9.6.1.6 ProchotOption1 Register (I^2C address = 39/38h) [reset = 81A0h]

Figure 9-17. ProchotOption1 Register (I^2C address = 39/38h) [reset = 81A0h]

7-2						1-0	
IDCHG_VTH						IDCHG_DEG	
R/W						R/W	
7	6	5	4	3	2	1	0
PP_VDPM	PROCHOT_PROFILE_IC	PP_ICRIT	PP_INOM	PP_IDCHG	PP_VSYS	PP_BATPRES	PP_ACOK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When the REG0x38[7:0] are set to be disabled, the $\overline{\text{PROCHOT}}$ event associated with that bit will not be reported in the $\overline{\text{PROCHOT}}$ status register REG0x22[7:0] any more, and the $\overline{\text{PROCHOT}}$ pin will not be pulled low any more if the event happens.

Table 9-15. ProchotOption1 Register (I^2C address = 39h) Field Descriptions

I^2C 39h	FIELD	TYPE	RESET	DESCRIPTION
7-2	IDCHG_VTH	R/W	100000b	IDCHG Threshold 6 bit, range, range 0 A to 32256 mA, step 512 mA. There is a 128 mA offset. Measure current between SRN and SRP. Trigger when the discharge current is above the threshold. If the value is programmed to 000000b, $\overline{\text{PROCHOT}}$ is always triggered. Default: 16384 mA or 100000b
1-0	IDCHG_DEG	R/W	01b	IDCHG Deglitch Time 00b: 1.6 ms 01b: 100 µs <default at POR> 10b: 6 ms 11b: 12 ms

Table 9-16. ProchotOption1 Register (I^2C address = 38h) Field Descriptions

I^2C 38h	FIELD	TYPE	RESET	DESCRIPTION
7	PROCHOT _PROFILE_VDPM	R/W	1b	$\overline{\text{PROCHOT}}$ Profile When all the REG0x38[7:0] bits are 0, $\overline{\text{PROCHOT}}$ function is disabled. Bit7 PP_VDPM detects VBUS voltage 0b: disable <default at POR> 1b: enable
6	PROCHOT _PROFILE_COMP	R/W	0b	0b: disable <default at POR> 1b: enable
5	PROCHOT _PROFILE_ICRIT	R/W	1b	0b: disable 1b: enable <default at POR>
4	PROCHOT _PROFILE_INOM	R/W	0b	0b: disable <default at POR> 1b: enable
3	PROCHOT _PROFILE_IDCHG	R/W	0b	0b: disable <default at POR> 1b: enable
2	PROCHOT _PROFILE_VSYS	R/W	0b	0b: disable <default at POR> 1b: enable
1	PROCHOT _PROFILE_BATPRES	R/W	0b	0b: disable <default at POR> 1b: enable (one-shot falling edge triggered) If BATPRES is enabled in $\overline{\text{PROCHOT}}$ after the battery is removed, it will immediately send out one-shot $\overline{\text{PROCHOT}}$ pulse.

Table 9-16. ProchotOption1 Register (I^2C address = 38h) Field Descriptions (continued)

I^2C 38h	FIELD	TYPE	RESET	DESCRIPTION
0	PROCHOT _PROFILE_ACOK	R/W	0b	0b: disable <default at POR> 1b: enable ChargeOption0[15] = 0 to assert $\overline{\text{PROCHOT}}$ pulse after adapter removal. If PROCHOT_PROFILE_ACOK is enabled in $\overline{\text{PROCHOT}}$ after the adapter is removed, it will be pulled low.

9.6.1.7 ADCOption Register (I²C address = 3B/3Ah) [reset = 2000h]

Figure 9-18. ADCOption Register (I²C address = 3B/3Ah) [reset = 2000h]

7	6	5	4-0				
ADC_CONV	ADC_START	ADC_ FULLSCALE	Reserved				
R/W	R/W	R/W	R/W				
7	6	5	4	3	2	1	0
EN_ADC_ CMPIN	EN_ADC_ VBUS	EN_ADC_ PSYS	EN_ADC_ IIN	EN_ADC_ IDCHG	EN_ADC_ ICHG	EN_ADC_ VSYS	EN_ADC_ VBAT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The ADC registers are read in the following order: VBAT, VSYS, ICHG, IDCHG, IIN, PSYS, VBUS, CMPIN. ADC is disabled in low power mode. When enabling ADC, the device exit low power mode at battery only.

Table 9-17. ADCOption Register (I²C address = 3Bh) Field Descriptions

I²C 3Bh	FIELD	TYPE	RESET	DESCRIPTION
7	ADC_CONV	R/W	0b	Typical ADC conversion time is 10 ms. 0b: One-shot update. Do one set of conversion updates to registers REG0x27/26(), REG0x29/28(), REG0x2B/2A(), and REG0x2D/2C() after ADC_START = 1. 1b: Continuous update. Do a set of conversion updates to registers REG0x27/26(), REG0x29/28(), REG0x2B/2A(), and REG0x2D/2C() every 1 sec.
6	ADC_START	R/W	0b	0b: No ADC conversion 1b: Start ADC conversion. After the one-shot update is complete, this bit automatically resets to zero
5	ADC_ FULLSCALE	R/W	1b	ADC input voltage range. When input voltage is below 5 V, or battery is 1S, full scale 2.04 V is recommended. 0b: 2.04 V 1b: 3.06 V <default at POR>
4-0	Reserved	R/W	00000b	Reserved

Table 9-18. ADCOption Register (I²C address = 3Ah) Field Descriptions

I²C 3Ah	FIELD	TYPE	RESET	DESCRIPTION
7	EN_ADC_CMPIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
6	EN_ADC_VBUS	R/W	0b	0b: Disable <default at POR> 1b: Enable
5	EN_ADC_PSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
4	EN_ADC_IIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
3	EN_ADC_IDCHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
2	EN_ADC_ICHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
1	EN_ADC_VSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
0	EN_ADC_VBAT	R/W	0b	0b: Disable <default at POR> 1b: Enable

9.6.2 Charge and $\overline{\text{PROCHOT}}$ Status

9.6.2.1 ChargerStatus Register (I^2C address = 21/20h) [reset = 0000h]

Figure 9-19. ChargerStatus Register (I^2C address = 21/20h) [reset = 0000h]

7	6	5	4	3	2	1	0
AC_STAT	ICO_DONE	IN_VAP	IN_VINDPM	IN_IINDPM	IN_FCHRG	IN_PCHRG	IN_OTG
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Fault ACOV	Fault BATOC	Fault ACOC	SYSOVP _STAT	Fault SYS _SHORT	Fault Latchoff	Fault_OTG _OVP	Fault_OTG _OCP
R	R	R	R/W	R/W	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-19. ChargerStatus Register (I^2C address = 21h) Field Descriptions

I^2C 21h	FIELD	TYPE	RESET	DESCRIPTION
7	AC_STAT	R	0b	Input source status, same as CHRG_OK bit 0b: Input not present 1b: Input is present
6	ICO_DONE	R	0b	After the ICO routine is successfully executed, the bit goes 1. 0b: ICO is not complete 1b: ICO is complete
5	IN_VAP	R	0b	0b: Charger is not operated in VAP mode 1b: Charger is operated in VAP mode
4	IN_VINDPM	R	0b	0b: Charger is not in VINDPM during forward mode, or voltage regulation during OTG mode 1b: Charger is in VINDPM during forward mode, or voltage regulation during OTG mode
3	IN_IINDPM	R	0b	0b: Charger is not in IINDPM 1b: Charger is in IINDPM
2	IN_FCHRG	R	0b	0b: Charger is not in fast charge 1b: Charger is in fast charger
1	IN_PCHRG	R	0b	0b: Charger is not in pre-charge 1b: Charger is in pre-charge
0	IN_OTG	R	0b	0b: Charger is not in OTG 1b: Charge is in OTG

Table 9-20. ChargerStatus Register (I^2C address = 20h) Field Descriptions

I^2C 20h	FIELD	TYPE	RESET	DESCRIPTION
7	Fault ACOV	R	0b	The faults are latched until a read from host. 0b: No fault 1b: ACOV
6	Fault BATOC	R	0b	The faults are latched until a read from host. 0b: No fault 1b: BATOC
5	Fault ACOC	R	0b	The faults are latched until a read from host. 0b: No fault 1b: ACOC

Table 9-20. ChargerStatus Register (I²C address = 20h) Field Descriptions (continued)

I²C 20h	FIELD	TYPE	RESET	DESCRIPTION
4	SYSOVP_STAT	R/W	0b	SYSOVP Status and Clear When the SYSOVP occurs, this bit is HIGH. During the SYSOVP, the converter is disabled. After the SYSOVP is removed, the user must write a 0 to this bit or unplug the adapter to clear the SYSOVP condition to enable the converter again. 0b: Not in SYSOVP <default at POR> 1b: In SYSOVP. When SYSOVP is removed, write 0 to clear the SYSOVP latch.
3	Fault SYS_SHORT	R/W	0b	The fault is latched until a clear from host by writing this bit to 0. 0b: No fault <default at POR> 1b: When SYS is lower than 2.4V, then 7 times restart tries are failed.
2	Fault Latchoff	R	0b	The faults are latched until a read from host. 0b: No fault 1b: Latch off (REG0x30[3])
1	Fault_OTG_OVP	R	0b	The faults are latched until a read from host. 0b: No fault 1b: OTG OVP
0	Fault_OTG_UVP	R	0b	The faults are latched until a read from host. 0b: No fault 1b: OTG UVP

9.6.2.2 ProchotStatus Register (I²C address = 23/22h) [reset = A800h]

Figure 9-20. ProchotStatus Register (I²C address = 23/22h) [reset = A800h]

7	6	5	4	3	2	1	0
Reserved	EN_PROCHOT _EXIT	PROCHOT_WIDTH		PROCHOT _CLEAR	Reserved	STAT_VAP _FAIL	STAT_EXIT _VAP
R	R/W	R/W		R/W	R	R/W	R/W
7	6	5	4	3	2	1	0
STAT_VDPM	STAT_COMP	STAT_ICRIT	STAT_INOM	STAT_IDCHG	STAT_VSYS	STAT_BAT _Removal	STAT_ADPT _Removal
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-21. ProchotStatus Register (I²C address = 23h) Field Descriptions

I²C 23h	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R	1b	Reserved
6	EN_PROCHOT _EXIT	R/W	0b	$\overline{\text{PROCHOT}}$ Pulse Extension Enable. When pulse extension is enabled, keep the $\overline{\text{PROCHOT}}$ pin voltage LOW until host writes REG0x23[3] = 0. 0b: Disable pulse extension <default at POR> 1b: Enable pulse extension
5-4	PROCHOT _WIDTH	R/W	10b	$\overline{\text{PROCHOT}}$ Pulse Width Minimum $\overline{\text{PROCHOT}}$ pulse width when REG0x23[6] = 0 00b: 100 us 01b: 1 ms 10b: 10 ms <default at POR> 11b: 5s
3	PROCHOT _CLEAR	R/W	1b	$\overline{\text{PROCHOT}}$ Pulse Clear. Clear $\overline{\text{PROCHOT}}$ pulse when 0x23[6] = 1. 0b: Clear $\overline{\text{PROCHOT}}$ pulse and drive $\overline{\text{PROCHOT}}$ pin HIGH 1b: Idle <default at POR>
2	Reserved	R	0b	Reserved
1	STAT_VAP_FAIL	R/W	0b	This status bit reports a failure to load VBUS 7 consecutive times in VAP mode, which indicates the battery voltage might be not high enough to enter VAP mode, or the VAP loading current settings are too high. 0b: Not is VAP failure <default at POR> 1b: In VAP failure, the charger exits VAP mode, and latches off until the host writes this bit to 0.
0	STAT_EXIT_VAP	R/W	0b	When the charger is operated in VAP mode, it can exit VAP by either being disabled through host, or there is any charger faults. 0b: PROCHOT_EXIT_VAP is not active <default at POR> 1b: PROCHOT_EXIT_VAP is active, $\overline{\text{PROCHOT}}$ pin is low until host writes this status bit to 0.

Table 9-22. ProchotStatus Register (I²C address = 22h) Field Descriptions

I²C 22h	FIELD	TYPE	RESET	DESCRIPTION
7	STAT_VDPM	R/W	0b	0b: Not triggered 1b: Triggered
6	STAT_COMP	R	0b	0b: Not triggered 1b: Triggered
5	STAT_ICRIT	R	0b	0b: Not triggered 1b: Triggered
4	STAT_INOM	R	0b	0b: Not triggered 1b: Triggered

Table 9-22. ProchotStatus Register (I^2C address = 22h) Field Descriptions (continued)

I^2C 22h	FIELD	TYPE	RESET	DESCRIPTION
3	STAT_IDCHG	R	0b	0b: Not triggered 1b: Triggered
2	STAT_VSYS	R	0b	0b: Not triggered 1b: Triggered
1	STAT_Battery_Removal	R	0b	0b: Not triggered 1b: Triggered
0	STAT_Adapter_Removal	R	0b	0b: Not triggered 1b: Triggered

9.6.3 ChargeCurrent Register (I²C address = 03/02h) [reset = 0000h]

To set the charge current, write a 16-bit ChargeCurrent() command (REG0x03/02h()) using the data format listed in Figure 9-21, Table 9-23, and Table 9-24.

With 10-mΩ sense resistor, the charger provides charge current range of 64 mA to 8.128 A, with a 64-mA step resolution. Upon POR, when auto wakeup is not active, ChargeCurrent() is 0 A. Any conditions for CHRG_OK low except ACOV will reset ChargeCurrent() to zero. CELL_BATPRESZ going LOW (battery removal) will reset the ChargeCurrent() register to 0 A.

Charge current is not reset in ACOC, TSHUT, power path latch off (REG0x30[1]), and SYSOVP.

A 0.1-µF capacitor between SRP and SRN for differential mode filtering is recommended; an optional 0.1-µF capacitor between SRN and ground, and an optional 0.1-µF capacitor between SRP and ground for common mode filtering. Meanwhile, the capacitance on SRP should not be higher than 0.1 µF in order to properly sense the voltage across SRP and SRN for cycle-by-cycle current detection.

The SRP and SRN pins are used to sense voltage drop across RSR with default value of 10 mΩ. However, resistors of other values can also be used. For a larger sense resistor, a larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss. A current sensing resistor value no more than 20 mΩ is suggested.

Figure 9-21. ChargeCurrent Register With 10-mΩ Sense Resistor (I²C address = 03/02h) [reset = 0h]

7	6	5	4	3	2	1	0
Reserved			Charge Current, bit 6	Charge Current, bit 5	Charge Current, bit 4	Charge Current, bit 3	Charge Current, bit 2
R/W			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Charge Current, bit 1	Charge Current, bit 0	Reserved	Reserved				
R/W	R/W	R/W	R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-23. Charge Current Register (14h) With 10-mΩ Sense Resistor (I²C address = 03h) Field Descriptions

I²C 03h	FIELD	TYPE	RESET	DESCRIPTION
7-5	Reserved	R/W	000b	Not used. 1 = invalid write.
4	Charge Current, bit 6	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 4096 mA of charger current.
3	Charge Current, bit 5	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 2048 mA of charger current.
2	Charge Current, bit 4	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 1024 mA of charger current.
1	Charge Current, bit 3	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 512 mA of charger current.
0	Charge Current, bit 2	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 256 mA of charger current.

Table 9-24. Charge Current Register (14h) With 10-mΩ Sense Resistor (I²C address = 02h) Field Descriptions

I²C 02h	FIELD	TYPE	RESET	DESCRIPTION
7	Charge Current, bit 1	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 128 mA of charger current.
6	Charge Current, bit 0	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 64 mA of charger current.

Table 9-24. Charge Current Register (14h) With 10-mΩ Sense Resistor (I^2C address = 02h) Field Descriptions (continued)

I^2C 02h	FIELD	TYPE	RESET	DESCRIPTION
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

9.6.3.1 Battery Pre-Charge Current Clamp

During pre-charge, BATFET works in linear mode or LDO mode (default REG0x00[2] = 1). For 2-4 cell battery, the system is regulated at minimum system voltage in REG0x0D/0C() and the pre-charge current is clamped at 384 mA. For 1 cell battery, the pre-charge to fast charge threshold is 3 V, and the pre-charge current is clamped at 384 mA. However, the BATFET stays in LDO mode operation till battery voltage is above minimum system voltage (~3.6 V). During battery voltage from 3 V to 3.6 V, the fast charge current is clamped at 2 A.

9.6.4 MaxChargeVoltage Register (I^2C address = 05/04h) [reset value based on CELL_BATPRESZ pin setting]

To set the output charge voltage, write a 16-bit ChargeVoltage register command (REG0x05/04()) using the data format listed in Figure 9-22, Table 9-25, and Table 9-26. The charger provides charge voltage range from 1.024 V to 19.200 V, with 8-mV step resolution. Any write below 1.024 V or above 19.200 V is ignored.

Upon POR, REG0x05/04() is by default set as 4200 mV for 1 s, 8400 mV for 2 s, 12600 mV for 3 s or 16800 mV for 4 s. After CHRG_OK goes high, the charge will start when the host writes the charging current to REG0x03/02(), the default charging voltage is used if REG0x05/04() is not programmed. If the battery is different from 4.2 V/cell, the host has to write to REG0x05/04() before REG0x03/02() for correct battery voltage setting. Writing REG0x05/04() to 0 will set REG0x05/04() to the default value based on CELL_BATPRESZ pin, and force REG0x03/02() to zero to disable charge.

The SRN pin senses the battery voltage for voltage regulation and should be connected as close to the battery as possible, and directly place a decoupling capacitor (0.1 µF recommended) as close to the device as possible to decouple high frequency noise.

Figure 9-22. MaxChargeVoltage Register (I^2C address = 05/04h) [reset value based on CELL_BATPRESZ pin setting]

7	6	5	4	3	2	1	0
Reserved	Max Charge Voltage, bit 11	Max Charge Voltage, bit 10	Max Charge Voltage, bit 9	Max Charge Voltage, bit 8	Max Charge Voltage, bit 7	Max Charge Voltage, bit 6	Max Charge Voltage, bit 5
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Max Charge Voltage, bit 4	Max Charge Voltage, bit 3	Max Charge Voltage, bit 2	Max Charge Voltage, bit 1	Max Charge Voltage, bit 1	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-25. MaxChargeVoltage Register (I^2C address = 05h) Field Descriptions

I^2C 05h	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	Max Charge Voltage, bit 11	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 16384 mV of charger voltage.
5	Max Charge Voltage, bit 10	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 8192 mV of charger voltage
4	Max Charge Voltage, bit 9	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 4096 mV of charger voltage.
3	Max Charge Voltage, bit 8	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 2048 mV of charger voltage.
2	Max Charge Voltage, bit 7	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 1024 mV of charger voltage.
1	Max Charge Voltage, bit 6	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 512 mV of charger voltage.
0	Max Charge Voltage, bit 5	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 256 mV of charger voltage.

Table 9-26. MaxChargeVoltage Register (I^2C address = 04h) Field Descriptions

I^2C 04h	FIELD	TYPE	RESET	DESCRIPTION
7	Max Charge Voltage, bit 4	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 128 mV of charger voltage.
6	Max Charge Voltage, bit 3	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 64 mV of charger voltage.

Table 9-26. MaxChargeVoltage Register (I^2C address = 04h) Field Descriptions (continued)

I^2C 04h	FIELD	TYPE	RESET	DESCRIPTION
5	Max Charge Voltage, bit 2	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 32 mV of charger voltage.
4	Max Charge Voltage, bit 1	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 16 mV of charger voltage.
3	Max Charge Voltage, bit 0	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 8 mV of charger voltage.
2-0	Reserved	R/W	000b	Not used. Value Ignored.

9.6.5 MinSystemVoltage Register (I²C address = 0D/0Ch) [reset value based on CELL_BATPRESZ pin setting]

To set the minimum system voltage, write a 16-bit MinSystemVoltage register command (REG0x0D/0C()) using the data format listed in Figure 9-23, Table 9-27, and Table 9-28. The charger provides minimum system voltage range from 1.024 V to 16.128 V, with 256-mV step resolution. Any write below 1.024 V or above 16.128 V is ignored. Upon POR, the MinSystemVoltage register is 3.584 V for 1 S, 6.144 V for 2 S and 9.216 V for 3 S, and 12.288 V for 4 S.

Figure 9-23. MinSystemVoltage Register (I²C address = 0D/0Ch) [reset value based on CELL_BATPRESZ pin setting]

7	6	5	4	3	2	1	0
Reserved		Min System Voltage, bit 5	Min System Voltage, bit 4	Min System Voltage, bit 3	Min System Voltage, bit 2	Min System Voltage, bit 1	Min System Voltage, bit 0
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-27. MinSystemVoltage Register (I²C address = 0Dh) Field Descriptions

I²C 0Dh	FIELD	TYPE	RESET	DESCRIPTION
7-6	Reserved	R/W	00b	Not used. 1 = invalid write.
5	Min System Voltage, bit 5	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 8192 mV of system voltage.
4	Min System Voltage, bit 4	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 4096mV of system voltage.
3	Min System Voltage, bit 3	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 2048 mV of system voltage.
2	Min System Voltage, bit 2	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 1024 mV of system voltage.
1	Min System Voltage, bit 1	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 512 mV of system voltage.
0	Min System Voltage, bit 0	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 256 mV of system voltage.

Table 9-28. MinSystemVoltage Register (I²C address = 0Ch) Field Descriptions

I²C 0Ch	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R/W	00000000b	Not used. Value Ignored.

9.6.5.1 System Voltage Regulation

The device employs Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG0x0D/0C(). Even with a deeply depleted battery, the system is regulated above the minimum system voltage with BATFET.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on when charging or in supplement mode and the voltage difference between the system and battery is the VDS of BATFET. System voltage is regulated 160 mV above battery voltage when BATFET is off (no charging or no supplement current).

When BATFET is removed, the system node VSYS is shorted to SRP. Before the converter starts operation, LDO mode needs to be disabled. The following sequence is required to configure charger without BATFET.

1. Before adapter plugs in, put the charger into HIZ mode. (either pull pin 6 ILIM_HIZ to ground, or set REG0x35[7] to 1)
2. Set 0x00[2] to 0 to disable LDO mode.
3. Set 0x30[0] to 0 to disable auto-wakeup mode.
4. Check if battery voltage is properly programmed (REG0x05/04)
5. Set pre-charge/charge current (REG0x03/02)
6. Put the device out of HIZ mode. (Release ILIM_HIZ from ground and set REG0x35[7]=0).

In order to prevent any accidental SW mistakes, the host sets low input current limit (a few hundred milliamps) when device is out of HIZ.

9.6.6 Input Current and Input Voltage Registers for Dynamic Power Management

The charger supports Dynamic Power Management (DPM). Normally, the input power source provides power for the system load or to charge the battery. When the input current exceeds the input current setting, or the input voltage falls below the input voltage setting, the charger decreases the charge current to provide priority to the system load. As the system current rises, the available charge current drops accordingly towards zero. If the system load keeps increasing after the charge current drops down to zero, the system voltage starts to drop. As the system voltage drops below the battery voltage, the battery will discharge to supply the heavy system load.

9.6.6.1 Input Current Registers

To set the maximum input current limit, write a 16-bit IIN_HOST register command (REG0x0F/0E()) using the data format listed in Table 9-29 and Table 9-30. When using a 10-mΩ sense resistor, the charger provides an input-current limit range of 50 mA to 6400 mA, with 50-mA resolution. The default current limit is 3.25 A. Due to the USB current setting requirement, the register setting specifies the maximum current instead of the typical current. Upon adapter removal, the input current limit is reset to the default value of 3.25 A. With code 0, the input current limit is 50 mA.

The ACP and ACN pins are used to sense R_{AC} with the default value of 10 mΩ. For a 20-mΩ sense resistor, a larger sense voltage is given and a higher regulation accuracy, but at the expense of higher conduction loss.

Instead of using the internal DPM loop, the user can build up an external input current regulation loop and have the feedback signal on the ILIM_HIZ pin.

$$V_{ILIM\_HIZ} = 1V + 40 \times (V_{ACP} - V_{ACN}) = 1 + 40 \times I_{DPM} \times R_{AC} \quad (2)$$

In order to disable ILIM_HIZ pin, the host can write to 0x32[7] to disable ILIM_HIZ pin, or pull ILIM_HIZ pin above 4.0 V.

9.6.6.1.1 IIN_HOST Register With 10-mΩ Sense Resistor (I²C address = 0F/0Eh) [reset = 4100h]

With code 0, the input current limit readback is 50 mA.

Figure 9-24. IIN_HOST Register With 10-mΩ Sense Resistor (I²C address = 0F/0Eh) [reset = 4100h]

7	6	5	4	3	2	1	0
Reserved	Input Current set by host, bit 6	Input Current set by host, bit 5	Input Current set by host, bit 4	Input Current set by host, bit 3	Input Current set by host, bit 2	Input Current set by host, bit 1	Input Current set by host, bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-29. IIN_HOST Register With 10-mΩ Sense Resistor (I²C address = 0Fh) Field Descriptions

I²C 0Fh	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	Input Current set by host, bit 6	R/W	1b	0 = Adds 0 mA of input current. 1 = Adds 3200 mA of input current.
5	Input Current set by host, bit 5	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 1600 mA of input current.
4	Input Current set by host, bit 4	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 800 mA of input current.
3	Input Current set by host, bit 3	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 400 mA of input current.
2	Input Current set by host, bit 2	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 200 mA of input current.
1	Input Current set by host, bit 1	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 100 mA of input current.
0	Input Current set by host, bit 0	R/W	1b	0 = Adds 0 mA of input current. 1 = Adds 50 mA of input current.

Table 9-30. IIN_HOST Register With 10-mΩ Sense Resistor (I²C address = 0Eh) Field Descriptions

I²C 0Eh	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R	00000000b	Not used. Value Ignored.

9.6.6.1.2 IIN_DPM Register With 10-mΩ Sense Resistor (I^2C address = 25/24h) [reset = 4100h]

IIN_DPM register reflects the actual input current limit programmed in the register, either from host or from ICO.

After ICO, the current limit used by DPM regulation may differ from the IIN_HOST register settings. The actual DPM limit is reported in REG0x25/24(). With code 0, the input current limit read-back is 50 mA.

Figure 9-25. IIN_DPM Register With 10-mΩ Sense Resistor (I^2C address = 25/24h) [reset = 4100h]

7	6	5	4	3	2	1	0
Reserved	Input Current in DPM, bit 6	Input Current in DPM, bit 5	Input Current in DPM, bit 4	Input Current in DPM, bit 3	Input Current in DPM, bit 2	Input Current in DPM, bit 1	Input Current in DPM, bit 0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-31. IIN_DPM Register With 10-mΩ Sense Resistor (I^2C address = 25h) Field Descriptions

I^2C 25h	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R	0b	Not used. 1 = invalid write.
6	Input Current in DPM, bit 6	R	0b	0 = Adds 0 mA of input current. 1 = Adds 3200 mA of input current.
5	Input Current in DPM, bit 5	R	0b	0 = Adds 0 mA of input current. 1 = Adds 1600 mA of input current.
4	Input Current in DPM, bit 4	R	0b	0 = Adds 0 mA of input current. 1 = Adds 800mA of input current
3	Input Current in DPM, bit 3	R	0b	0 = Adds 0 mA of input current. 1 = Adds 400 mA of input current.
2	Input Current in DPM, bit 2	R	0b	0 = Adds 0 mA of input current. 1 = Adds 200 mA of input current.
1	Input Current in DPM, bit 1	R	0b	0 = Adds 0 mA of input current. 1 = Adds 100 mA of input current.
0	Input Current in DPM, bit 0	R	0b	0 = Adds 0 mA of input current. 1 = Adds 50 mA of input current.

Table 9-32. IIN_DPM Register With 10-mΩ Sense Resistor (I^2C address = 24h) Field Descriptions

I^2C 24h	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R	00000000b	Not used. Value Ignored.

9.6.6.1.3 InputVoltage Register (I²C address = 0B/0Ah) [reset = VBUS-1.28V]

To set the input voltage limit, write a 16-bit InputVoltage register command (REG0x0B/0A()) using the data format listed in Figure 9-26, Table 9-33, and Table 9-34.

If the input voltage drops more than the InputVoltage register allows, the device enters DPM and reduces the charge current. The default offset voltage is 1.28 V below the no-load VBUS voltage. The DC offset is 3.2 V (0000000).

Figure 9-26. InputVoltage Register (I²C address = 0B/0Ah) [reset = VBUS-1.28V]

7	6	5	4	3	2	1	0
Reserved		Input Voltage, bit 7	Input Voltage, bit 6	Input Voltage, bit 5	Input Voltage, bit 4	Input Voltage, bit 3	Input Voltage, bit 2
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Input Voltage, bit 1	Input Voltage, bit 0	Reserved					
R/W	R/W	R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-33. InputVoltage Register (I²C address = 0Bh) Field Descriptions

I²C 0Bh	FIELD	TYPE	RESET	DESCRIPTION
7-6	Reserved	R/W	00b	Not used. 1 = invalid write.
5	Input Voltage, bit 7	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 8192 mV of input voltage.
4	Input Voltage, bit 6	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 4096mV of input voltage.
3	Input Voltage, bit 5	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 2048 mV of input voltage.
2	Input Voltage, bit 4	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 1024 mV of input voltage.
1	Input Voltage, bit 3	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 512 mV of input voltage.
0	Input Voltage, bit 2	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 256 mV of input voltage.

Table 9-34. InputVoltage Register (I²C address = 0Ah) Field Descriptions

I²C 0Ah	FIELD	TYPE	RESET	DESCRIPTION
7	Input Voltage, bit 1	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 128 mV of input voltage.
6	Input Voltage, bit 0	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 64 mV of input voltage
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

9.6.7 OTGVoltage Register (I²C address = 07/06h) [reset = 0000h]

To set the OTG output voltage limit, write to REG0x07/06() using the data format listed in Figure 9-27, Table 9-35, and Table 9-36.

The DAC is clamped in digital core at minimal 3V and maximum 20.8V. Any register writing lower than the minimal or higher than the maximum will be ignored. When REG0x34[2] = 1, there is no DAC offset. When REG0x34[2] = 0 the DAC is offset by 1.28V

Figure 9-27. OTGVoltage Register (I²C address = 07/06h) [reset = 0000h]

7	6	5	4	3	2	1	0
Reserved		OTG Voltage, bit 11	OTG Voltage, bit 10	OTG Voltage, bit 9	OTG Voltage, bit 8	OTG Voltage, bit 7	OTG Voltage, bit 6
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
OTG Voltage, bit 5	OTG Voltage, bit 4	OTG Voltage, bit 3	OTG Voltage, bit 2	OTG Voltage, bit 1	OTG Voltage, bit 0	Reserved	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-35. OTGVoltage Register (I²C address = 07h) Field Descriptions

I²C 07h	FIELD	TYPE	RESET	DESCRIPTION
7-6	Reserved	R/W	00b	Not used. 1 = invalid write.
5	OTG Voltage, bit 11	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 16656 mV of OTG voltage.
4	OTG Voltage, bit 10	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 8328 mV of OTG voltage.
3	OTG Voltage, bit 9	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 4164 mV of OTG voltage.
2	OTG Voltage, bit 8	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 2082 mV of OTG voltage.
1	OTG Voltage, bit 7	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 1041 mV of OTG voltage.
0	OTG Voltage, bit 6	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 521 mV of OTG voltage.

Table 9-36. OTGVoltage Register (I²C address = 06h) Field Descriptions

I²C 06h	FIELD	TYPE	RESET	DESCRIPTION
7	OTG Voltage, bit 5	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 260 mV of OTG voltage.
6	OTG Voltage, bit 4	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 130 mV of OTG voltage.
5	OTG Voltage, bit 3	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 65 mV of OTG voltage.
4	OTG Voltage, bit 2	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 33 mV of OTG voltage.
3	OTG Voltage, bit 1	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 16 mV of OTG voltage.
2	OTG Voltage, bit 0	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 8.1 mV of OTG voltage.
1-0	Reserved	R/W	00b	Not used. Value Ignored.

9.6.8 OTGCurrent Register (I²C address = 09/08h) [reset = 0000h]

To set the OTG output current limit, write to REG0x09/08() using the data format listed in Figure 9-28, Table 9-37, and Table 9-38.

Figure 9-28. OTGCurrent Register (I²C address = 09/08h) [reset = 0000h]

7	6	5	4	3	2	1	0
Reserved	OTG Current set by host, bit 6	OTG Current set by host, bit 5	OTG Current set by host, bit 4	OTG Current set by host, bit 3	OTG Current set by host, bit 2	OTG Current set by host, bit 1	OTG Current set by host, bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-37. OTGCurrent Register (I²C address = 09h) Field Descriptions

I²C 09h	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Not used. 1 = invalid write.
6	OTG Current set by host, bit 6	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 3200 mA of OTG current.
5	OTG Current set by host, bit 5	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 1600mA of OTG current.
4	OTG Current set by host, bit 4	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 800 mA of OTG current.
3	OTG Current set by host, bit 3	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 400 mA of OTG current.
2	OTG Current set by host, bit 2	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 200 mA of OTG current.
1	OTG Current set by host, bit 1	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 100 mA of OTG current.
0	OTG Current set by host, bit 0	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 50 mA of OTG current.

Table 9-38. OTGCurrent Register (I²C address = 08h) Field Descriptions

I²C 08h	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R/W	00000000b	Not used. Value Ignored.

9.6.9 ADCVBUS/PSYS Register (I²C address = 27/26h)

- PSYS: Full range: 3.06 V, LSB: 12 mV
- VBUS: Full range: 3200 mV to 19520 mV, LSB: 64 mV

Figure 9-29. ADCVBUS/PSYS Register (I²C address = 27/26h)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-39. ADCVBUS/PSYS Register (I²C address = 27h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Input Voltage

Table 9-40. ADCVBUS/PSYS Register (I²C address = 26h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of System Power

9.6.10 ADCIBAT Register (I^2C address = 29/28h)

- ICHG: Full range: 8.128 A, LSB: 64 mA
- IDCHG: Full range: 32.512 A, LSB: 256 mA

Figure 9-30. ADCIBAT Register (I^2C address = 29/28h)

7	6	5	4	3	2	1	0
Reserved	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Reserved	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-41. ADCIBAT Register (I^2C address = 29h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R		Not used. Value ignored.
6-0		R		7-bit Digital Output of Battery Charge Current

Table 9-42. ADCIBAT Register (I^2C address = 28h) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R		Not used. Value ignored.
6-0		R		7-bit Digital Output of Battery Discharge Current

9.6.11 ADCIINCMPIN Register (I²C address = 2B/2Ah)

- IIN: Full range: 12.75 A, LSB: 50 mA. For 10mΩ sense resistor, IIN full range = 6.4A
- CMPIN: Full range: 3.06 V, LSB: 12 mV

Figure 9-31. ADCIINCMPIN Register (I²C address = 2B/2Ah)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-43. ADCIINCMPIN Register (I²C address = 2Bh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Input Current

Table 9-44. ADCIINCMPIN Register (I²C address = 2Ah) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of CMPIN voltage

9.6.12 ADCVSYSVBAT Register (I^2C address = 2D/2Ch)

- VSYS: Full range: 2.88 V to 19.2 V, LSB: 64 mV
- VBAT: Full range: 2.88 V to 19.2 V, LSB: 64 mV

Figure 9-32. ADCVSYSVBAT Register (I^2C address = 2D/2Ch)

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-45. ADCVSYSVBAT Register (I^2C address = 2Dh) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of System Voltage

Table 9-46. ADCVSYSVBAT Register (I^2C address = 2Ch) Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0		R		8-bit Digital Output of Battery Voltage

9.6.13 ID Registers

9.6.13.1 ManufactureID Register (I²C address = 2Eh) [reset = 0040h]

Figure 9-33. ManufactureID Register (I²C address = 2Eh) [reset = 0040h]

7-0
MANUFACTURE_ID
R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-47. ManufactureID Register Field Descriptions

I2C 2Eh	FIELD	TYPE	RESET	DESCRIPTION (READ ONLY)
7-0	MANUFACTURE_ID	R		40h

9.6.13.2 Device ID (DeviceAddress) Register (I²C address = 2Fh) [reset = 0h]

Figure 9-34. Device ID (DeviceAddress) Register (I²C address = 2Fh) [reset = 0h]

7-0
DEVICE_ID
R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-48. Device ID (DeviceAddress) Register Field Descriptions

I2C 2Fh	FIELD	TYPE	RESET	DESCRIPTION (READ ONLY)
7-0	DEVICE_ID	R	0b	I2C: 88h (BQ25713); 8Ah (BQ25713B)

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The BQ2571xEVM-017 evaluation module (EVM) is a complete charger module for evaluating the BQ25713/ BQ25713B. The application curves were taken using the BQ2571xEVM-017. Refer to the EVM User's Guide for EVM information.

10.2 Typical Application

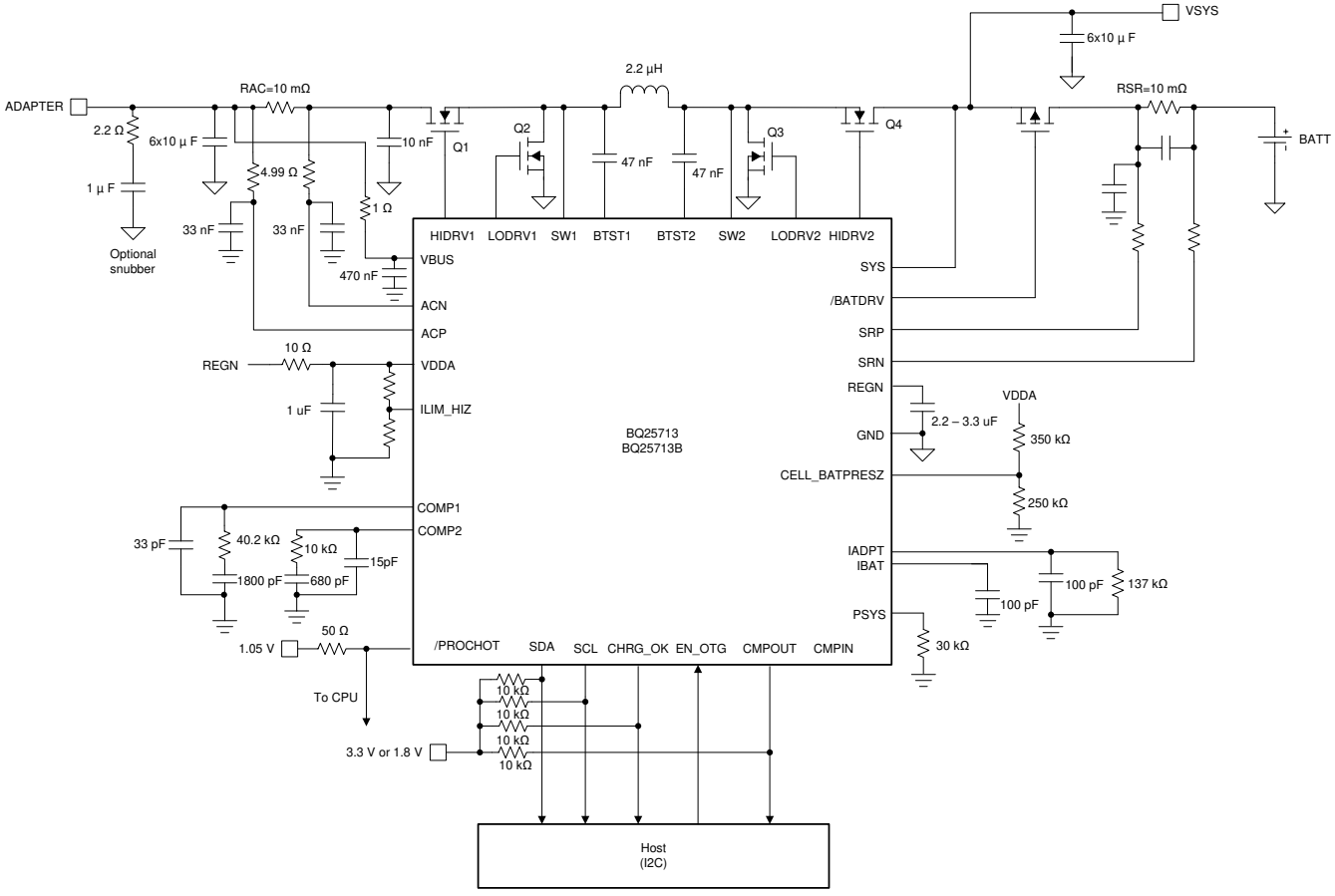


Figure 10-1. Application Diagram

10.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage(2)	3.5 V < Adapter Voltage < 24 V
Input Current Limit (2)	3.2 A for 65 W adapter
Battery Charge Voltage(1)	8400 mV for 2s battery
Battery Charge Current(1)	3072 mA for 2s battery

DESIGN PARAMETER	EXAMPLE VALUE
Minimum System Voltage(1)	6144 mV for 2s battery

(1) Refer to battery specification for settings.
(2) Refer to adapter specification for settings for Input Voltage and Input Current Limit.

10.2.2 Detailed Design Procedure

The parameters are configurable using the evaluation software. The simplified application circuit (see Figure 10-1, as the application diagram) shows the minimum component requirements. Inductor, capacitor, and MOSFET selection are explained in the rest of this section. Refer to the EVM User's Guide for the complete application schematic.

10.2.2.1 ACP-ACN Input Filter

The BQ25713/BQ25713B has average current mode control. The input current sensing through ACP/ACN is critical to recover inductor current ripple. Parasitic inductance on board will generate high frequency ringing on ACP-ACN which overwhelms converter sensed inductor current information, so it is difficult to manage parasitic inductance created based on different PCB layout. Bigger parasitic inductance will generate bigger sense current ringing which will cause the average current control loop to go into oscillation.

For real system board condition, we suggest to use below circuit design to get best result and filter noise induced from different PCB parasitic factor. With time constant of filter from 47 nsec to 200 nsec, the filtering on ringing is effective and in the meantime, the delay of on the sensed signal is small and therefore poses no concern for average current mode control.

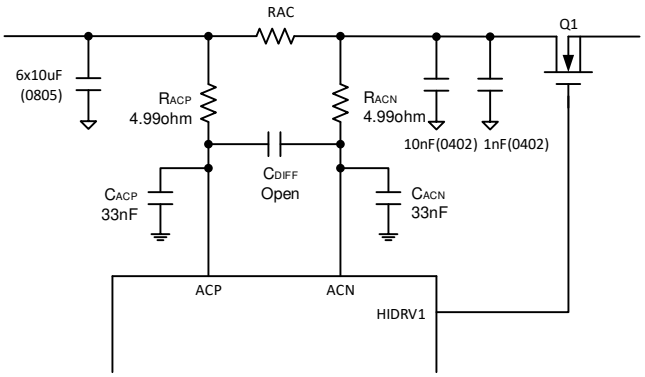


Figure 10-2. ACN-ACP Input Filter

10.2.2.2 Inductor Selection

The BQ25713/BQ25713B has two selectable fixed switching frequency. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \tag{3}$$

The inductor ripple current in buck operation depends on input voltage (V_{IN}), duty cycle ($D_{BUCK} = V_{OUT}/V_{IN}$), switching frequency ($f_S$) and inductance (L):

$$I_{RIPPLE\_BUCK} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \tag{4}$$

During boost operation, the duty cycle is:

$D_{BOOST} = 1 – (V_{IN}/V_{BAT})$

and the ripple current is:

$I_{RIPPLE\_BOOST} = (VIN \times D_{BOOST}) / (f_S \times L)$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9 V to 12.6 V for 3-cell battery pack. For 20-V adapter voltage, 10-V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12 V to 16.8 V, and 12-V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

10.2.2.3 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current (plus system current there is any system load) when duty cycle is 0.5 in buck mode. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by Equation 5:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (5)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed in front of R_{AC} current sensing and as close as possible to the power stage half bridge MOSFETs. Capacitance after R_{AC} before power stage half bridge should be limited to 10 nF + 1 nF referring to Figure 10-2. Because too large capacitance after R_{AC} could filter out R_{AC} current sensing ripple information. Voltage rating of the capacitor must be higher than normal input voltage level, 25-V rating or higher capacitor is preferred for 19-V to 20-V input voltage. The minimum input effective capacitance recommendation is shown in Table 10-1.

Ceramic capacitors (MLCC) show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's datasheet about the derating performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required effective capacitance value at the operating point. Considering the 25 V 0603 package MLCC capacitance derating under 19-V to 20-V input voltage, the recommended practical capacitors configuration can also be found in Table 10-1. Tantalum capacitors (POSCAP) can avoid dc-bias effect and temperature variation effect which is recommended for 90 W to 130 W higher power application.

Table 10-1. Minimum Input Capacitance Requirement

Input Capacitors VS Total Input Power	65W	90W	130W
Minimum effective input capacitance	4 µF	6 µF	13 µF
Minimum practical input capacitors configuration	4*10 µF (0603 25 V MLCC)	6*10 µF (0603 25 V MLCC)	3*10 µF (0603 25 V MLCC) 1* 10 µF (25 V to 35 V POSCAP)

10.2.2.4 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 10 kHz and 20 kHz. The preferred ceramic capacitor is 25-V X7R or X5R for output capacitor. Minimum 7 pcs of 10-µF 0603 package capacitor is suggested to be placed as close as possible to Q3&Q4 half bridge (between Q4 drain and Q3 source terminal). Total minimum output effective capacitance along VSYS distribution line is 50 µF refers to Table 10-2. Recommend to place minimum 20-µF MLCC capacitors after the charge current sense resistor for best stability.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the derating performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required capacitance value at the

operating point. Considering the 25-V 0603 package MLCC capacitance derating under 21-V to 23-V output voltage, the recommended practical capacitors configuration at VSYS output terminal can also be found in Table 10-2. Tantalum capacitors (POSCAP) can avoid dc-bias effect and temperature variation effect which are recommended to be used along VSYS output distribution line to meet total minimum effective output capacitance requirement.

Table 10-2. Minimum Output Capacitance Requirement

OUTPUT CAPACITORS VS TOTAL INPUT POWER	65W	90W	130W
Minimum Effective Output Capacitance	50 µF	50 µF	50 µF
Minimum output capacitors at charger VSYS output terminal	7*10 µF (0603 25 V MLCC)	9*10 µF (0603 25 V MLCC)	9*10 µF (0603 25 V MLCC)
Additional output capacitors along VSYS distribution line	2*22 µF (25 V~35 V POSCAP)	2*22 µF (25 V~35 V POSCAP)	2*22 µF (25 V~35 V POSCAP)

10.2.2.5 Power MOSFETs Selection

Four external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6 V of gate drive voltage. 30 V or higher voltage rating MOSFETs are preferred for 19 V - 20 V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For the bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD};\ FOM_{bottom} = R_{DS(on)} \times Q_G \tag{6}$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance ($R_{DS(ON)}$), input voltage (V_{IN}), switching frequency (f_S), turn on time (t_{on}) and turn off time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_{on} + t_{off}) \times f_s \tag{7}$$

The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100°C junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}},\quad t_{off} = \frac{Q_{SW}}{I_{off}} \tag{8}$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current and I_{off} is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \tag{9}$$

Gate driving current can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}) and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \tag{10}$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

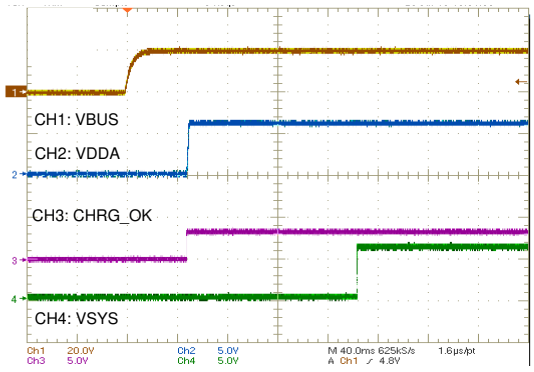
$$P_{bottom} = (1 - D) \times I_{CHG}^{2} \times R_{DS(on)} \tag{11}$$

When charger operates in non-synchronous mode, the bottom-side MOSFET is off. As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The body diode power loss depends on its forward voltage drop (V_F), non-synchronous mode charging current ($I_{NONSYNC}$), and duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D) \tag{12}$$

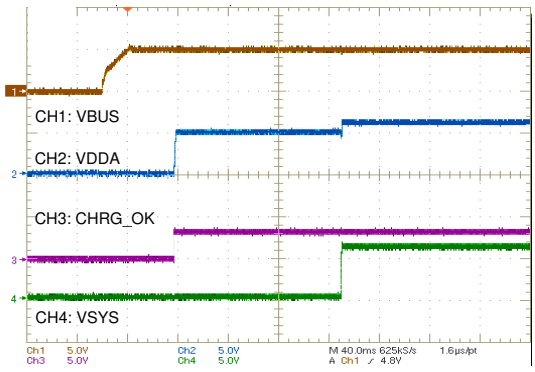
The maximum charging current in non-synchronous mode can be up to 0.25 A for a 10-mΩ charging current sensing resistor or 0.5 A if battery voltage is below 2.5 V. The minimum duty cycle happens at lowest battery voltage. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

10.2.3 Application Curves



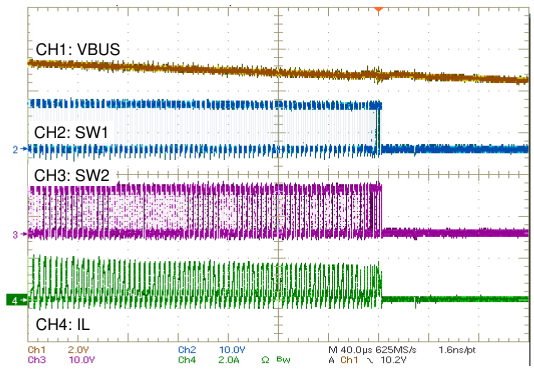
2-cell without battery

Figure 10-3. Power Up from 20 V



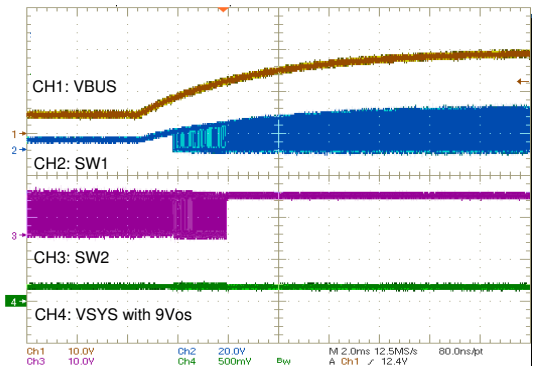
2-cell without battery

Figure 10-4. Power Up from 5 V



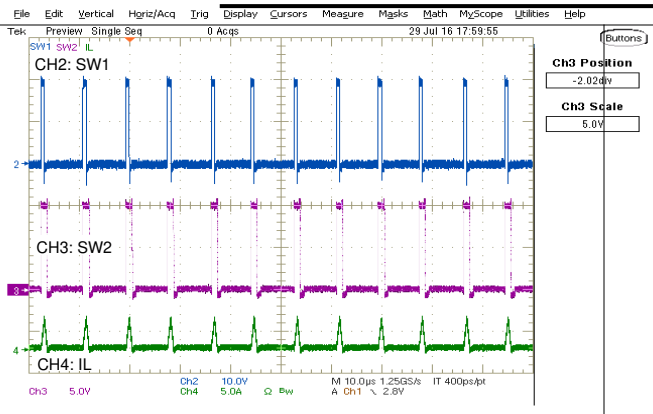
3-cell VBAT = 10 V

Figure 10-5. Power Off from 12 V



VBUS 5 V to 20 V

Figure 10-6. System Regulation



VBUS = 20 V, VSYS = 10 V, ISYS = 200 mA
CH2: SW1, CH3: SW2, CH4: IL

Figure 10-7. PFM Operation

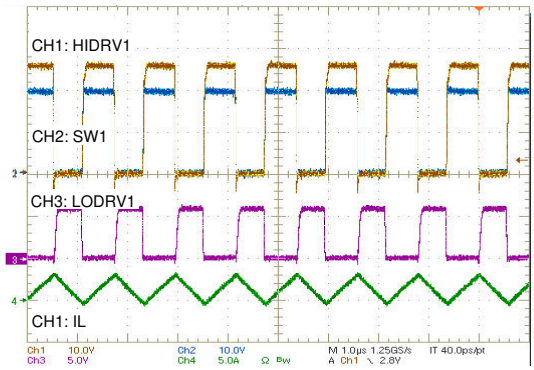
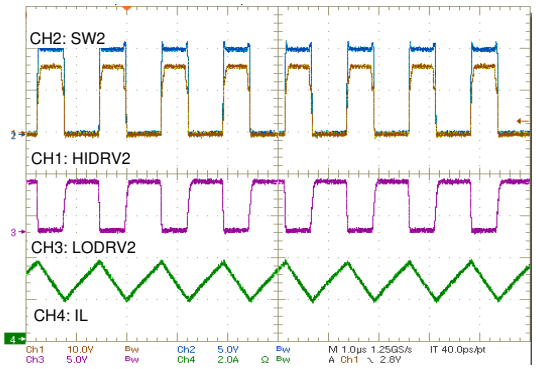
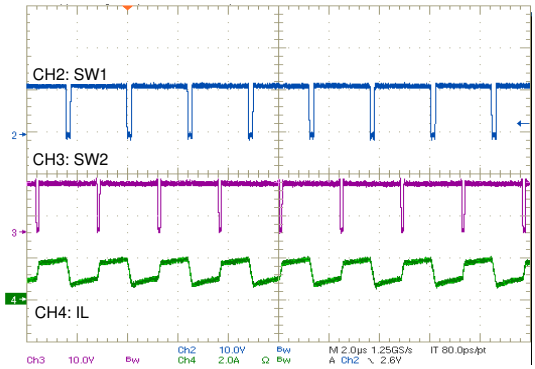


Figure 10-8. PWM Operation



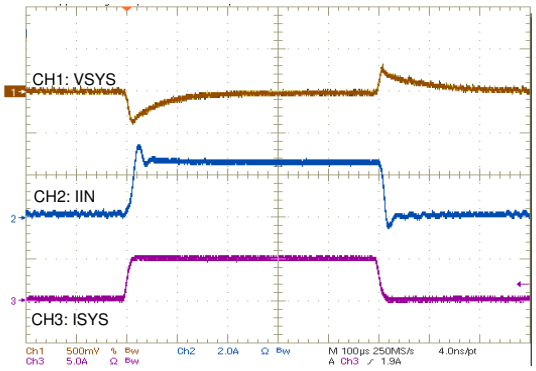
VBUS = 5 V, VBAT = 10 V

Figure 10-9. Switching During Boost Mode



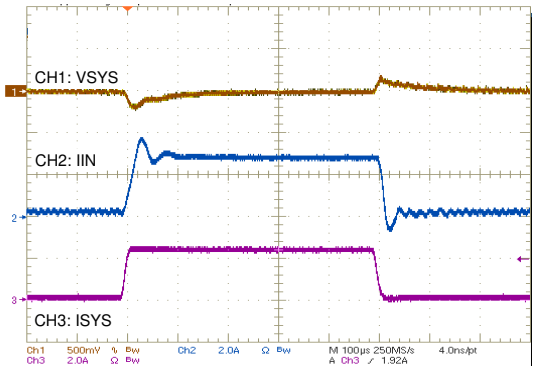
VBUS = 12 V, VBAT = 12 V

Figure 10-10. Switching During Buck Boost Mode



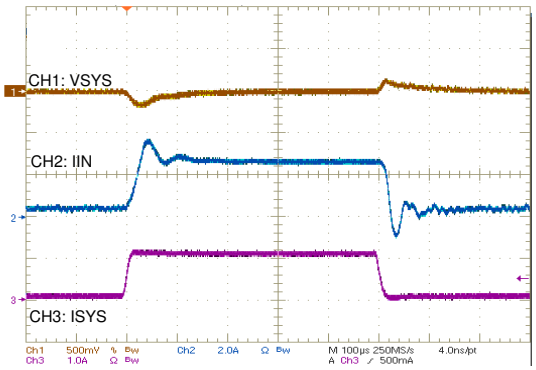
VBUS = 12 V/3.3 A, 3-cell, VSYS = 9 V, Without battery

Figure 10-11. System Regulation in Buck Mode



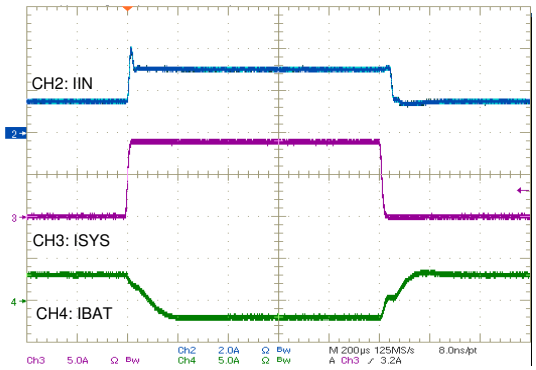
VBUS = 9 V/3.3 A, 3-cell, VSYS = 9 V, Without battery

Figure 10-12. System Regulation in Buck Boost Mode



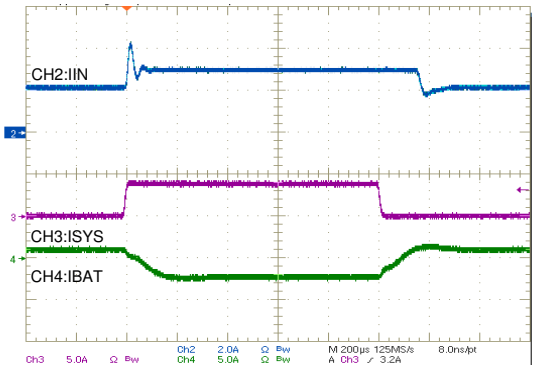
VBUS = 5 V/3.3 A, 3-cell, VSYS = 9 V, Without battery

Figure 10-13. System Regulation in Boost Mode



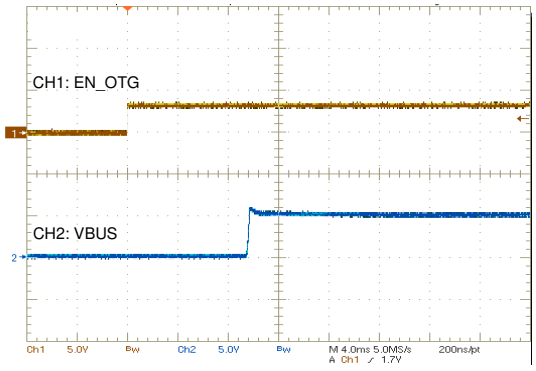
VBUS = 20 V/3.3 V, VBAT = 7.5 V

Figure 10-14. Input Current Regulation in Buck Mode



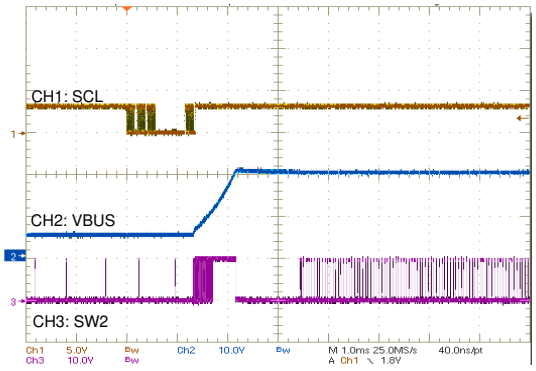
VBUS = 5 V/3.3 V, VBAT = 7.5 V

Figure 10-15. Input Current in Boost Mode



VBUS = 5 V

Figure 10-16. OTG Power Up from 8 V Battery



VBAT = 10 V, VBUS 5 V to 20 V, IOTG = 500 mA

Figure 10-17. OTG Voltage Ramp Up

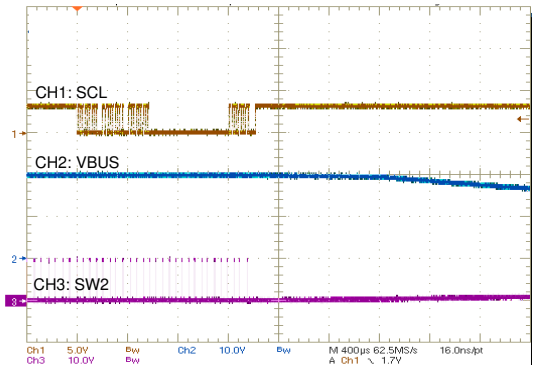
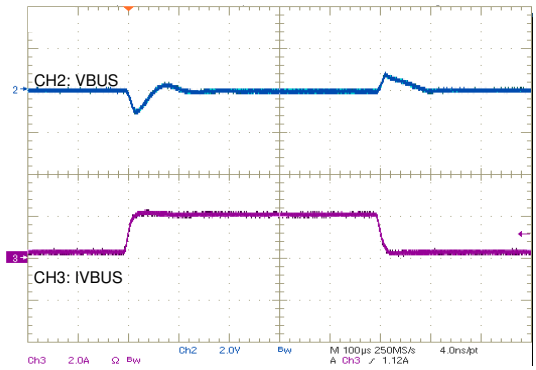


Figure 10-18. OTG Power Off



VBAT = 10 V, VBUS = 20 V

Figure 10-19. OTG Load Transient

11 Power Supply Recommendations

The valid adapter range is from 3.5 V (V_{VBUS_CONVEN}) to 24 V (ACOV) with at least 500-mA current rating. When CHRG_OK goes HIGH, the system is powered from adapter through the charger. When adapter is removed, the system is connected to battery through BATFET. Typically the battery depletion threshold should be greater than the minimum system voltage so that the battery capacity can be fully utilized for maximum battery life.

12 Layout

12.1 Layout Guidelines

Proper layout of the components to minimize high frequency current path loop (see Section 12.2) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout.

Table 12-1. PCB Layout Guidelines

RULES	COMPONENTS	FUNCTION	IMPACT	GUIDELINES
1		PCB layer stack up	Thermal, efficiency, signal integrity	Multi- layer PCB is suggested. Allocate at least one ground layer. The BQ257XXEVM uses a 4-layer PCB (top layer, ground layer, signal layer and bottom layer).
2	CBUS, RAC, Q1, Q2	Input loop	High frequency noise, ripple	VBUS capacitors, RAC, Q1 and Q2 form a small loop 1. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CBUS to the other side of PCB for high density design. After RAC before Q1 and Q2 power stage recommend to put 10 nF + 1 nF (0402 package) decoupling capacitors as close as possible to IC to decoupling switching loop high frequency noise.
3	R_{AC}, Q1, L1, Q4	Current path	Efficiency	The current path from VBUS to VSYS, through R_{AC}, Q1, L1, Q4, has low impedance. Pay attention to via resistance if they are not on the same side. The number of vias can be estimated as 1 to 2A/via for a 10-mil via with 1 oz. copper thickness.
4	CSYS, Q3, Q4	Output loop	High frequency noise, ripple	VSYS capacitors, Q3 and Q4 form a small loop 2. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CSYS to the other side of PCB for high density design.
5	QBAT, R_{SR}	Current path	Efficiency, battery voltage detection	Place QBAT and R_{SR} near the battery terminal. The current path from VBAT to VSYS, through $R_{SR}$and QBAT, has low impedance. Pay attention to via resistance if they are not on the same side. The device detects the battery voltage through SRN near battery terminal.
6	Q1, Q2, L1, Q3, Q4	Power stage	Thermal, efficiency	Place Q1, Q2, L1, Q3 and Q4 next to each other. Allow enough copper area for thermal dissipation. The copper area is suggested to be 2x to 4x of the pad size. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat.
7	R_{AC}, R_{SR}	Current sense	Regulation accuracy	Use Kelvin-sensing technique for R_{AC} and R_{SR} current sense resistors. Connect the current sense traces to the center of the pads, and run current sense traces as differential pairs.
8	Small capacitors	IC bypass caps	Noise, jittering, ripple	Place VBUS cap, VCC cap, REGN caps near IC.
9	BST capacitors	HS gate drive	High frequency noise, ripple	Place HS MOSFET boost strap circuit capacitor close to IC and on the same side of PCB board. Capacitors SW1/2 nodes are recommended to use wide copper polygon to connect to power stage and capacitors BST1/2 node are recommended to use at least 8mil trace to connected to IC BST1/2 pins.
10		Ground partition	Measurement accuracy, regulation accuracy, jitters, ripple	Separate analog ground(AGND) and power grounds(PGND) is preferred. PGND should be used for all power stage related ground net. AGND should be used for all sensing, compensation and control network ground for example ACP/ACN/COMP1/ COMP2/CMPIN/CMPOUT/IADPT/IBAT/PSYS. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. If possible, use dedicated COMP1, COMP2 AGND traces. Connect analog ground and power ground together using power pad as the single ground connection point.

12.2 Layout Example

12.2.1 Layout Example Reference Top View

Based on the above layout guidelines, the buck-boost charger layout example top view is shown below including all the key power components.

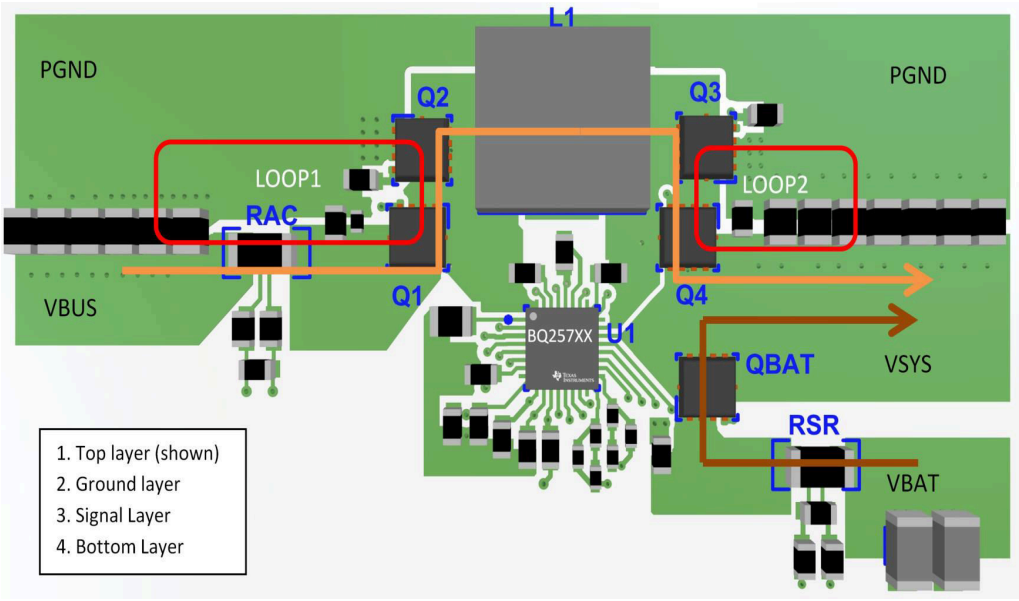


Figure 12-1. Buck-Boost Charger Layout Reference Example Top View

12.2.2 Inner Layer Layout and Routing Example

For both input sensing resistor and charging current sensing resistor, differential sensing and routing method are suggested and highlighted in below figure. Use wide trace for gate drive traces, minimum 15 mil trace width. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. Suggest using dedicated COMP1, COMP2 analog ground traces shown in below figure.

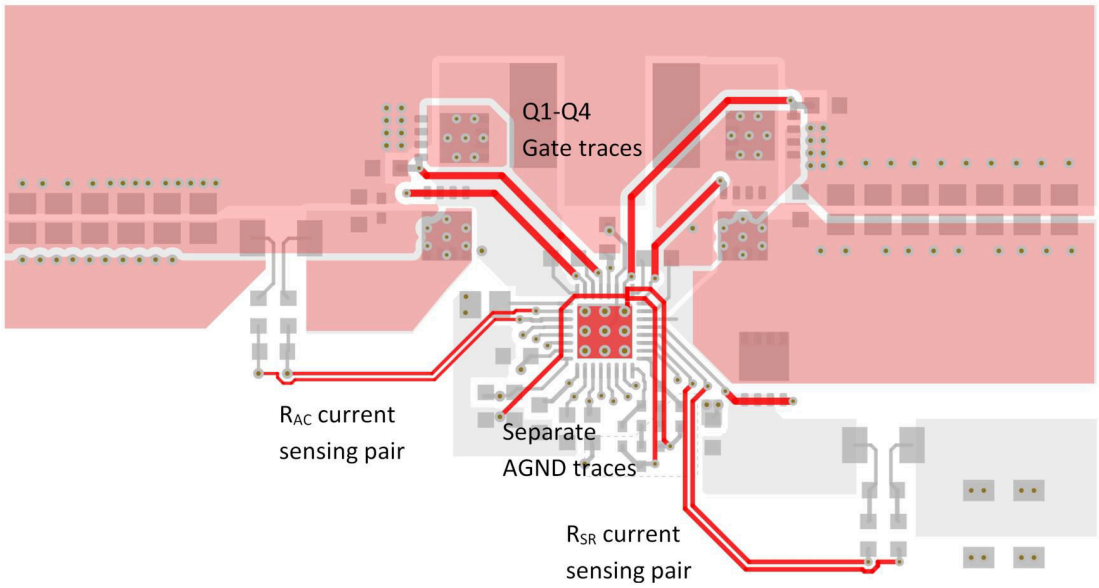


Figure 12-2. Buck-Boost Charger Gate Drive/Current Sensing/AGND Signal Layer Routing Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Package Thermal Metrics Application Report*
- *BQ2571x Evaluation Module User's Guide*
- *QFN/SON PCB Attachment Application Report*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.5 Trademarks

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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

1-Jan-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25713BRSNR	ACTIVE	QFN	RSN	32	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BQ 25713B	Samples
BQ25713BRSNT	ACTIVE	QFN	RSN	32	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BQ 25713B	Samples
BQ25713RSNR	ACTIVE	QFN	RSN	32	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BQ25713	Samples
BQ25713RSNT	ACTIVE	QFN	RSN	32	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BQ25713	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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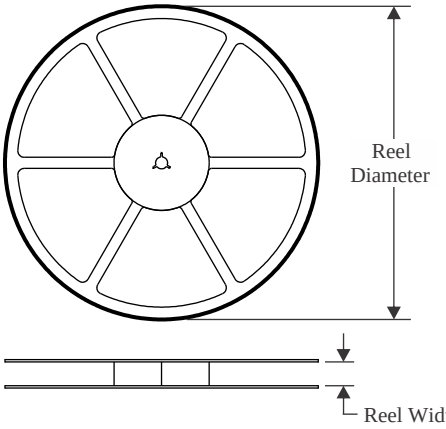
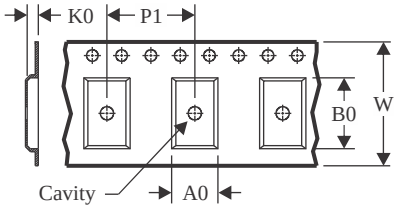
TAPE AND REEL INFORMATION

REEL DIMENSIONS

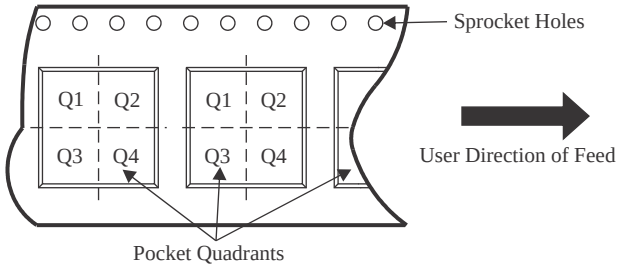


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

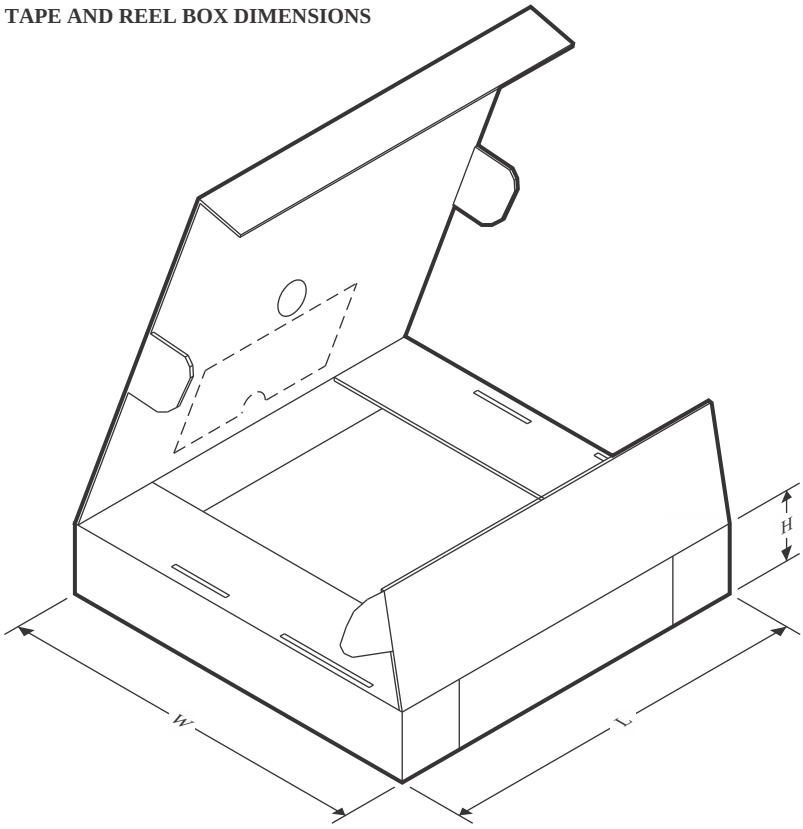
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25713BRSNR	QFN	RSN	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25713BRSNR	QFN	RSN	32	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
BQ25713BRSNT	QFN	RSN	32	250	180.0	12.5	4.35	4.35	1.1	8.0	12.0	Q2
BQ25713BRSNT	QFN	RSN	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25713RSNR	QFN	RSN	32	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
BQ25713RSNR	QFN	RSN	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25713RSNT	QFN	RSN	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25713RSNT	QFN	RSN	32	250	180.0	12.5	4.35	4.35	1.1	8.0	12.0	Q2

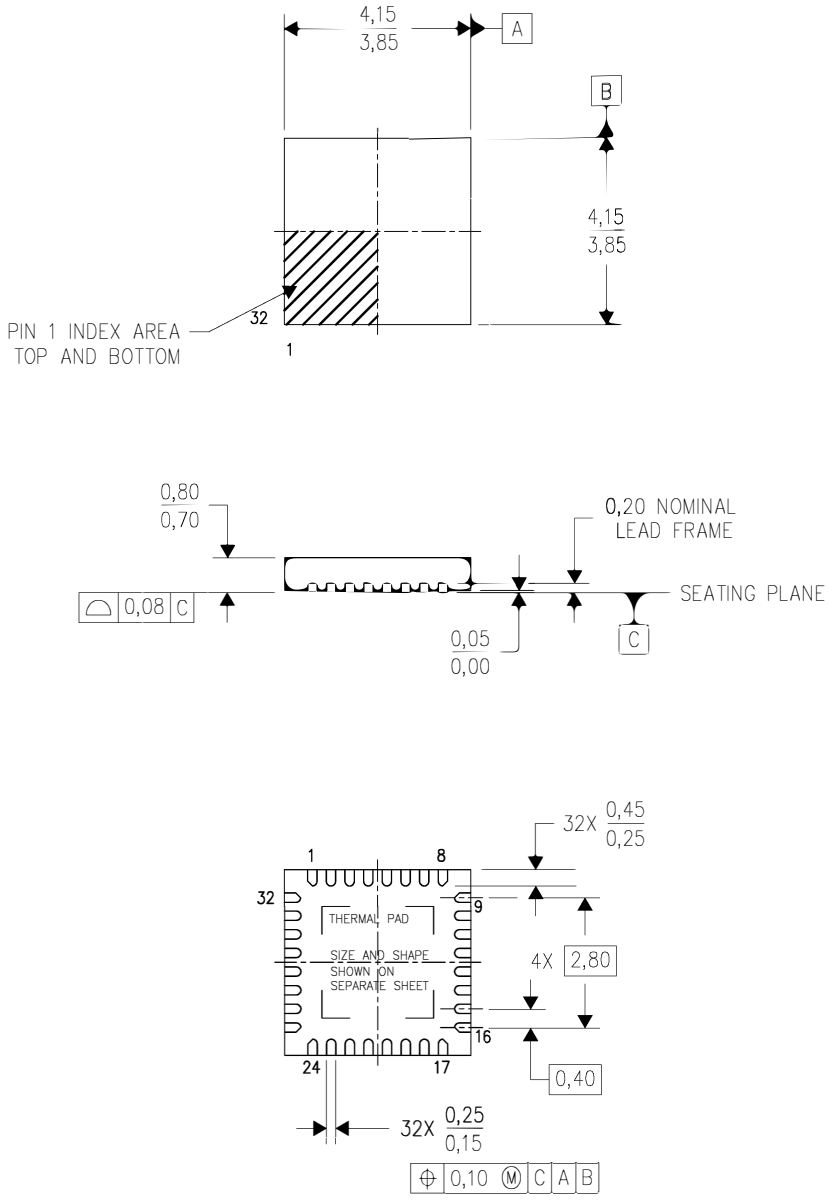
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25713BRSNR	QFN	RSN	32	3000	367.0	367.0	35.0
BQ25713BRSNR	QFN	RSN	32	3000	338.0	355.0	50.0
BQ25713BRSNT	QFN	RSN	32	250	205.0	200.0	33.0
BQ25713BRSNT	QFN	RSN	32	250	210.0	185.0	35.0
BQ25713RSNR	QFN	RSN	32	3000	338.0	355.0	50.0
BQ25713RSNR	QFN	RSN	32	3000	367.0	367.0	35.0
BQ25713RSNT	QFN	RSN	32	250	210.0	185.0	35.0
BQ25713RSNT	QFN	RSN	32	250	205.0	200.0	33.0

RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207561/C 08/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

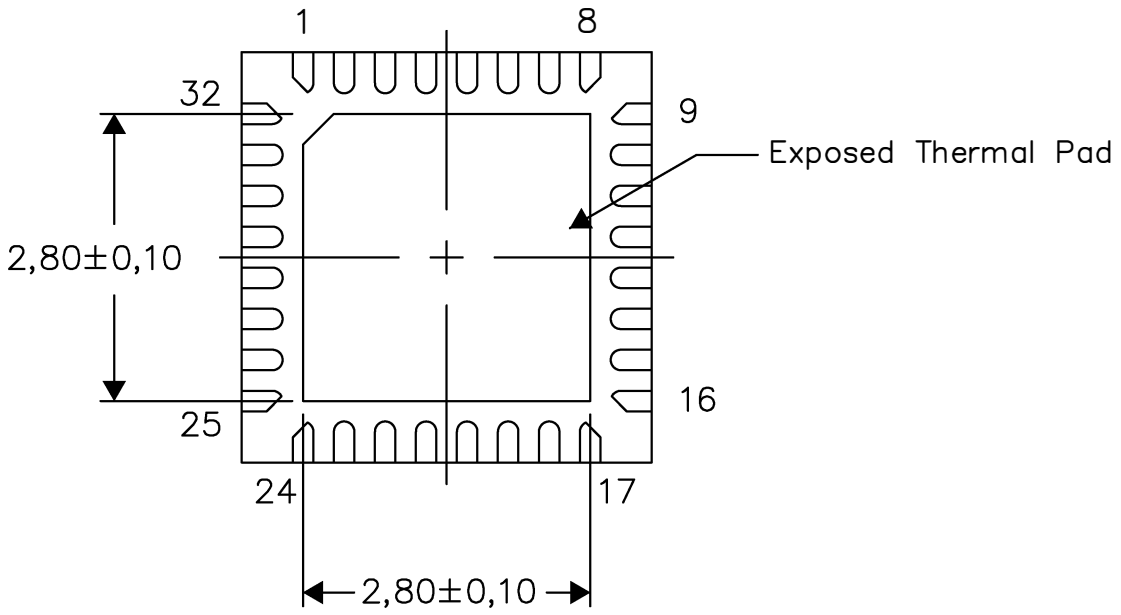
RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



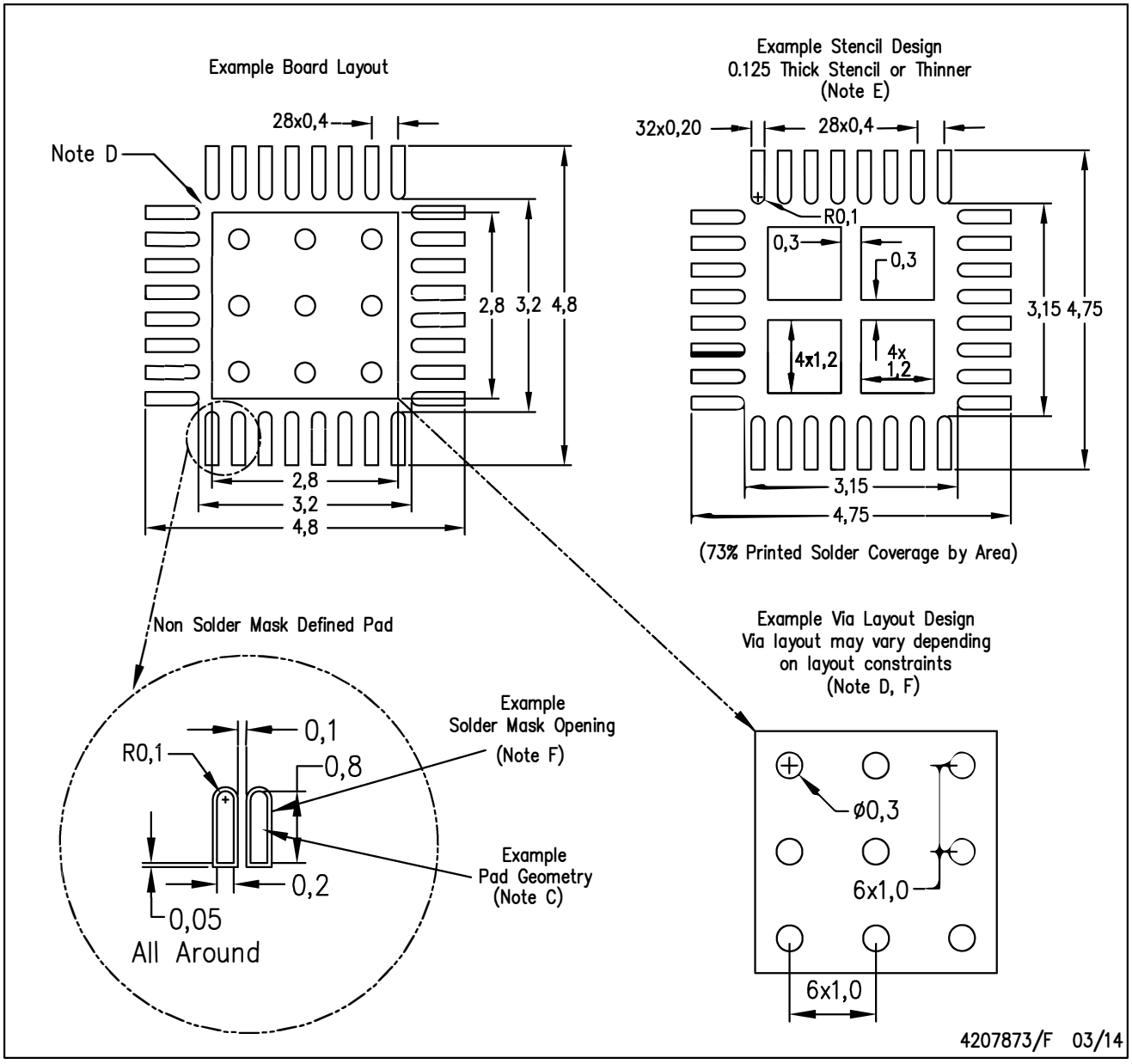
Bottom View

Exposed Thermal Pad Dimensions

4209775–2/F 03/14

NOTE: All linear dimensions are in millimeters

RSN (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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