3-Channel Simple Power Sequencer with Adjustable Timing Control

Features

- Input Voltage Range: 2.7 V to 5.5V
- Power-Up and Power-Down Sequence Control
- Single Enable Control Signal Input Channel
- Three Power Sequence Channels:
  - Open-Drain Output
  - Adjustable Timing Controlled by Capacitor
  - Support Invert Output
- Support Cascaded Device Output
- Low Power Consumption
- Junction Temperature: –40°C to +125°C
- Small MSOP8 Package

Applications

- Video Surveillance
- Network Equipment and Servers
- Industrial Control
- FPGA/ASIC/CPLD Power Sequence Control
- Multi-channel Power Supply Sequence Control

Description

The TPK1031 series products are simple power sequencers, which provide power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1031 series support maximum three devices cascaded to control sequence of nine-channel power rails in one system.

The TPK1031 series products have three open-drain output channels, and all the channels can be pulled up to any required voltage level equal or lower than V_{CC}. When the TPK1031 series are enabled with EN pin goes high, the three output channels toggle with the sequence of FLAG1-FLAG2-FLAG3 after the delay period individually set by the external capacitor; when the TPK1031 series are disabled with EN pin goes low, the three output channels toggle following a reverse sequence after the delay period individually set by the external capacitor.

The TPK1031 series products provide small MSOP8 package with guaranteed junction temperature range (T_J) from –40°C to +125°C.

Typical Application Circuit

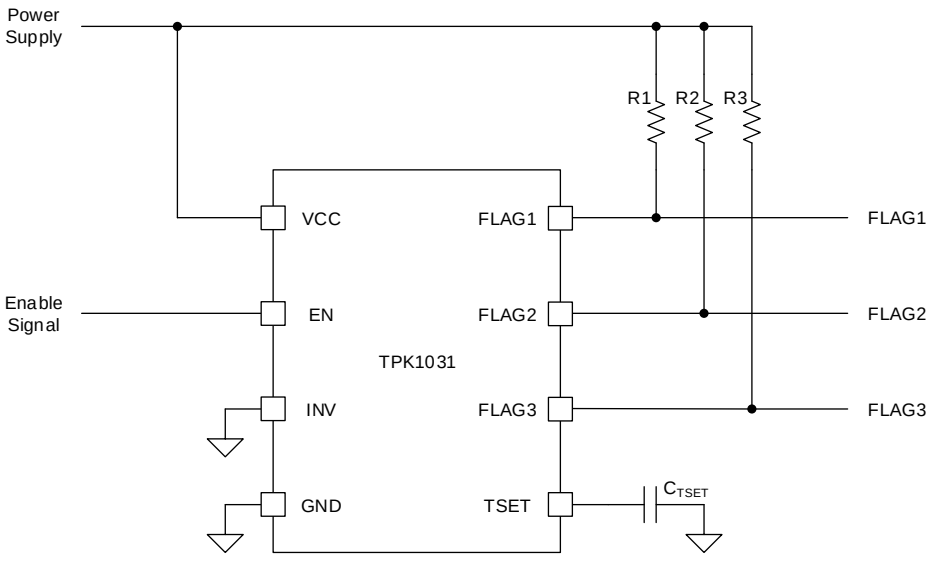


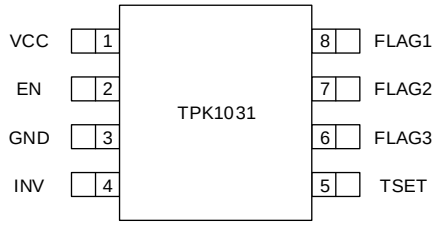
Table of Contents

Revision History

Date	Revision	Notes
2019/05/31	Rev. Pre	Preliminary Version
2019/08/31	Rev.A.0	Initial Release
2020/10/26	Rev.A.1	Correct the Mistake Pin Number of EN from 3 to 2 (Page 5)
2021/12/05	Rev.A.2	Add Tape and Reel Information.

Pin Configuration and Functions

8-Pin MSOP



Pin Functions

Pin		I/O	Description
No.	Name		
2	EN	I	Device enable pin.
8	FLAG1	O	Open-drain output pin.
7	FLAG 2	O	Open-drain output pin.
6	FLAG 3	O	Open-drain output pin.
3	GND	–	Ground reference pin.
4	INV	I	Invert output set pin.
5	TSET	O	Delay time set pin.
1	VCC	I	Input power supply.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Input Voltage	VCC, EN, INV, TSET	−0.3	6	V
Output Voltage	FLAG1, FLAG2, FLAG3	−0.3	6	V
T_J	Maximum Junction Temperature	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001(1)	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
VCC	2.7		5.5	V
EN, INV, TSET	0		V_{CC} + 0.3	V
FLAG1, FLAG2, FLAG3	0		V_{CC} + 0.3	V

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
MSOP8	247	118	°C/W

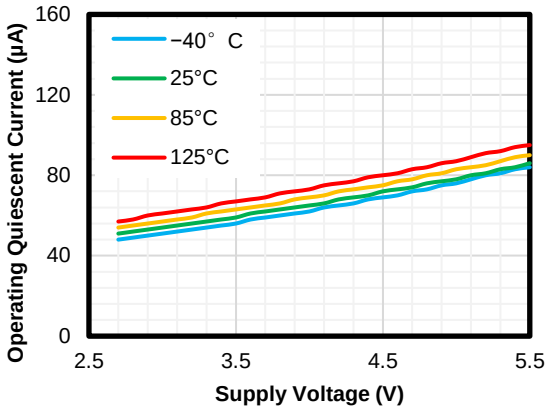
Electrical Characteristics

T_J = −40°C to +125°C (typical value at T_J = +25°C), V_{CC} = 3.3 V, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Supply						
V_{CC}	Input supply voltage		2.7		5.5	V
I_{CC}	Operating quiescent current	INV = GND		55	100	μA
		INV = V_{CC}		85	130	μA
Enable						
V_{EN_TH}	EN pin threshold voltage		1	1.23	1.5	V
I_{EN}	EN pin pull-up current	V_{EN} = 0 V	5	6.5	8	μA
Open-Drain Output						
V_{OL}	FLAGx pin output low level	I_{FLAGx} = 1.2 mA	0		0.4	V
I_{FLAGx}	FLAGx pin leakage current	V_{FLAGx} = 3.3 V		0.3	1	μA
Open-Drain Output						
V_{OL}	FLAGx pin output low level	I_{FLAGx} = 1.2 mA	0		0.4	V
I_{FLAGx}	FLAGx pin leakage current	V_{FLAGx} = 3.3 V		0.3	1	μA
Delay Time Setup						
I_{TSET_SOURCE}	TSET pin source current		7	11	15	μA
I_{TSET_SINK}	TSET pin sink current		7	11	15	μA
V_{TSET_H}	TSET pin high-level threshold		1	1.14	1.4	V
V_{TSET_L}	TSET pin low-level threshold		0.4	0.5	0.7	V
T_{CLK}	Clock cycle	C_{TSET} = 10 nF	0.9	1.16	1.4	ms
Timing Delays						
t_{d1}, t_{d4}	Timing delays		9		10	Cycles
t_{d2}, t_{d3}, t_{d5}, t_{d6}	Timing delays			8		Cycles
Invert Output Setup						
V_{INV_IH}	Invert pin high-level input		90%			Of V_{CC}
V_{INV_IL}	Invert pin low-level input				10%	Of V_{CC}

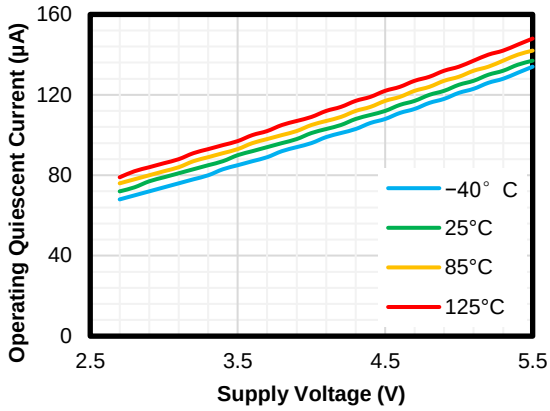
Typical Performance Characteristics

T_J = −40°C to +125°C (typical value at T_J = +25°C), V_{CC} = 3.3 V, unless otherwise noted.



INV = GND

Figure 1 Quiescent Current vs Supply Voltage



INV = V_{CC}

Figure 2 Quiescent Current vs Supply Voltage

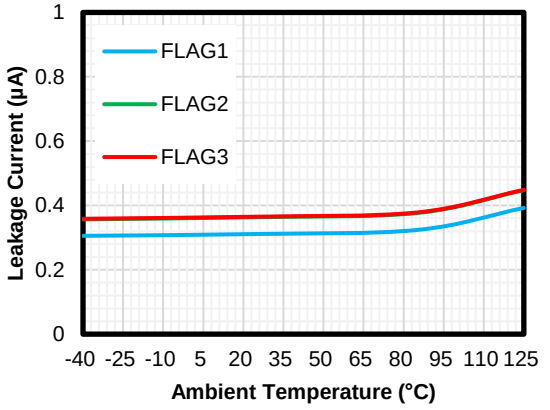


Figure 3 FLAGx Leakage Current vs Temperature

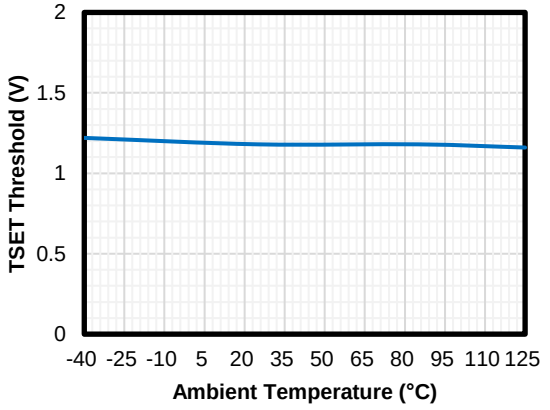
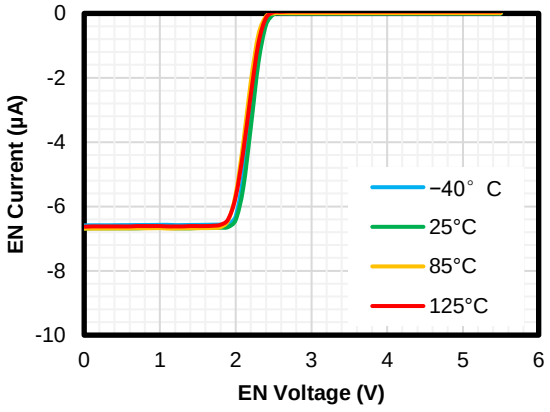
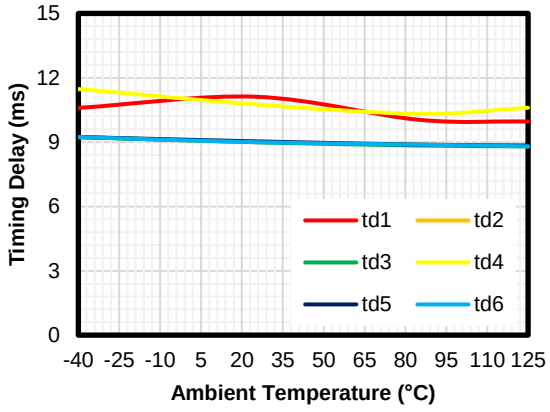


Figure 4 TSET Threshold vs Temperature



INV = GND

Figure 5 EN Input Current vs EN Voltage



C_{TSET} = 10 nF

Figure 6 Timing Delay vs Temperature

Detailed Description

Overview

The TPK1031 series products are simple power sequencers, which provide power-up and power-down sequence control of multi-channel power supplies. Furthermore, the TPK1031 series support maximum three devices cascaded to control sequence of nine-channel power rails in one system.

The TPK1031 series products have three open-drain output channels, and all the channels can be pulled up to any required voltage level equal or lower than V_{CC}. When the TPK1031 series are enabled with EN pin goes high, the three output channels toggle with the sequence of FLAG1-FLAG2-FLAG3 after the delay period individually set by the external capacitor; when the TPK1031 series are disabled with EN pin goes low, the three output channels toggle following a reverse sequence after the delay period individually set by the external capacitor.

Functional Block Diagram

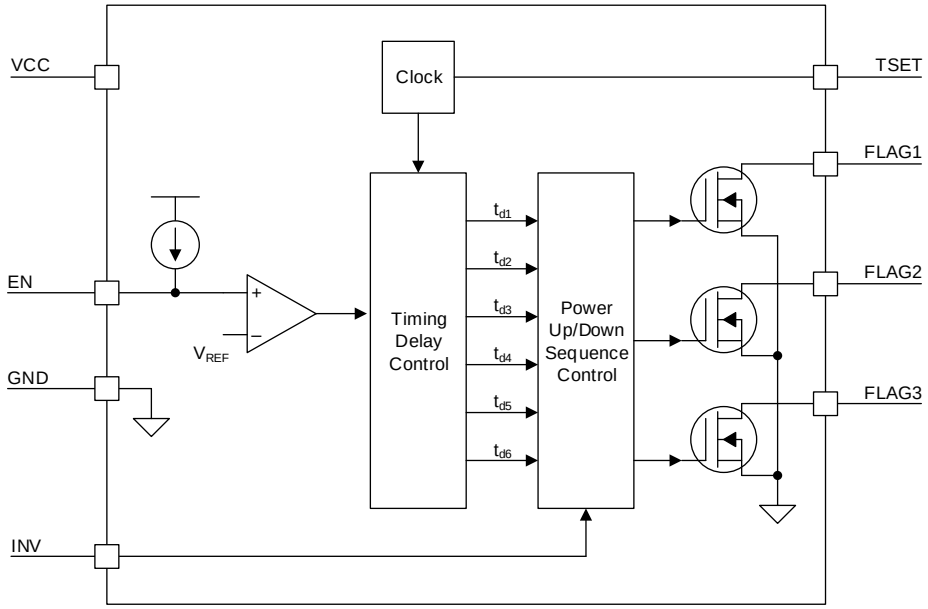


Figure 7 Functional Block Diagram

Feature Description

Device Enable (EN)

The timing sequence of TPK1031 series is controlled by the enable (EN) signal. An internal comparator connected at EN pin, with referenced to the bandgap voltage, set the enable threshold precisely at 1.23 V. With this precision enable threshold, the TPK1031 series can be enabled after a certain delay period set by external capacitor or a certain voltage value determined by external resistor divider.

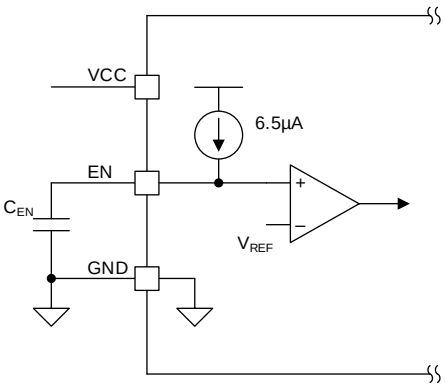


Figure 8 Using Capacitor at EN

When using a capacitor at the EN pin (Figure 8), the enable delay period can be calculated by Equation (1):

$$t_{EN\_DLY}=\frac{1.23V\times C_{EN}}{6.5\mu A} \quad (1)$$

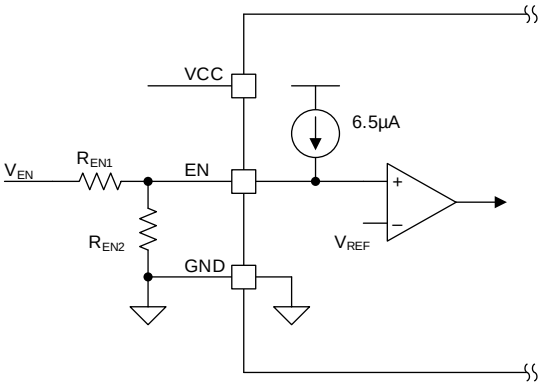


Figure 9 Using Resistor Divider at EN

When using the resistor divider at the EN pin (Figure 9), the resistor divider can be calculated by Equation (2):

$$V_{EN}=V_{EN\_TH}\times\frac{R_{EN1}+R_{EN2}}{R_{EN2}}-6.5\mu A\times R_{EN1} \quad (2)$$

The TPK1031 series also implement the EN pin de-glitch function. When there are ripple across the enable threshold at the EN pin, the device will always reset if the EN pin falls below the threshold. The timing delay only start counting at the last EN rising threshold (Figure 10).

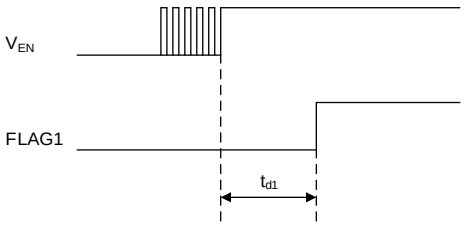


Figure 10 Enable De-glitch (INV = Low)

Inverted Output (INV)

The voltage level of TPK1031 series output flags is selectable HIGH or LOW by setting the INV voltage.

When INV = LOW,

- Output flags turn to HIGH sequentially after each timing delay period when the device enable signal comes.
- Output flags turn to LOW sequentially after each timing delay period when the device disable signal comes.

When INV = HIGH,

- Output flags turn to LOW sequentially after each timing delay period when the device enable signal comes.
- Output flags turn to HIGH sequentially after each timing delay period when the device disable signal comes.

Adjustable Timing Delay

The delay period between TPK1031 series output flags is adjustable with a small external capacitor C_{TSET} at T_{SET} pin. The TSET pin charges/discharges the capacitor C_{TSET} with about ±11 μA source/sink current, I_{TSET_SOURCE} and I_{TSET_SINK}, between voltage threshold V_{TSET_H} and V_{TSET_L}. The charging period, T_{CHG}, and discharging period, T_{DISCHG}, compose one delay clock cycle, T_{CLK}.

Figure 11 shows the delay clock cycle timing waveform.

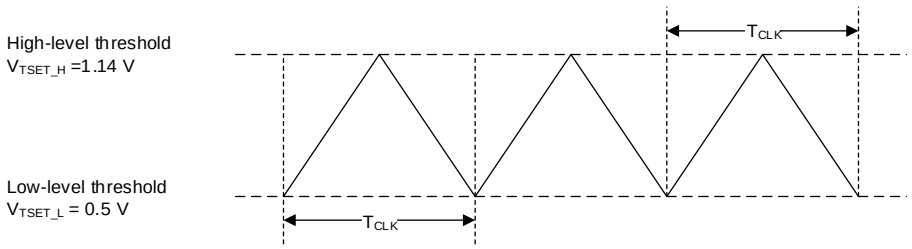


Figure 11 Delay Clock Cycle Timing Waveform

The delay clock period can be calculated by Equation (3):

$$T_{CLK}=\left(\frac{V_{TSET\_H}-V_{TSET\_L}}{I_{TSET\_SOURCE}}+\frac{V_{TSET\_H}-V_{TSET\_L}}{I_{TSET\_SINK}}\right)\times C_{TSET} \quad (3)$$

Power Sequence (FLAGx)

When the TPK1031 series devices are enabled, all the output flags will be released sequentially. The timing delay period between two adjacent flags is determined by the product of each delay clock period and the internal delay clock counter.

Figure 12 and Figure 13 show the power sequences of the output flags.

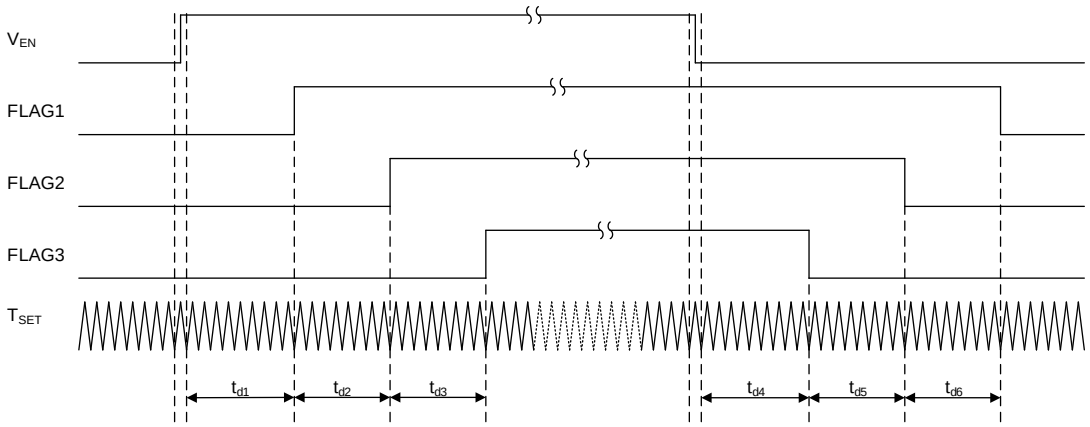


Figure 12 Power Up and Power Down Sequence when INV = LOW

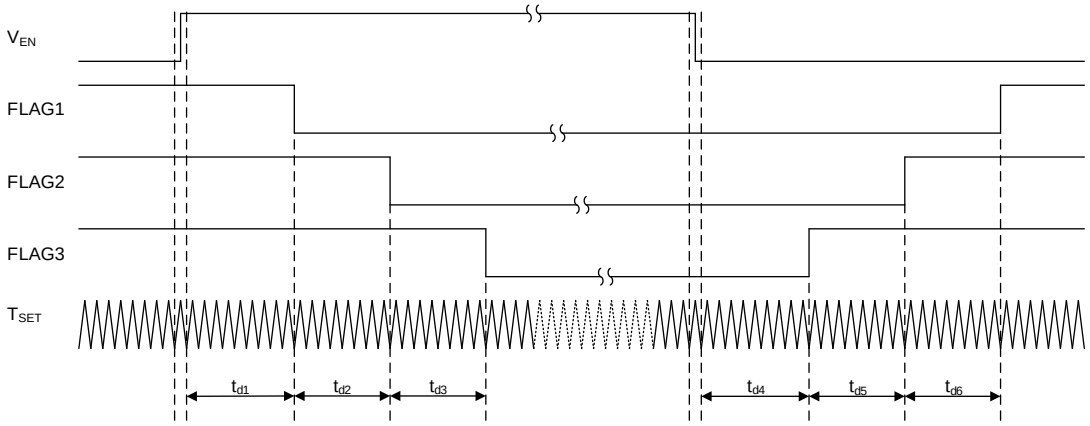


Figure 13 Power Up and Power Down Sequence when INV = HIGH

Power Sequence Interruption

When the enable signal keeps constant during the entire power up or power down sequence, the TPK1031 series devices will operate the whole sequence as shown in Figure 12 and Figure 13. However, if the enable signal falling or rising edge comes during the power up or power down sequence, the device will enter the interrupt status and initialize a new power down or power up sequence.

Figure 14 shows the power sequence with EN interruption when INV is LOW.

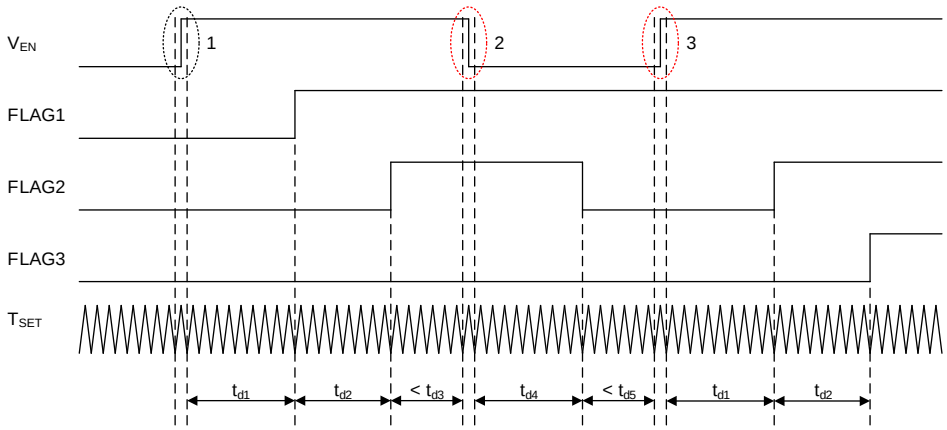


Figure 14 Power Sequence Interruption when INV = LOW

Notes:

1. Device enable signal
2. Enable interrupt during the power up sequence
3. Enable interrupt during the power down sequence

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPK1031 series products are 3-channel simple power sequencers, which provide power-up and power-down sequence control of multi-channel power supplies. The following application schematic shows a typical usage of the TPK1031 series.

Typical Application

Figure 15 and Figure 16 shows the typical application schematic of the TPK1031 series.

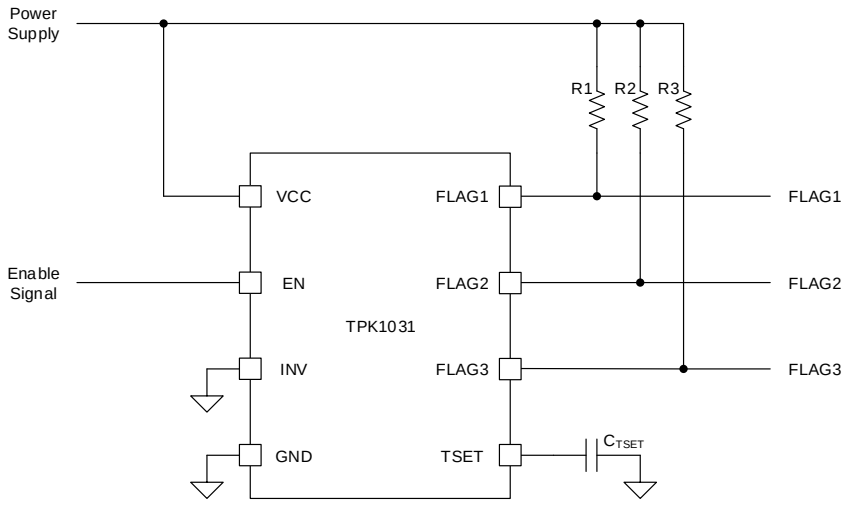


Figure 15 VCC and FLAGx with Same Power Rail

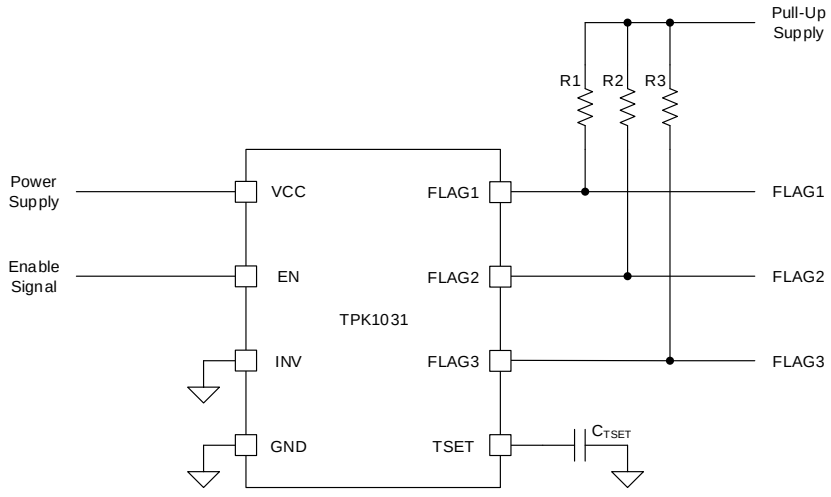


Figure 16 VCC and FLAGx with Different Power Rails

Design Parameters

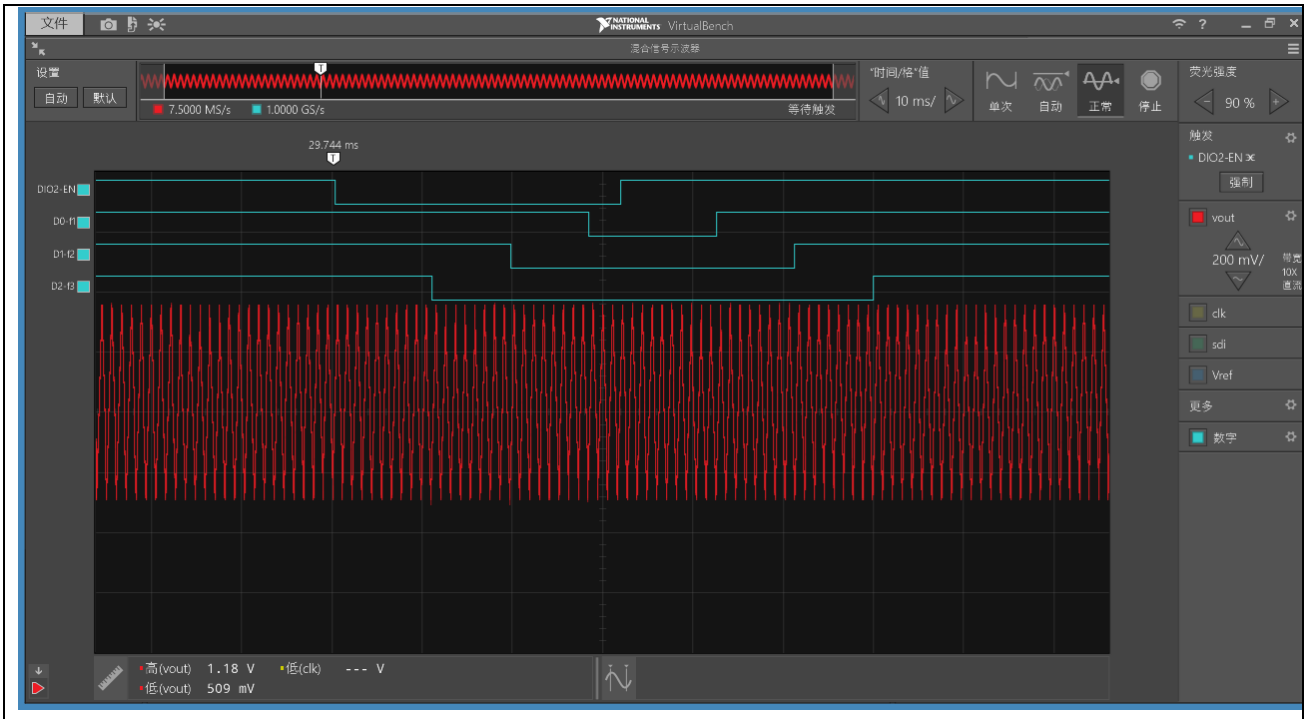
For this design example, use the parameters listed in Table 1.

Table 1 Design Parameters

PARAMETERS	VALUE
Power supply voltage range, V_{CC}	2.7 V to 5.5 V
Enable signal voltage	LOW (< 10% of V_{CC}), HIGH (>90% of V_{CC})
Pull-up resistors, R1, R2, R3	100 kΩ
Timing delay capacitor, C_{TSET} (1)	10 nF
t_{d1}, t_{d4} (1)	10.44 ms to 11.60 ms
t_{d2}, t_{d3}, t_{d6}, t_{d6} (1)	9.28 ms

(1) See Adjustable Timing Delay section for more details

Application Waveform



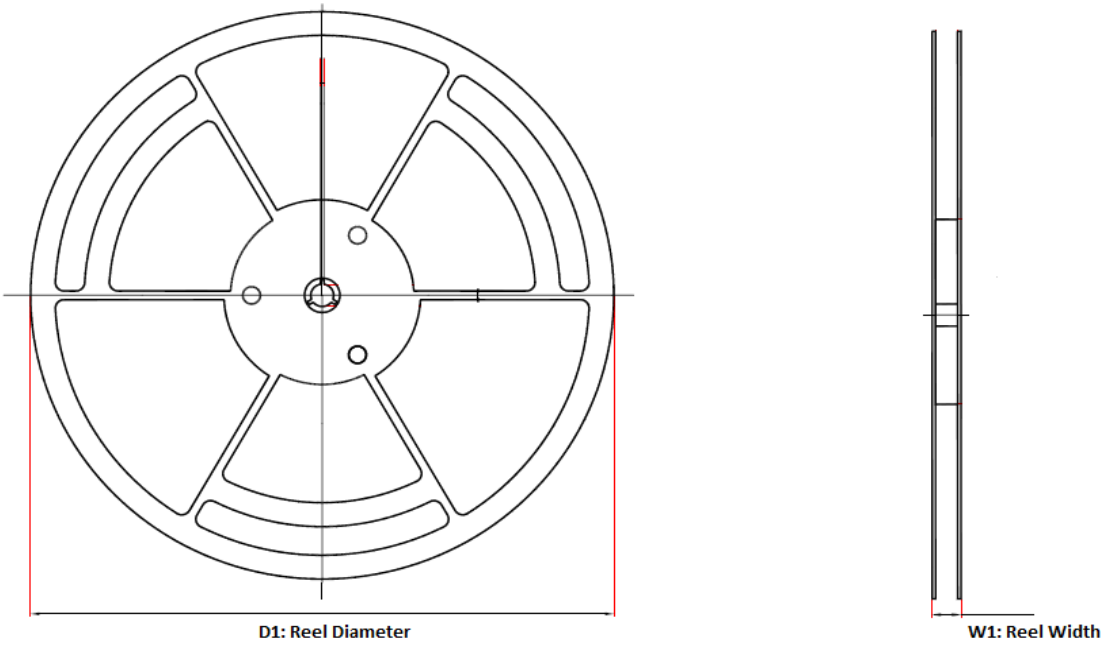
INV = GND

Figure 17 Power Up and Power Down Sequence

Layout

- FLAGx pull-up resistors, recommended 100 kΩ, should be placed closely to the flag output pins and the pull-up power supply. The traces should be equal to each other, and the trace length should be as short as possible.
- Timing delay capacitor should be placed as close as possible to the TSET pin, and straight trace without via is recommended.

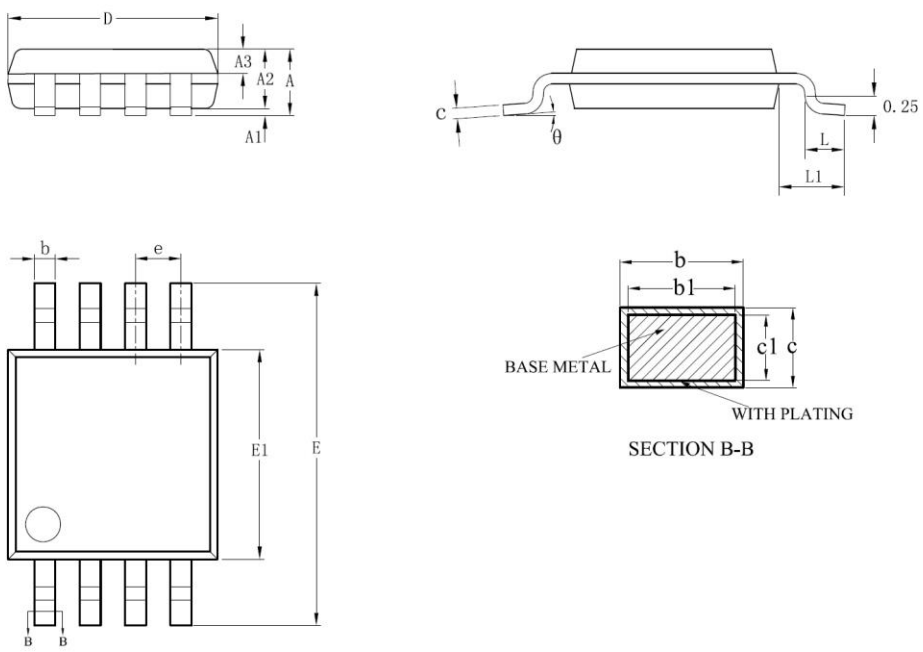
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPK1031L1-VS1R	MSOP8	330	17.6	5.2	3.3	1.5	8	12	Q1

Package Outline Dimensions

MSOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.40	—	0.70
L1	0.95REF		
θ	0	—	8°

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPK1031L1-VS1R	−40 to 125°C	MSOP8	K1031	MSL1	3,000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.