SGM51622S8/SGM51652S8 8-Channel, 16-Bit, Bipolar Input Simultaneous Sampling ADC

GENERAL DESCRIPTION

The SGM51622S8 and SGM51652S8 are 16-bit, 8-channel simultaneous sampling, high-precision successive approximation (SAR) analog-to-digital converters (ADCs).

These ADCs are powered by a single unipolar 5V, and support true bipolar ±10V and ±5V inputs. The input range is configured by hardware pin.

These chips provide over-voltage protection up to ±20V at the input.

These chips have an on-chip high accuracy and low drift 10ppm reference.

The input impedance of these chips is ~1MΩ and it is independent of input range selection.

These ADCs support both high-speed serial and parallel interfaces.

The SGM51622S8 and SGM51652S8 are available in a Green LQFP-10×10-64L package. They are all specified from -40℃ to +125℃.

FEATURES

- **8 Channels Simultaneous Sampling**
  - **SGM51652S8 Supports 500kSPS on All Channels Simultaneously**
  - **SGM51622S8 Supports 250kSPS on All Channels Simultaneously**
- **True Bipolar Analog Input Ranges: ±10V, ±5V**
- **Single 5V Analog Supply and 2.7V to 5V V_{DRIVE}**
- **Input Buffer with 1MΩ Analog Input Impedance**
- **On-Chip Accurate Reference and Reference Buffer**
- **Configurable Oversampling Capability with Digital Filter**
- **Flexible Parallel Interface or Serial Interface**
  - **SPI-Compatible**
- **Performance**
  - **SNR: 91.2dB (TYP), THD: -106dB (TYP)**
  - **INL: ±1.5LSB (TYP), DNL: +1LSB/-0.65LSB (TYP)**
  - **TBDkV ESD Rating on Analog Input Channels**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in a Green LQFP-10×10-64L Package**

APPLICATIONS

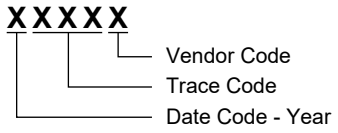
Power-Line Monitoring and Protection Systems
Instrumentation and Control Systems
Multi-Axis Sensor Systems

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM51622S8	LQFP-10×10-64L	-40℃ to +125℃	SGM51622S8XLFH64G/TR	SGM51622S8 XLFH64 XXXXX	Tape and Reel, 1500
SGM51652S8	LQFP-10×10-64L	-40℃ to +125℃	SGM51652S8XLFH64G/TR	SGM51652S8 XLFH64 XXXXX	Tape and Reel, 1500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AV_{CC} to AGND ..... -0.3V to 6V
V_{DRIVE} to AGND ..... -0.3V to AV_{CC} + 0.3V
Analog Input Voltage to AGND (1) ..... ±20V
Digital Input Voltage to AGND ..... -0.3V to V_{DRIVE} + 0.3V
Digital Output Voltage to AGND ..... -0.3V to V_{DRIVE} + 0.3V
REFIN to AGND ..... -0.3V to AV_{CC} + 0.3V
Input Current to Any Pin except Supplies (1) ..... ±10mA
Package Thermal Resistance
LQFP-10×10-64L, θ_{JA} ..... TBD℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

NOTE:
1. Transient currents of up to 100mA do not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

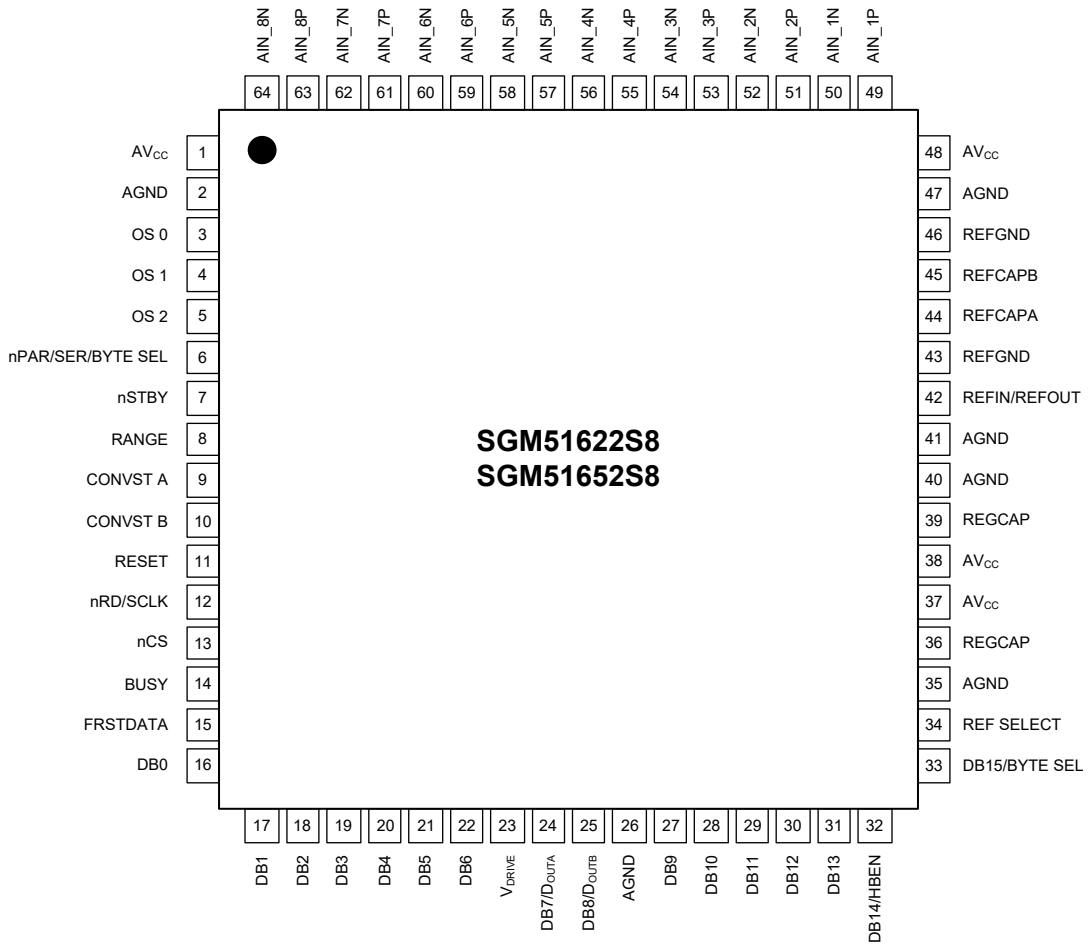
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM51622S8/SGM51652S8 (TOP VIEW)



LQFP-10×10-64L

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1, 37, 38, 48	AV_{CC}	P	Analog Power Supply Pin. It is the power supply of analog front end and ADC core circuit. It is the reference to AGND pin.
2, 26, 35, 40, 41, 47	AGND	P	Analog Ground Pin. All AGND pins must share the same system connection plane.
3	OS 0	DI	Oversampling Mode Setting Pins. They are logic input control pins. More details please refer to Table 4.
4	OS 1		
5	OS 2		
6	nPAR/SER/ BYTE SEL	DI	Parallel/Serial/Byte Interface Setting Pin. It is a logic input. If it is set to logic low, the parallel interface is enabled. If it is set to logic high, the serial interface is enabled. To select byte parallel interface, set the pin to logic high and DB15/BYTE SEL pin to logic high at the same time for a combined enable controlling (refer to Table 3). If the chip works in serial mode, the nRD/SCLK pin is the serial interface clock input pin. The DB7/D_{OUTA} pin and DB8/D_{OUTB} pin are combined together as two lane serial interface data output pins. The DB[15:9] and DB[6:0] pins should be connected to GND. If the chip works in byte parallel interface mode, DB14 is used as the HBEN pin. DB[7:0] is read out in two nRD read frame. The data format is high byte first.
7	nSTBY	DI	Standby Mode Setting Input Pin. This pin is a logic input pin. It works with the RANGE pin together to determine which power-down mode the chip is going to enter standby mode or shutdown mode. More details please refer to Table 2.
8	RANGE	DI	Analog Input Range Setting Pin. This pin is a logic input pin. If it is set to logic high, the analog input range ±10V is set for all channels. If it is set to logic low, the analog input range ±5V is set for all channels. Any change on the logic of the input range setting pin is effect immediately. It is strongly not recommended to change the input range during a conversion or a consequences inputs scanning.
9	CONVST A	DI	Conversion Start Input Pin A and Conversion Start Input Pin B. They are logic input pins. When the input logic from low to high, the input tracking and holding circuitry stops sampling and changes to hold, and ADC initiates a conversion. CONVST A and CONVST B can be tied together for all channels sampling simultaneously. When the oversampling function is not enabled, CONVST A and CONVST B can be used to control ADC conversion separately. CONVST A can be used to control channel V1, V2, V3 and V4. CONVST B can be used to control channel V5, V6, V7 and V8.
10	CONVST B		
11	RESET	DI	Reset Input Pin. An input from logic low to logic high, the rising edge of the input signal triggers the reset action, and the high pulse must be hold at least 50ns. Reset input will terminate the ongoing ADC conversion. And the reset input also will set the ADC output registers to all zero.
12	nRD/SCLK	DI	Multi-Function Pin nRD/SCLK. When the chip is in parallel interface mode, the nRD/SCLK is active logic low. When the chip is in serial interface mode, the nRD/SCLK is active logic low. The data on data bus are locked out on the rising edge of SCLK. For more information, see the Conversion Control section.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE (1)	FUNCTION
13	nCS	DI	Chip Select Control Pin. This pin is active logic low. In serial interface mode, the nCS is used as data frame signal, and the MSB of the serial output is shifted out on the falling edge of nCS.
14	BUSY	DO	Busy Indicator Output Pin. If there is a trigger rising edge of CONVST A or CONVST B, this BUSY pin goes to high immediately. It does not go to low until all the channels conversions have been completed. The falling edge of the BUSY pin indicates that the conversion results are read to read (it needs a reasonable time delay t_4). Any data read operation must be finished before the next falling edge of BUSY coming. During the high of BUSY, any ADC trigger signals of CONVST A and CONVST B are ignored.
15	FRSTDATA	DO	Digital Indicator Output Pin. This pin is active high. In parallel interface mode, the falling edge of nRD which is corresponded to read V1 channel sets the FRSTDATA pin high, and the next following edge of nRD sets the FRSTDATA pin low. In serial interface mode, the falling edge of nCS sets the FRSTDATA pin high. In the same read operation frame, the 16th SCLK falling edge sets the FRSTDATA pin low. If nCS is high, the FRSTDATA pin is in three-state.
16, 17, 18, 19, 20, 21, 22	DB0, DB1, DB2, DB3, DB4, DB5, DB6	DO	Parallel Output Data Bits. In serial interface mode, these pins should be connected to AGND.
23	V_{DRIVE}	P	Login Interface Power Supply Pin.
24	DB7/D_{OUTA}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 7 (DB7)/Serial Interface Data Output Pin (D_{OUTA}). In parallel interface mode, this pin works as DB7. In serial interface mode, this pin works as D_{OUTA}.
25	DB8/D_{OUTB}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 8 (DB8)/Serial Interface Data Output Pin (D_{OUTB}). In parallel interface mode, this pin works as DB8. In serial interface mode, this pin works as D_{OUTB}.
27, 28, 29, 30, 31	DB9, DB10, DB11, DB12, DB13	DO	Parallel Output Data Bits. In byte parallel interface mode and serial interface mode (nPAR/SER/BYTE SEL = 1), these pins should be connected to AGND.
32	DB14/HBEN	DO/DI	Multi-Function Pin, Parallel Interface Output Data Bit 14 (DB14)/High Byte Enable (HBEN). In parallel interface mode, this pin works as DB14. In parallel byte interface mode, this pin is used to select if the most significant byte (MSB) or the least significant byte (LSB) of the data is output first. If HBEN is set to high, MSB is first out. If HBEN is set to low, LSB is first out. In serial mode, this pin should be tied to GND.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE (1)	FUNCTION
33	DB15/ BYTE SEL	DO/DI	Multi-Function Pin, Parallel Interface Output Data Bit 15 (DB15)/Parallel Interface Byte Mode Select (BYTE SEL). In parallel interface mode, this pin works as DB15. If nPAR/SER/BYTE SEL is set to high and DB15/BYTE SEL is set to low, the chip works in serial interface mode. If nPAR/SER/BYTE SEL is set to high and DB15/BYTE SEL is set to high, the chip works in parallel byte interface mode.
34	REF SELECT	DI	Internal/External Reference Selection Pin. This is a logic input pin. If it is set to logic high, the internal reference is enabled. If it is set to logic low, an external reference must be connected to the chip.
36, 39	REGCAP	P	Internal Regulator Decoupling Pins. Each pin needs a separate 1μF decoupling capacitor connected to AGND.
42	REFIN/REFOUT	REF	Reference Input Pin (REFIN)/Reference Output Pin (REFOUT). A 10μF decoupling capacitor needs to be connected between this pin and REFGND.
43, 46	REFGND	REF	Reference Ground Pins. These pins should be connected to AGND.
44, 45	REFCAPA, REFCAPB	REF	Reference Buffer Output Sense Pins. These pins must be tied together. A 10μF decoupling capacitor needs to be connected between these pins and AGND.
49	AIN_1P	AI	Channel 1 Positive Analog Input.
50, 52	AIN_1N, AIN_2N	AI	Channel 1 and Channel 2 Negative Analog Inputs.
51	AIN_2P	AI	Channel 2 Positive Analog Input.
53	AIN_3P	AI	Channel 3 Positive Analog Input.
54	AIN_3N	AI	Channel 3 Negative Analog Input.
55	AIN_4P	AI	Channel 4 Positive Analog Input.
56	AIN_4N	AI	Channel 4 Negative Analog Input.
57	AIN_5P	AI	Channel 5 Positive Analog Input.
58	AIN_5N	AI	Channel 5 Negative Analog Input.
59	AIN_6P	AI	Channel 6 Positive Analog Input.
60	AIN_6N	AI	Channel 6 Negative Analog Input.
61	AIN_7P	AI	Channel 7 Positive Analog Input.
62	AIN_7N	AI	Channel 7 Negative Analog Input.
63	AIN_8P	AI	Channel 8 Positive Analog Input.
64	AIN_8N	AI	Channel 8 Negative Analog Input.

NOTE:
1. P = Power Supply, DI = Digital Input, DO = Digital Output, REF = Reference Input/Output, AI = Analog Input.

ELECTRICAL CHARACTERISTICS

(V_{REF} = 2.5V external/internal, AV_{CC} = 4.75V to 5.25V, V_{DRIVE} = 2.7V to 5.25V, f_{SAMPLE} = 250kSPS, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic Performance (f_{IN} = 1kHz sine wave, unless otherwise noted)							
Signal-to-Noise Ratio (1)	SNR	Oversampling by 16, ±10V range, f_{IN} = 130Hz			91.2		dB
		Oversampling by 16, ±5V range, f_{IN} = 130Hz			91		
		No oversampling, ±10V range			89.9		
		No oversampling, ±5V range			89.3		
Signal-to-Noise + Distortion	SINAD	No oversampling, ±10V range			89.8		dB
		No oversampling, ±5V range			89.2		
Dynamic Range		No oversampling, ±10V range			91		dB
		No oversampling, ±5V range			91		
Total Harmonic Distortion	THD				-106		dB
Peak Harmonic or Spurious Noise	SFDR				-109		dB
Intermodulation Distortion	IMD	f_A = 1kHz, f_B = 1.1kHz	Second-order terms		-115		dB
			Third-order terms		-105		
Analog Input Filter							
Full Power Bandwidth	BW	-3dB	±10V range		24		kHz
			±5V range		24		
		-0.1dB	±10V range		4		
			±5V range		4		
DC Accuracy							
Resolution		No missing codes		16			Bits
Differential Nonlinearity	DNL				+1/-0.65		LSB (2)
Integral Nonlinearity	INL				±1.5		LSB
Total Unadjusted Error	TUE	±10V range			±12		LSB
		±5V range			±13		
Positive Full-Scale Error (3)		External reference			±9		LSB
		Internal reference			±9		
Positive Full-Scale Error Drift		External reference			3		ppm/℃
		Internal reference			7		
Positive Full-Scale Error Matching		±10V range			6		LSB
		±5V range			6		
Bipolar Zero-Code Error (4)		±10V range			±2		LSB
		± 5V range			±3		
Bipolar Zero-Code Error Drift		±10V range			8		μV/℃
		± 5V range			20		
Bipolar Zero-Code Error Matching		±10V range			2		LSB
		±5V range			3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{REF} = 2.5V external/internal, AV_{CC} = 4.75V to 5.25V, V_{DRIVE} = 2.7V to 5.25V, f_{SAMPLE} = 250kSPS, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Negative Full-Scale Error (3)		External reference		±9		LSB
		Internal reference		±9		
Negative Full-Scale Error Drift		External reference		3		ppm/℃
		Internal reference		7		
Negative Full-Scale Error Matching		±10V range		6		LSB
		±5V range		6		
Analog Input						
Input Voltage Ranges	V_{IN}	RANGE = 1			±10	V
		RANGE = 0			±5	
Analog Input Current		10V		7.3		μA
		5V		2.8		
Input Capacitance (5)	C_{IN}			5		pF
Input Impedance	R_{IN}	See the Analog Input section		1		MΩ
Input Over-Voltage Protection						
Over-Voltage Protection Voltage	V_{OVP}	AVDD = 5V or offers low impedance < 30kΩ, all input ranges	-20		+20	V
		AVDD = floating with impedance > 30kΩ, all input ranges	-11		+11	V
Reference Input/Output						
Reference Input Voltage Range	V_{REF}	See the ADC Transfer Function section	2.475	2.5	2.525	V
DC Leakage Current				±0.1		μA
Input Capacitance (5)		REF SELECT = 1		6		pF
Reference Output Voltage		REFIN/REFOUT		2.5		V
Reference Temperature Coefficient				±8		ppm/℃
Logic Inputs						
Input High Voltage	V_{IH}		0.8 × V_{DRIVE}			V
Input Low Voltage	V_{IL}				0.2 × V_{DRIVE}	V
Input Current	I_{IN}			±0.1		μA
Input Capacitance (5)	C_{IN}			5		pF
Logic Outputs						
Output High Voltage	V_{OH}	I_{SOURCE} = 100μA	V_{DRIVE} - 0.2			V
Output Low Voltage	V_{OL}	I_{SINK} = 100μA			0.2	V
Floating-State Leakage Current				±0.1		μA
Floating-State Output Capacitance (5)				5		pF
Output Coding		Two's complement				
Conversion Rate						
Conversion Time	t_{CONV}	All eight channels included, see Timing Specifications section		2		μs
Track-and-Hold Acquisition Time	t_{ACQ}			2		μs
Throughput Rate		Per channel, all eight channels included			250	kSPS

ELECTRICAL CHARACTERISTICS (continued)

(V_{REF} = 2.5V external/internal, AV_{CC} = 4.75V to 5.25V, V_{DRIVE} = 2.7V to 5.25V, f_{SAMPLE} = 250kSPS, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Requirements							
Analog Supply Voltage	AV_{CC}			4.75		5.25	V
Digital I/O Supply Voltage	V_{DRIVE}			2.7		AV_{CC}	V
I_{TOTAL}		Digital inputs = 0V or V_{DRIVE}	Normal mode (static)		22.2		mA
			Normal mode (operational) (6), f_{SAMPLE} = 250kSPS		33		mA
			Standby mode		9.2		mA
			Shutdown mode		16		μA
Power Dissipation							
Power Dissipation	P_D	Normal mode (static)			111		mW
		Normal mode (operational) (6), f_{SAMPLE} = 250kSPS			165		mW
		Standby mode			46		mW
		Shutdown mode			90		μW

NOTES:

1. This specification applies when reading during a conversion or after a conversion. If reading during a conversion in parallel mode with V_{DRIVE} = 5V, SNR typically reduces by 1.5dB and THD by 3dB.
2. LSB = Least Significant Bit. 1LSB = 152.58μV in the ±5V input range. 1LSB = 305.175μV in the ±10V input range.
3. These specifications include the full temperature range variation and contribution from the internal reference buffer, but exclude the error contribution from the external reference.
4. Bipolar zero-code error is calculated with respect to the analog input voltage. Refer to the Analog Input Clamp Protection section.
5. Test samples at initial release to ensure compliance.
6. Operational power/current figure includes contribution when running in oversampling mode.

TIMING SPECIFICATIONS

(AV_{CC} = 4.75V to 5.25V, V_{DRIVE} = 2.7V to 5.25V, V_{REF} = 2.5V external reference/internal reference, Full = -40℃ to +125℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Parallel/Serial/Byte Mode						
1/Throughput Rate	t_4/t_{CYCLE}	Parallel mode, reading during or after conversion, or serial mode: V_{DRIVE} = 3.3V to 5.25V, reading during a conversion using D_{OUTA} and D_{OUTB} lines			4	μs
		Serial mode reading after a conversion, V_{DRIVE} = 2.7V		7.3		
Conversion Time	t_{CONV}	Oversampling off		2		μs
		Oversampling by 2		5.8		
		Oversampling by 4		13.4		
		Oversampling by 8		28.6		
		Oversampling by 16		59		
		Oversampling by 32		120		
		Oversampling by 64		242		
nSTBY Rising Edge to CONVST x Rising Edge, Power-Up Time from Standby Mode	$t_{WAKE-UP\ STANDBY}$			360		μs
nSTBY Rising Edge to CONVST x Rising Edge, Power-Up Time from Shutdown Mode	$t_{WAKE-UP\ SHUTDOWN}$	Internal reference		17		ms
		External reference		17		
RESET High Pulse Width	t_1		50			ns
BUSY to OS x Pin Setup Time	t_{OS_SETUP}		50			ns
BUSY to OS x Pin Hold Time	t_{OS_HOLD}		25			ns
CONVST x High to BUSY High	t_6				40	ns
Minimum CONVST x Low Pulse	t_3		25			ns
Minimum CONVST x high pulse	t_5		25			ns
BUSY Falling Edge to nCS Falling Edge Setup Time	t_7		0			ns
Maximum Delay Allowed between CONVST A and CONVST B Rising Edges (2)	t_{30}				0.5	ms
Maximum Time between Last nCS Rising Edge and BUSY Falling Edge	t_8				25	ns
Minimum Delay between RESET Low to CONVST x Low	t_2		25			ns
Parallel/Byte Read Operation						
nCS to nRD Setup Time	t_9		0			ns
nCS to nRD Hold Time	t_{12}		0			ns
nRD Low Pulse Width	t_{10}	V_{DRIVE} above 4.75V	18			ns
		V_{DRIVE} above 3.3V	20			
		V_{DRIVE} above 2.7V	20			

TIMING SPECIFICATIONS (continued)

(AV_{CC} = 4.75V to 5.25V, V_{DRIVE} = 2.7V to 5.25V, V_{REF} = 2.5V external reference/internal reference, Full = -40℃ to +125℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
nRD High Pulse Width	t_{11}		16			ns
nCS High Pulse Width, nCS and nRD Linked	t_{29}	See Figure 4	20			ns
Delay from nCS until DB[15:0] Three-State Disabled	t_{13}	V_{DRIVE} above 4.75V			16	ns
		V_{DRIVE} above 3.3V			20	
		V_{DRIVE} above 2.7V			25	
Data Access Time after nRD Falling Edge (3)	t_{14}	V_{DRIVE} above 4.75V			16	ns
		V_{DRIVE} above 3.3V			20	
		V_{DRIVE} above 2.7V			25	
Data Hold Time after nRD Falling Edge	t_{31}		6			ns
nCS to DB[15:0] Hold Time	t_{32}		12			ns
Delay from nCS Rising Edge to DB[15:0] Three-State Enabled	t_{33}				25	ns
Serial Read Operation						
Frequency of Serial Read Clock	f_{SCLK}	V_{DRIVE} above 4.75V			25	MHz
		V_{DRIVE} above 3.3V			22	
		V_{DRIVE} above 2.7V			20	
Delay from nCS until D_{OUTA}/D_{OUTB} Three-State Disabled/Delay from nCS until MSB Valid	t_{22}	V_{DRIVE} above 4.75V			16	ns
		V_{DRIVE} above 3.3V			18	
		V_{DRIVE} above 2.7V			20	
Data Access Time after SCLK Rising Edge (3)	t_{23}	V_{DRIVE} above 4.75V			16	ns
		V_{DRIVE} above 3.3V			18	
		V_{DRIVE} above 2.7V			20	
SCLK Low Pulse Width	t_{21}		0.4 × t_{SCLK}			ns
SCLK High Pulse Width	t_{20}		0.4 × t_{SCLK}			ns
SCLK Rising Edge to D_{OUTA}/D_{OUTB} Valid Hold Time	t_{24}		6			ns
nCS Rising Edge to D_{OUTA}/D_{OUTB} Three-State Enabled	t_{25}				25	ns

TIMING SPECIFICATIONS (continued)

(AV_{CC} = 4.75V to 5.25V, V_{DRIVE} = 2.7V to 5.25V, V_{REF} = 2.5V external reference/internal reference, Full = -40℃ to +125℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FRSTDATA Operation						
Delay from nCS Falling Edge until FRSTDATA Three-State Disabled	t_{16}	V_{DRIVE} above 4.75V			15	ns
		V_{DRIVE} above 3.3V			20	
		V_{DRIVE} above 2.7V			25	
Delay from nCS Falling Edge until FRSTDATA High, Serial Mode	t_{26}	V_{DRIVE} above 4.75V			15	ns
		V_{DRIVE} above 3.3V			20	
		V_{DRIVE} above 2.7V			25	
Delay from nRD Falling Edge to FRSTDATA High	t_{17}	V_{DRIVE} above 4.75V			15	ns
		V_{DRIVE} above 3.3V			20	
		V_{DRIVE} above 2.7V			25	
Delay from nRD Falling Edge to FRSTDATA Low	t_{18}	V_{DRIVE} = 3.3V to 5.25V			15	ns
		V_{DRIVE} = 2.7V to 3.3V			18	
Delay from 16th SCLK Falling Edge to FRSTDATA Low	t_{27}	V_{DRIVE} = 3.3V to 5.25V			15	ns
		V_{DRIVE} = 2.7V to 3.3V			18	
Delay from nCS Rising Edge until FRSTDATA Three-State Enabled	t_{19}				22	ns

NOTES:

1. Sample tested during initial release to ensure compliance. All input signals are specified with t_R = t_F = 5ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6V.
2. The delay between the CONVST x signals was measured as the maximum time allowed while ensuring a < 10LSB performance matching between channel sets.
3. A buffer is used on the data output pins for these measurements, which is equivalent to a 20pF load on the output pins.

TIMING DIAGRAMS

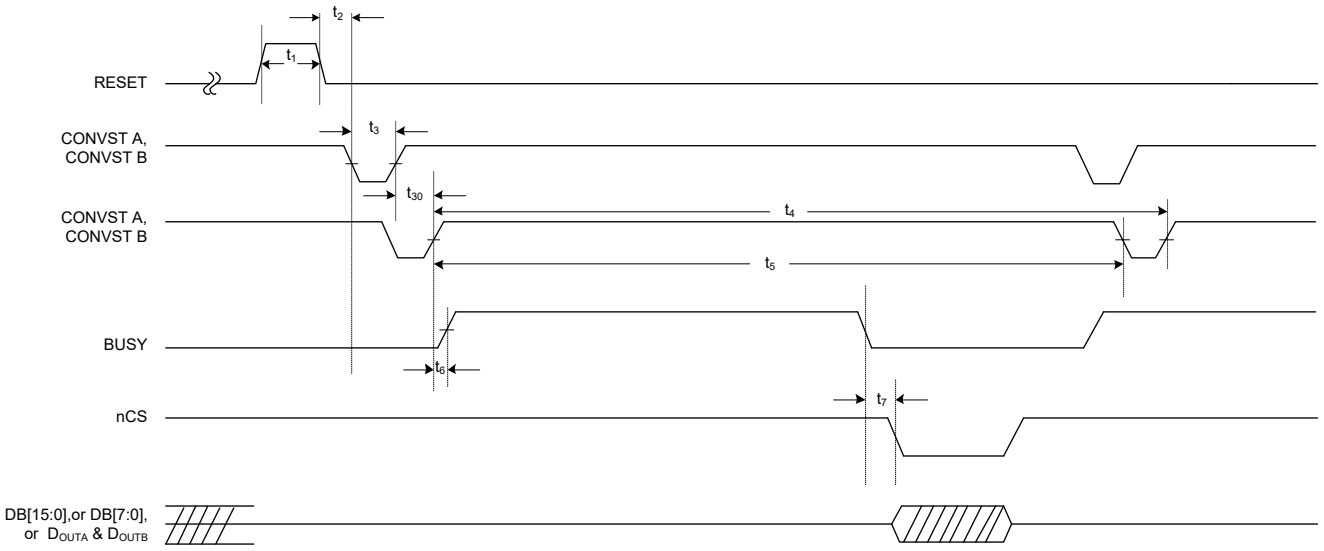


Figure 1. CONVST Timing (Reading after a Conversion)

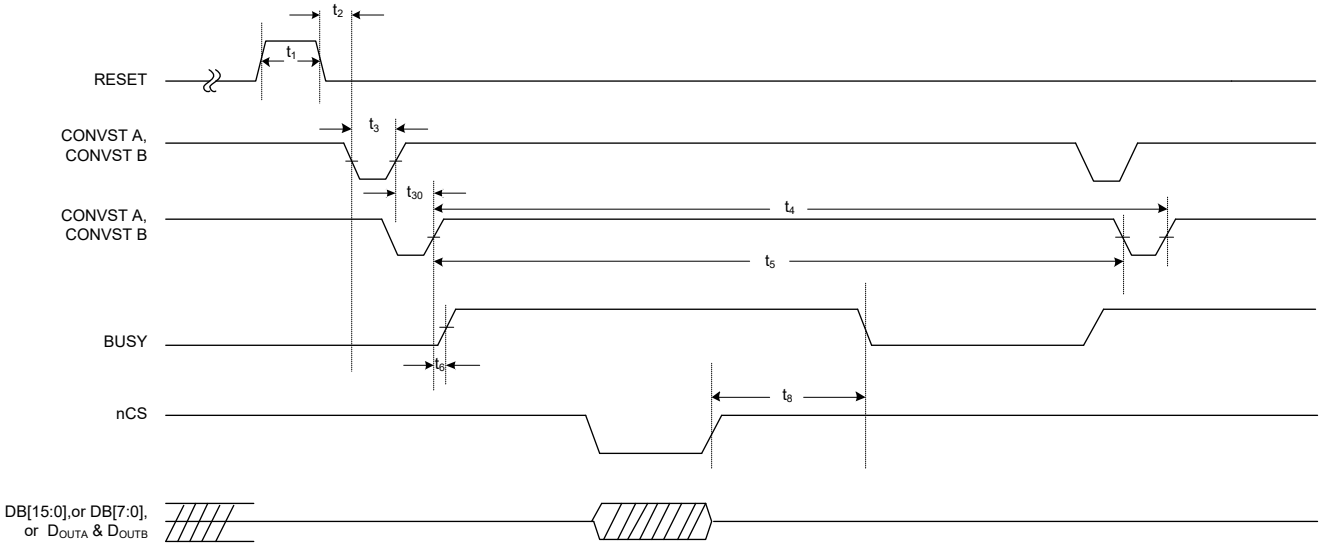


Figure 2. CONVST Timing (Reading during a Conversion)

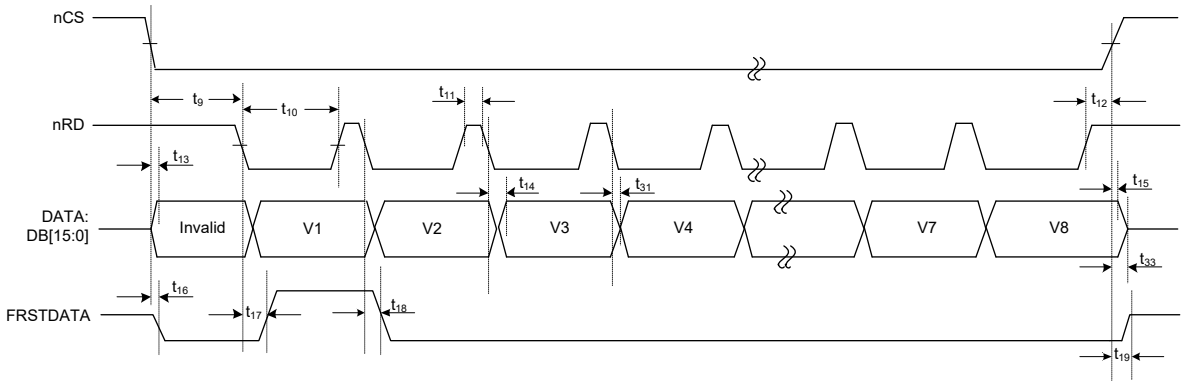


Figure 3. Parallel Mode, Separate nCS and nRD Pulses

TIMING DIAGRAMS (continued)

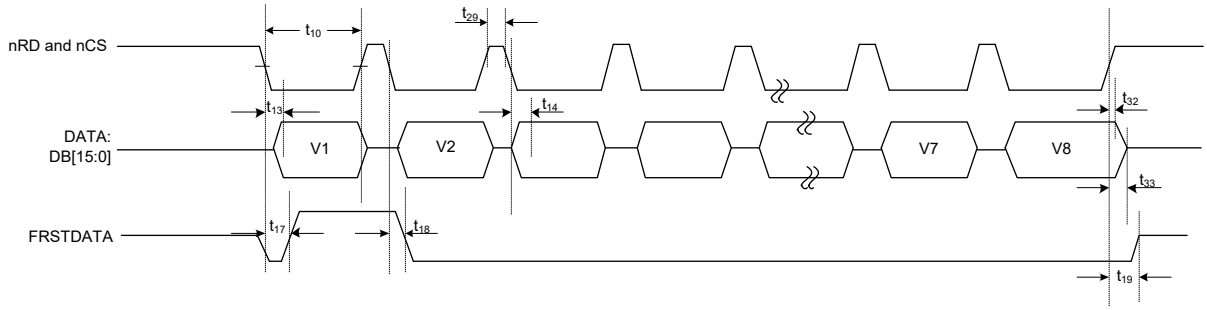


Figure 4. nCS and nRD, Linked Parallel Mode

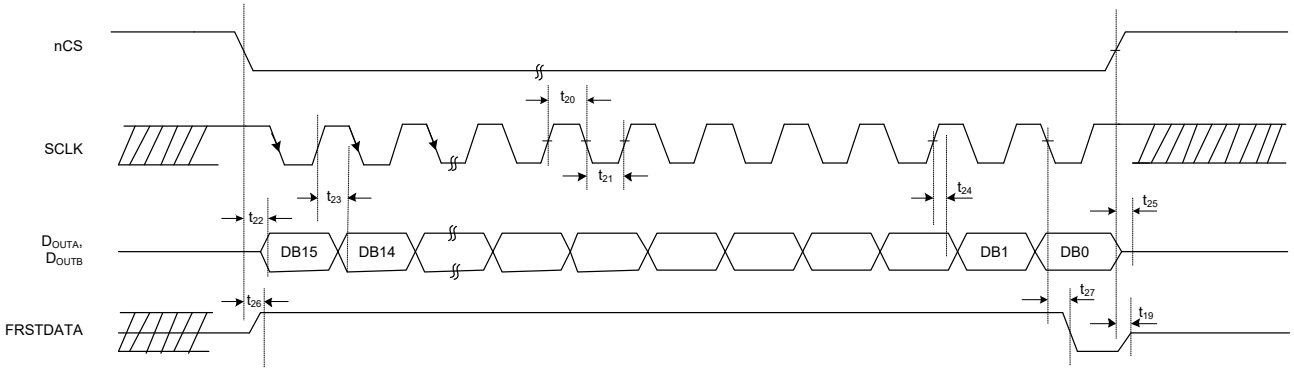


Figure 5. Serial Read Operation (Channel 1)

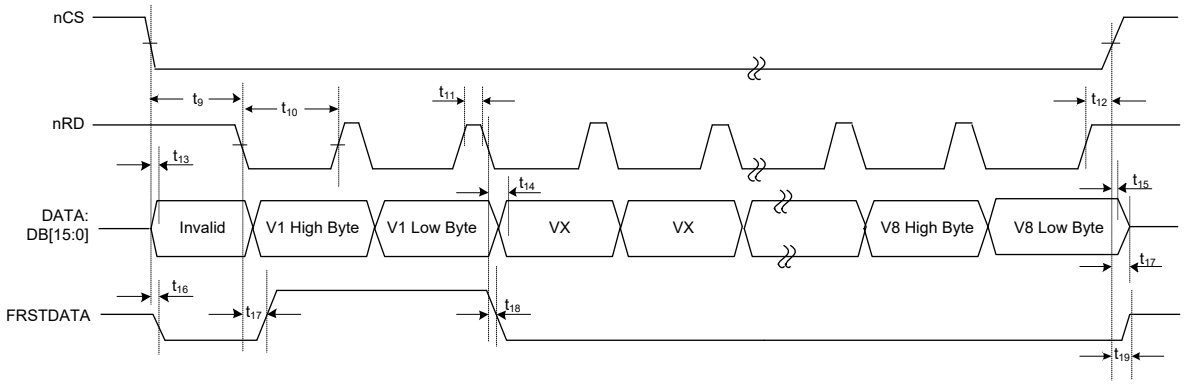


Figure 6. BYTE Mode Read Operation

FUNCTIONAL BLOCK DIAGRAM

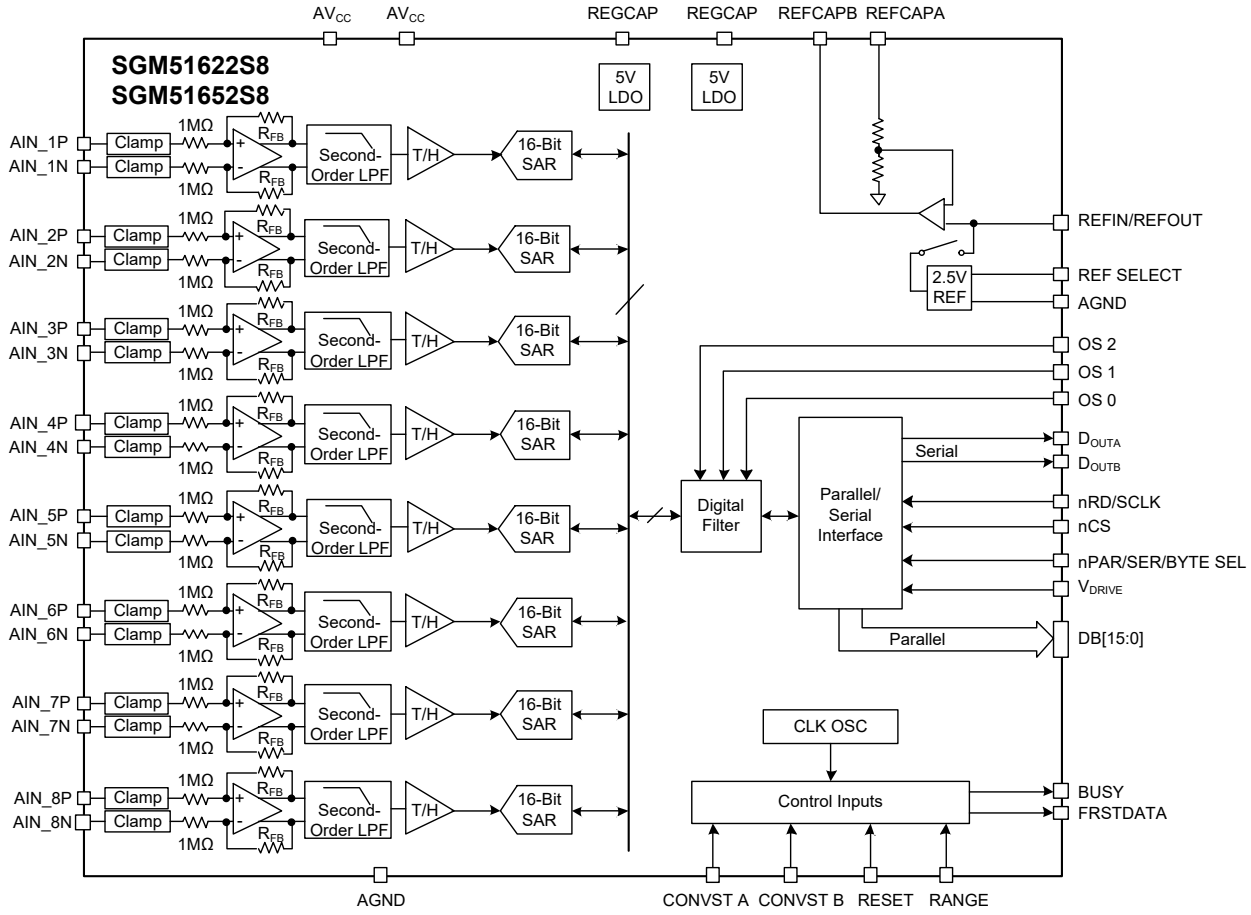


Figure 7. Block Diagram

DETAILED DESCRIPTION

Converter Details

The SGM51622S8 is a unipolar 5V supply SAR ADC. It supports true bipolar signal input. The device can perform all eight channels simultaneously sampling at speed of 250kHz.

The SGM51652S8 is a unipolar 5V supply SAR ADC. It supports true bipolar signal input. The device can perform all eight channels simultaneously sampling at speed of 500kHz.

Analog Input

Analog Input Ranges

The ADCs input range is selected by setting the logic voltage of the RANGE pin. If the pin is set to logic high, the ±10V input range is selected for all channels. If the pin is set to logic low, the ±5V input range is selected for all channels.

It is suggested that the input range pin should be set by hardware pull-up or pull-down. After the system is powered up, a reset pulse must be issued to ensure that the input range is correctly set for all channels.

When in a power-down mode, it is recommended to tie the analog inputs to GND.

Analog Input Impedance

The input impedance of each channel is ≥ 1MΩ.

Analog Input Clamp Protection

The chip has the input over-voltage protection (OVP) circuit. Table 1 shows these characteristics.

Table 1. Input Over-Voltage Protection Limits when AVDD = 5V (1)

Input Condition (V_{OVP} = ±20V)	ADC Output	Comments
$\|V_{IN}\| < \|V_{RANGE}\|$	Valid	Work normally.
$\|V_{RANGE}\| < \|V_{IN}\| < \|V_{OVP}\|$	Saturated	ADC output is saturated, and the internal protection circuits are on.
$\|V_{IN}\| > \|V_{OVP}\|$	Saturated	This may damage the chip.

NOTE: 1. AGND = 0V, $|V_{RANGE}|$ is the maximum input voltage for any selected input range, and $|V_{OVP}|$ is the break-down voltage for the internal OVP circuit. Assume that R_S is approximately 0Ω.

In the following condition, the input signal is applied before analog AVDD is powered on or the input signal is applied and keep analog AVDD floating, the input OVP circuits will be on. And if the input voltage exceeds $|V_{OVP}|$, the chip will be damaged.

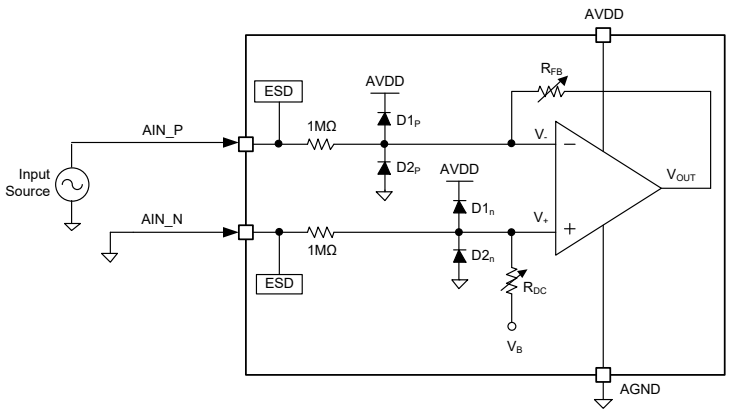


Figure 8. Analog Input Equal Circuitry

DETAILED DESCRIPTION (continued)

Analog Input Antialiasing Filter

The SGM51622S8 and SGM51652S8 have an internal second-order low pass filter in front of ADC core. If ±5V input range is selected, the -3dB bandwidth is about 24kHz. If ±10V input range is selected, the -3dB bandwidth is about 24kHz.

Figure 9. Analog Antialiasing Filter Frequency Response

Figure 10. Analog Antialias Filter Phase Response

Track-and-Hold Amplifiers

This section briefly introduces how the device works and interfaces with the host controller.

Figure 11 shows the timing marks, there are three events T1 ~ T3.

T1: On the rising edge of CONVST x, the input signals are simultaneously sampled by the device.

T2: The device starts converting of all the input signals, the conversion is driven by internal clock.

T3: After all conversions completed, the BUSY goes to low. On the following edge of BUSY, the device goes to tracking mode.

T4: On a new rising edge of CONVST x, a new conversion cycle is started.

DETAILED DESCRIPTION (continued)

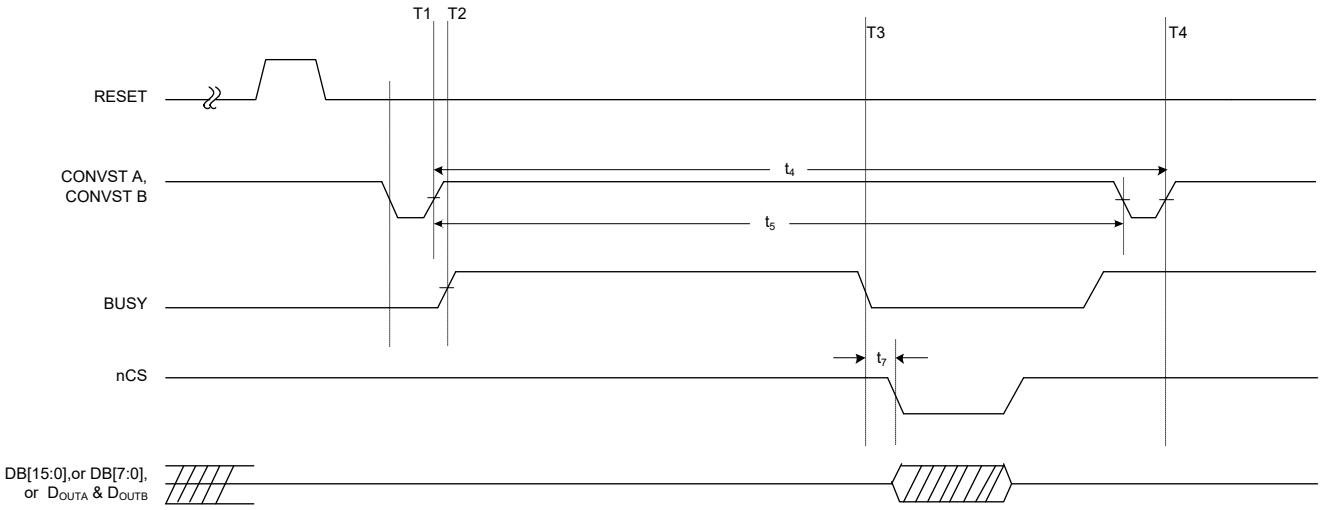
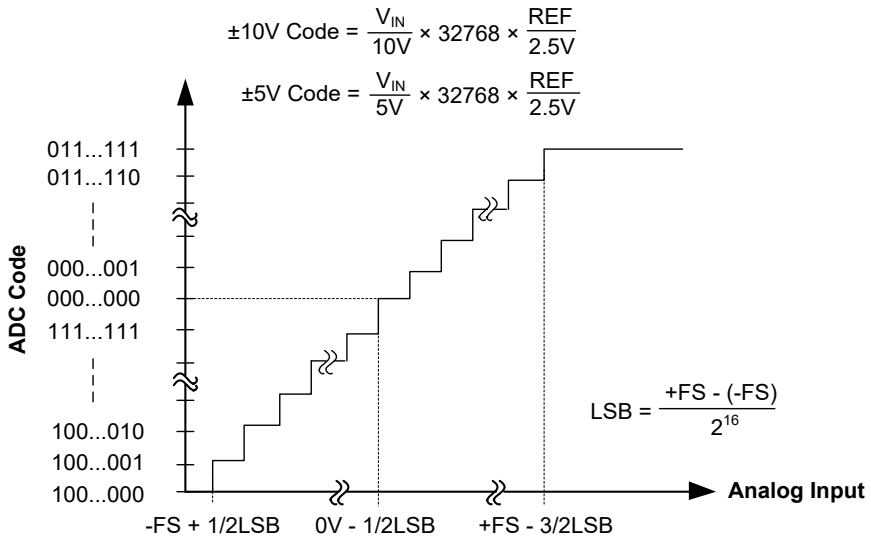


Figure 11. Timing Diagram of Device Operation

ADC Transfer Function

The chip output code is in twos complement format.

The ideal transfer function of SGM51622S8/SGM51652S8 is shown in Figure 12.



	+FS	Midscale	-FS	LSB
±10V Range	±10V	0V	-10V	305μV
±5V Range	±5V	0V	-5V	152μV

NOTE: The LSB size is dependent on the analog input range selected.

Figure 12. SGM51622S8/SGM51652S8 Transfer Characteristics

DETAILED DESCRIPTION (continued)

Internal/External Reference

The SGM51622S8 and SGM51652S8 have an internal 2.5V on-chip reference. They can work with internal reference or external reference. To use internal reference or external reference is decided by REF SELECT pin. When this pin is set to logic high, the internal reference is enabled. When this pin is set to logic low, the internal reference is disabled and an external 2.5V reference must be applied.

After a reset, the chip refreshes the reference selection status. It is decided by the REF SELECT pin setting.

For both the internal reference and the external reference, the chip needs decoupling caps on the REFIN/REFOUT pin. At the same time, the REFCAPA and REFCAPB must be tied together. And a typical decoupling 10μF capacitor must be applied between this pin and REFGND pin.

External Reference Mode

An external reference chip SGM4029-2.5 is used to drive three pcs of ADCs. A demo circuit connection is shown in Figure 13.

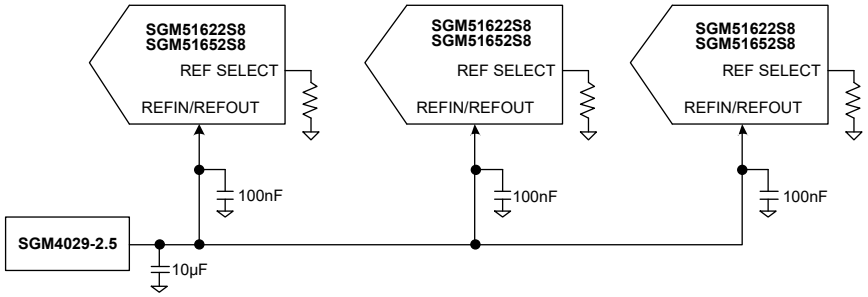


Figure 13. Single External Reference Driving Multiple SGM51622S8/SGM51652S8 REFIN Pins

Internal Reference Mode

In a multi-chip system, one SGM51622S8 or SGM51652S8 on-chip reference can be configured as output, the other chip can be configured as external reference input mode. A demo circuit connection is shown in Figure 14.

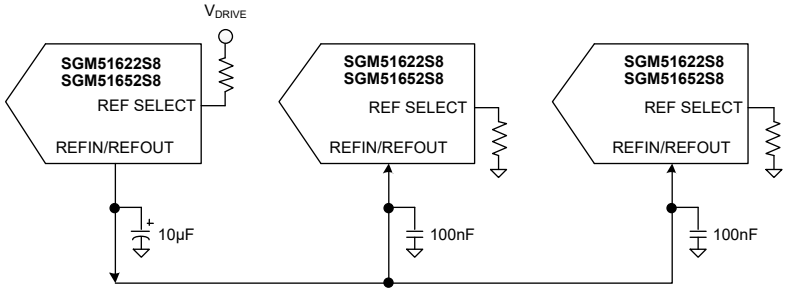


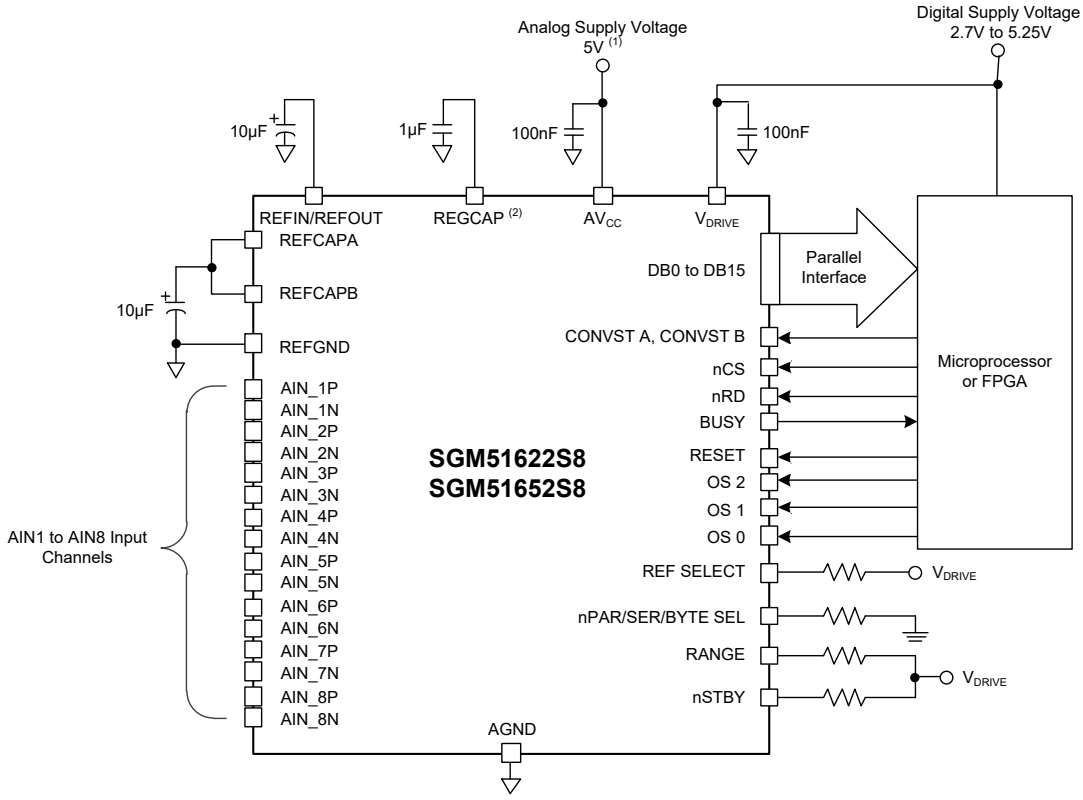
Figure 14. Internal Reference Driving Multiple SGM51622S8/SGM51652S8 REFIN Pins

DETAILED DESCRIPTION (continued)

Typical Connection Diagram

A typical connection circuit is shown in Figure 15. Note that all power supply pins and reference pins should be decoupled by the decoupling capacitors.

After the system is powered up, a reset should be issued to the chip to ensure all hardware setting is configured correctly.



NOTES:
1. At least one decoupling capacitor should be applied to each AV_{CC} pin (pin 1, pin 37, pin 38, pin 48).
2. At least one decoupling capacitor should be applied to each REGCAP pin (pin 36, pin 39).

Figure 15. Typical Connection Diagram

Power-Down Modes

The SGM51622S8 and SGM51652S8 support two low power modes, standby mode and shutdown mode. Table 2 shows how to configure the chip into according mode.

In standby mode, the chip only powers down the input buffer amplifier and ADC core. The current consumption is about 9.2mA. To quit the standby mode, the wake-up time is about 360μs.

In shutdown mode, the chip powers down all the internal circuits. The current consumption is about 16μA. To quit the shutdown mode, a RESET signal must be applied. The wake-up time is about 17ms.

Table 2. Power-Down Mode Selection

Power-Down Mode	nSTBY	RANGE
Standby	0	1
Shutdown	0	0

DETAILED DESCRIPTION (continued)

Conversion Control

Simultaneous Sampling on All Analog Input Channels

To sample and convert all 8 input channels simultaneously, CONVST A and CONVST B can be tied together.

Simultaneously Sampling Two Sets of Channels

CONVST A controls the sampling and conversion of V1 to V4 channel. CONVST B controls the sampling and conversion of V5 to V8 channel.

In a conversion process cycle, after both CONVST A and CONVST B rising edges have been issued, then BUSY goes high indicates that ADC is doing conversion. The data read out is no different with the operating of CONVST A and CONVST B tied together.

Note that all un-used input channels should be tied to system ground (AGND).

Digital Interface

The SGM51622S8 and SGM51652S8 have three operating interface modes: parallel interface mode, serial interface mode and parallel byte interface mode.

Table 3. Interface Mode Selection

nPAR/SER/BYTE SEL	DB15	Interface Mode
0	0	Parallel interface mode
1	0	Serial interface mode
1	1	Parallel byte interface mode

Serial Interface (nPAR/SER/BYTE SEL = 1)

In serial interface mode, there are two options: two serial data output pins mode (D_{OUTA} and D_{OUTB} output data simultaneously) and one serial data output pin mode (D_{OUTA} or D_{OUTB}, D_{OUTA} is preferred).

In two serial data output pins mode, channel V1 to V4 data are shifted by D_{OUTA}, channel V5 to V8 data are shifted by D_{OUTB}. The falling edge of the nCS calls D_{OUTA} and D_{OUTB} outing of the three-state and shifts out the MSB of the ADC result. The ADC data is shifted out at the rising edge of SCLK.

In one serial data output pin mode, D_{OUTA} or D_{OUTB} can be used as data output pin. If D_{OUTA} is selected, the ADC results sequence is V1 to V8. If D_{OUTB} is selected, the ADC results sequence is V5 to V8 and then V1 to V4.

In serial operation mode, Figure 5 shows a demo operating timing diagram of reading one channel ADC data and framed by nCS.

Digital Filter

The SGM51622S8 and SGM51652S8 have an internal configurable low pass digital filter. The oversampling rate is set by OS 2, OS 1 and OS 0 pins. OS 2 sets the MSB bit, OS 1 sets the middle weighting bit, and OS 0 sets the LSB bit. Table 4 shows the different available oversampling rates.

Once the OS x (OS 2, OS 1 and OS 0) pins setting are changed, the new setting will be latched on the falling edge of BUSY. And the new setting will take effect on the next conversion cycle. A demo time sequence is shown in Figure 16.

In the oversampling modes, CONVST A and CONVST B must be tied together to let ADC work correctly. The CONVST x (CONVST A and CONVST B) triggers the first conversion of each input channels in one conversion frame, the left conversions according to oversampling rates will be triggered internally by ADC. For example, if oversampling rate is set to 4, CONVST x triggers the first conversion and the left 3 times of conversions are triggered internally by ADC in one frame.

DETAILED DESCRIPTION (continued)

Refer to Table 4, the oversample rate is increased, and the SNR is increased. While the useful equal -3dB frequency bandwidth is decreased accordingly.

In Figure 16, for example, if the oversample rate is increased by 2, the conversion time is increased by 2. To let the host controller has adequate time to read out the ADC conversion results, the total conversion cycle needs to be extended accordingly.

Note that the falling edge of BUSY is used to update ADC output data register by the ADC chip internally in Figure 16. The host controller cannot use the falling edge of BUSY to trigger a read operation, in other words, the reading of ADC conversion data must not be started at this falling edge.

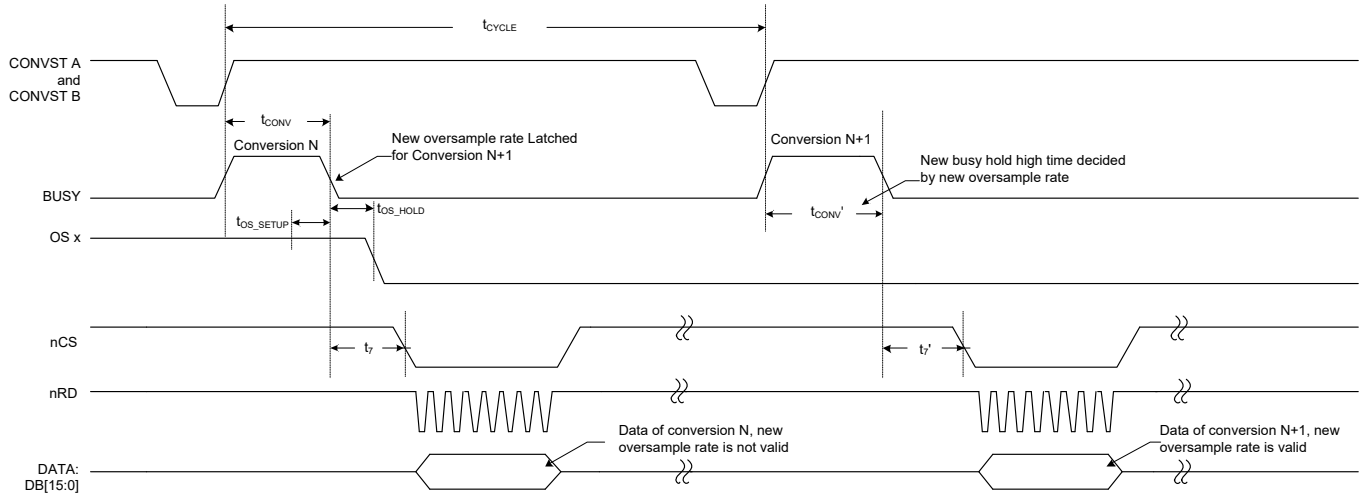


Figure 16. OS x Pin Timing

Table 4. Oversample Bit Decoding

OS[2:0]	OS Ratio	SNR 5V Range (dB)	SNR 10V Range (dB)	3dB BW 5V Range (kHz)	3dB BW 10V Range (kHz)	Maximum Throughput CONVST Frequency (kHz)
000	No OS					
001	2					
010	4					
011	8					
100	16					
101	32					
110	64					
111	Invalid					

DETAILED DESCRIPTION (continued)

The effect of oversampling on the code spread in a DC histogram plot is shown in Figure 17 to Figure 23. With the increase of the oversample rate, the spread of the codes decreases.

Figure 17. Histogram of Codes—No OS (Six Codes)

Figure 18. Histogram of Codes—OS × 2 (Four Codes)

Figure 19. Histogram of Codes—OS × 4 (Four Codes)

Figure 20. Histogram of Codes—OS × 8 (Three Codes)

Figure 21. Histogram of Codes—OS × 16 (Two Codes)

Figure 22. Histogram of Codes—OS × 32 (Two Codes)

DETAILED DESCRIPTION (continued)

Figure 23. Histogram of Codes—OS × 64 (Two Codes)

The digital filter frequency profiles for the different oversampling rates are shown in Figure 24 to Figure 29.

Figure 24. Digital Filter Response for OS 2

Figure 25. Digital Filter Response for OS 4

Figure 26. Digital Filter Response for OS 8

Figure 27. Digital Filter Response for OS 16

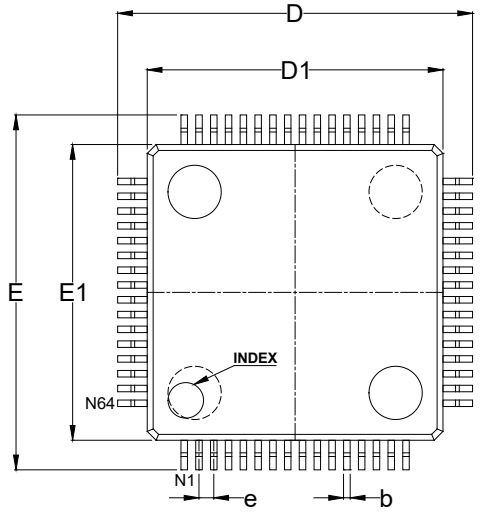
DETAILED DESCRIPTION (continued)

Figure 28. Digital Filter Response for OS 32

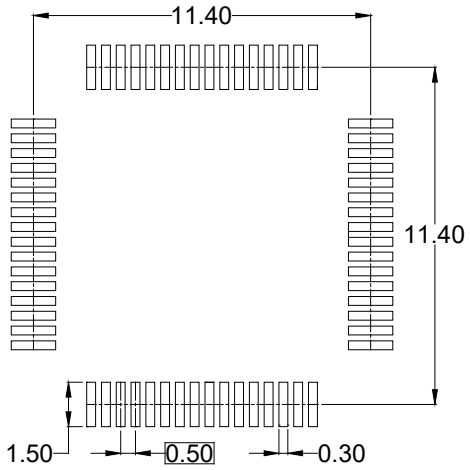
Figure 29. Digital Filter Response for OS 64

PACKAGE OUTLINE DIMENSIONS

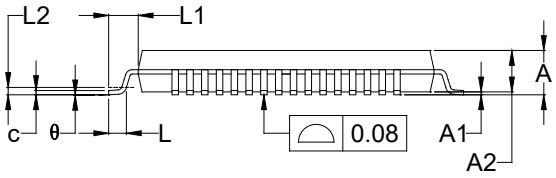
LQFP-10×10-64L



TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



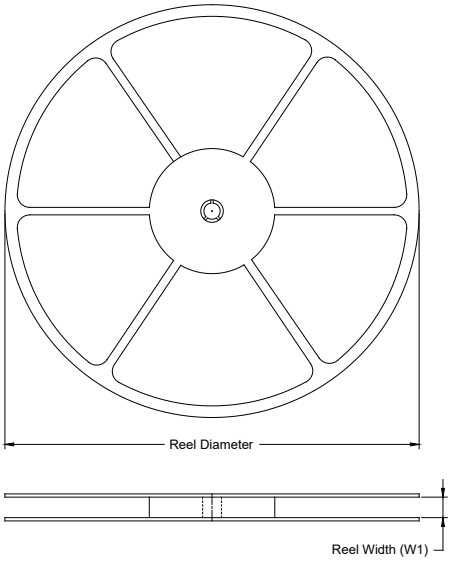
SIDE VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.170	-	0.270
c	0.090	-	0.200
D	11.800	-	12.200
D1	9.900	-	10.100
E	11.800	-	12.200
E1	9.900	-	10.100
e	0.500 BSC		
L	0.450	-	0.750
L1	1.000 REF		
L2	0.250 BSC		
θ	0°	-	7°

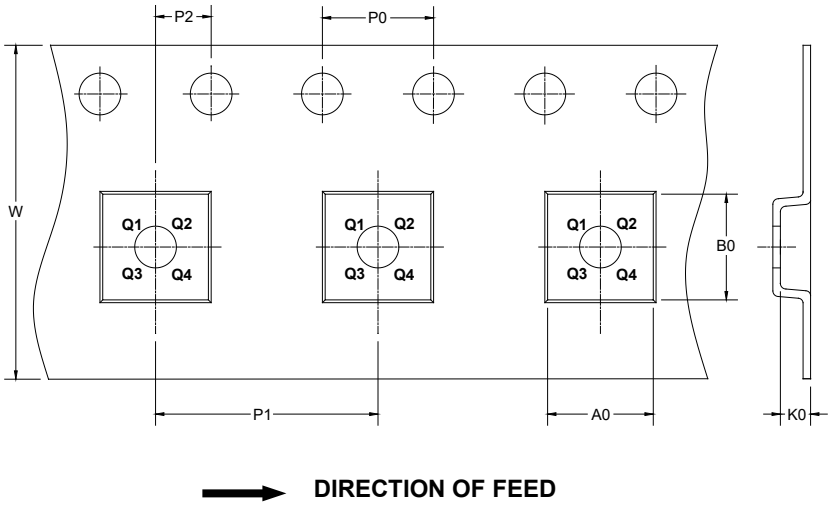
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-026.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



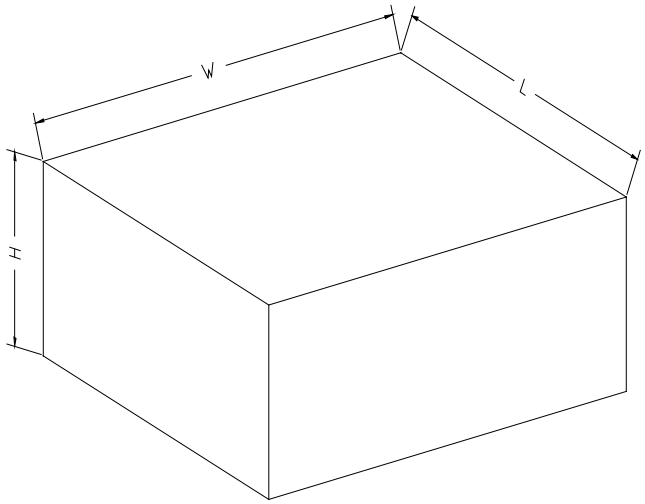
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
LQFP-10×10-64L	13″	24.4	12.5	12.5	2.05	4.0	16.0	2.0	24.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002