SGM61280
8A, 23V, Synchronous Buck Converters with 3.3V/5V LDO

GENERAL DESCRIPTION

The SGM61280 family is a high efficiency and miniature size synchronous Buck converter for wide input voltage applications.

The SGM61280 family, 8A synchronous Buck converter with integrated low R_{DSON} MOSFET switches, provides both SGM61280-3.3 and SGM61280-5.1 efficient fixed output voltage versions. The device uses constant on-time (COT) control for fast transient response and supports input voltage range from 4.5V to 23V for the SGM61280-3.3, and 5.1V to 23V for the SGM61280-5.1.

The SGM61280 is available in a space-saving Green UTQFN-3×3-12AL package. It can operate in the -40℃ to +125℃ junction temperature range.

APPLICATIONS

Industrial Low Power Systems
Laptops and Notebook Computers
LCD Monitors and TVs
Green Electronics and Appliances
DSP, FPGA and ASIC Power Supplies

FEATURES

- 8A Output Current
- Fixed Output Voltages
- Wide Input Voltage Range:
  - 4.5V to 23V Input Range for SGM61280-3.3
  - 5.1V to 23V Input Range for SGM61280-5.1
- Constant On-Time (COT) Control
- Low R_{DSON} MOSFET Switches (22mΩ/7mΩ)
- Fast Transient Response, Accurate Regulation
- Supports All Low ESR MLCC Output Capacitors
- Fixed Switching Frequency
- LDO Output Voltage
- Internal Soft-Start
- Integrated Output Discharge Resistance
- Cycle-by-Cycle Valley Over-Current Protection
- Input Under-Voltage Lockout
- Thermal Shutdown Protection
- Output Over/Under-Voltage Protection
- Audio Avoid Mode (AAM) to Avoid PFM Acoustic Noise
- Available in a Green UTQFN-3×3-12AL Package

TYPICAL APPLICATION

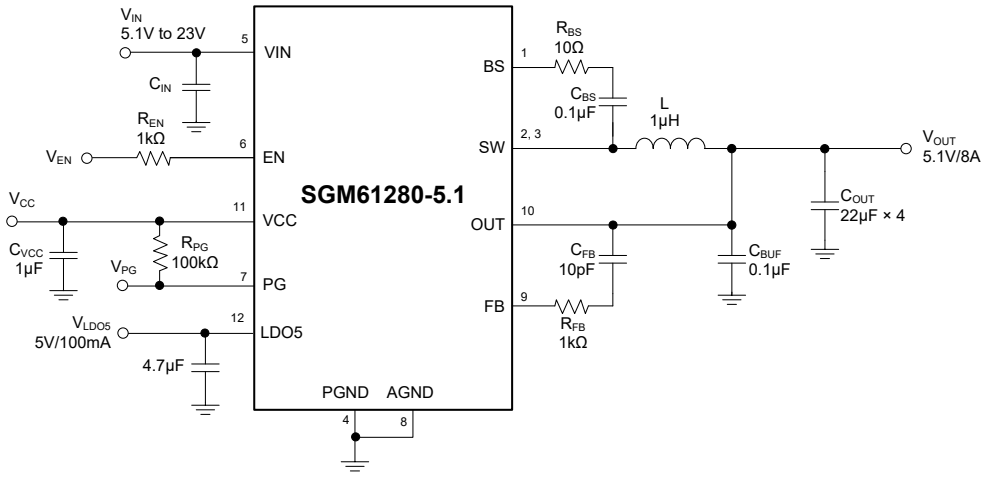


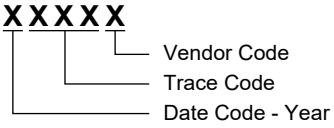
Figure 1. SGM61280-5.1 Typical Application

PACKAGE/ORDERING INFORMATION

MODEL	V_{OUT} (V)	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61280-5.1	5.1	UTQFN-3×3-12AL	-40℃ to +125℃	SGM61280-5.1XUSD12G/TR	SGM02A XUSD12 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN} ..... -0.3V to 27V
Enable Pin Voltage, EN ..... -0.3V to 27V
FB Pin Voltage, FB ..... -0.3V to 4.5V
OUT Pin Voltage, V_{OUT} (SGM61280-3.3)..... -0.3V to 4.5V
OUT Pin Voltage, V_{OUT} (SGM61280-5.1)..... -0.3V to 6V
Switch Voltage
SW (DC)..... -0.3V to (V_{IN} + 0.3V)
SW (AC, Less than 30ns)..... -5V to 28V
BS Voltage, V_{BS} ..... (V_{SW} - 0.3V) to (V_{SW} + 6V)
Other I/O Pin Voltages..... -0.3V to 6V
Power Dissipation, P_D @ T_A = +25℃
UTQFN-3×3-12AL.....1.5W
Package Thermal Resistance
UTQFN-3×3-12AL, θ_{JA}..... 82℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃

RECOMMENDED OPERATING CONDITIONS

Supply Input Voltage V_{IN} (SGM61280-3.3) .....4.5V to 23V
Supply Input Voltage V_{IN} (SGM61280-5.1) .....5.1V to 23V
Operating Junction Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

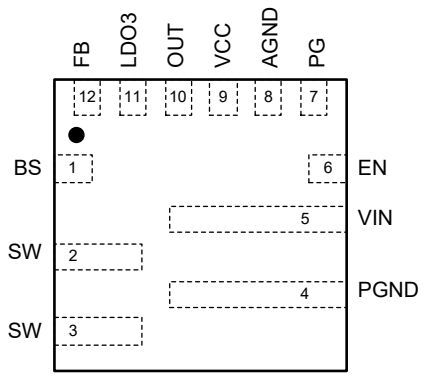
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

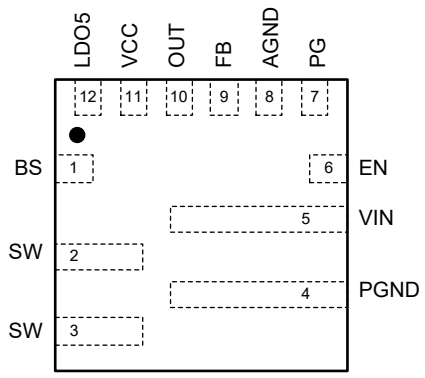
PIN CONFIGURATIONS

SGM61280-3.3 (TOP VIEW)



UTQFN-3×3-12AL

SGM61280-5.1 (TOP VIEW)



UTQFN-3×3-12AL

PIN DESCRIPTION

SGM61280 -3.3	SGM61280 -5.1	NAME	FUNCTION
1	1	BS	Upper Gate Driver Supply Bootstrap Input. Place a 0.1μF/10V ceramic capacitor C_{BS} in series with a 10Ω R_{BS} resistor between BS and SW pins as close as possible to the IC.
2, 3	2, 3	SW	Switching Node Output of the Internal Switches. These pins connect to one terminal of the output inductor and the bootstrap circuit. Keep this trace short with minimal copper area to minimize noise coupling, but it should be enough to carry inductor current.
4	4	PGND	Power Ground.
5	5	VIN	Input Supply Pin. Decouple this pin to PGND with at least 10μF ceramic capacitor as close as possible to these two pins.
6	6	EN	Enable Input. Applying a logic high voltage (above 0.6V and below V_{IN}) to EN pin enables the device and a logic low (below 0.5V) will shut it down. EN pin should not be left open. This pin is also used to activate the audio avoid mode (AAM) to prevent audio noise at light loads. The AAM is allowed if the V_{EN} voltage is in the 0.6V to 1.9V range. The device is enabled without AAM if V_{EN} is between 2V and V_{IN}.
7	7	PG	Open-Drain Power Good Indicator. With a pull-up resistor, this output will go high when the V_{OUT} is above 90% of is nominal value. Pull it up to VCC or a 5.5V or less voltage rail with a resistor (like 100kΩ).
8	8	AGND	Analog Ground. Decouple VCC to AGND with a 1μF ceramic capacitor.
9	11	VCC	5.5V Internal Supply Linear Regulator Output. Connect a 1μF ceramic capacitor between VCC and AGND pins as close to the device as possible.
10	10	OUT	Output Feedback Pin. OUT is an input pin into the IC and must be connected to the output capacitor (regulation point). Output discharge (56Ω) is also through this pin when the device is disabled. It also replaces VIN as input source of the LDO regulator when the V_{OUT} is high enough (>3.1V for SGM61280-3.3 and >4.7V for SGM61280-5.1 devices respectively).
11	—	LDO3	3.3V LDO Output (SGM61280-3.3 Only). It is the power supply source for the internal analog and gate driving circuits, and it can supply up to 100mA to external loads. It must be decoupled to PGND with at least a 4.7μF ceramic capacitor.
12	9	FB	Feedback Input Pin. Connect the output voltage with an RC network for closed loop control. Keep this line away from noise sources such as SW node.
—	12	LDO5	5.0V LDO Output (SGM61280-5.1 Only). It is the power supply source for the internal analog and gate driving circuits and can supply up to 100mA to external loads. It must be decoupled to PGND with at least a 4.7μF ceramic capacitor.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply						
VIN Input Voltage Range	V_{IN}	SGM61280-3.3	4.5		23	V
		SGM61280-5.1	5.1		23	
Shutdown Current into VIN	I_{SD}	V_{EN} = 0V		66		μA
Quiescent Current into VIN	I_Q	V_{EN} = 2.3V, no load		138		μA
Under-Voltage Lockout Threshold	V_{UVLO}	SGM61280-3.3, rising V_{IN}		TBD		V
		SGM61280-5.1, rising V_{IN}		5.1		
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}			239		mV
Logic Input Threshold						
EN Input Low Threshold	V_{EN_L}	Shutdown below this threshold.		0.5		V
EN Input High Threshold	V_{EN_H}	Enabled above this threshold.		0.6		V
Allow Audio Avoid Mode	V_{EN_H1}	Allow AAM		1.9		V
Do not Allow Audio Avoid Mode	V_{EN_H2}	Normal Mode		2.2		V
Output Voltage						
Output Voltage	V_{OUT}	SGM61280-3.3		TBD		V
		SGM61280-5.1		5.1		
VCC Regulator Voltage	V_{CC}	Internal regulator		5.5		V
Discharge Pull Down Resistance	R_{DIS}	V_{EN} = 0V		56		Ω
Soft-Start						
Soft-Start Time	t_{SS}	From EN rising to PG Release to High		1.8		ms
Output Rising Time	t_R	V_{OUT} rising from 10% to 90%		0.7		ms
Power Switch						
High-side Switch On-Resistance	R_{ON_HS}			22		mΩ
Low-side Switch On-Resistance	R_{ON_LS}			7		mΩ
Current Limit						
Low-side Switch Current Limit	I_{LIM_LS}			13		A
Switching Frequency						
PWM Switching Frequency	f_{SW}	SGM61280-3.3		TBD		kHz
		SGM61280-5.1		624		
Timer Control						
Minimum On-Time	t_{ON_MIN}	V_{IN} = $V_{IN(MAX)}$		60		ns
Minimum Off-Time	t_{OFF_MIN}			230		ns
Audio Avoid Mode (AAM)						
Operation Period	t_{ASMD}			30		μs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, typical values are provided at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Over-Voltage Protection						
Output Over-Voltage Threshold	OVP_TH	Rising (% of V_{OUT})		120		%
Output Over-Voltage Hysteresis		In % of V_{OUT}		5		%
Output Over-Voltage Delay Time				20		μs
Output Under-Voltage Protection						
Output Under-Voltage Threshold	UVP_TH	Falling (% of V_{FB})		61		%
Output Under-Voltage Delay Time		FB Forced below UVP Threshold		20		μs
UVP Blanking Time		From EN rising edge		1.8		ms
Power Good						
PG Threshold	PG_TH	PG going from Low to High (V_{OUT} Rising)		90		%
PG Hysteresis				15		%
PG Delay Time		PG released to go from Low to High		10		μs
LDO Regulator						
LDO Output Voltage	V_{LDO5}	SGM61280-5.1 only		5		V
	V_{LDO3}	SGM61280-3.3 only		TBD		
LDO Dropout Voltage	$V_{DROPOUT}$	V_{IN} = 5.5V		573		mV
LDO Output Current Limit	LDO_ILM			183		mA
Bypass MOSFET On-Resistance	R_{ON_BP}			3		Ω
Thermal Protection						
OTP Shutdown Threshold	T_{SD}			150		℃

TYPICAL APPLICATION CIRCUITS

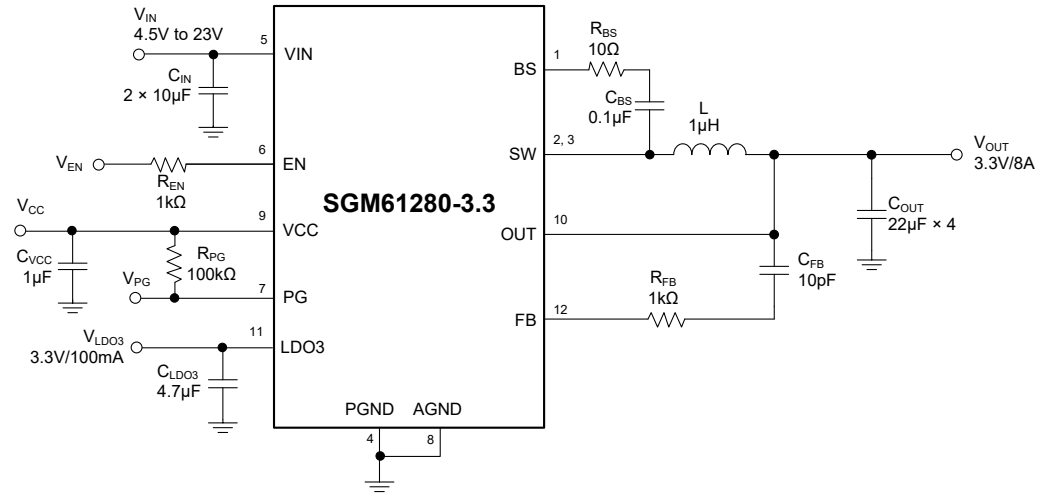


Figure 2. SGM61280-3.3 Typical Application Circuit

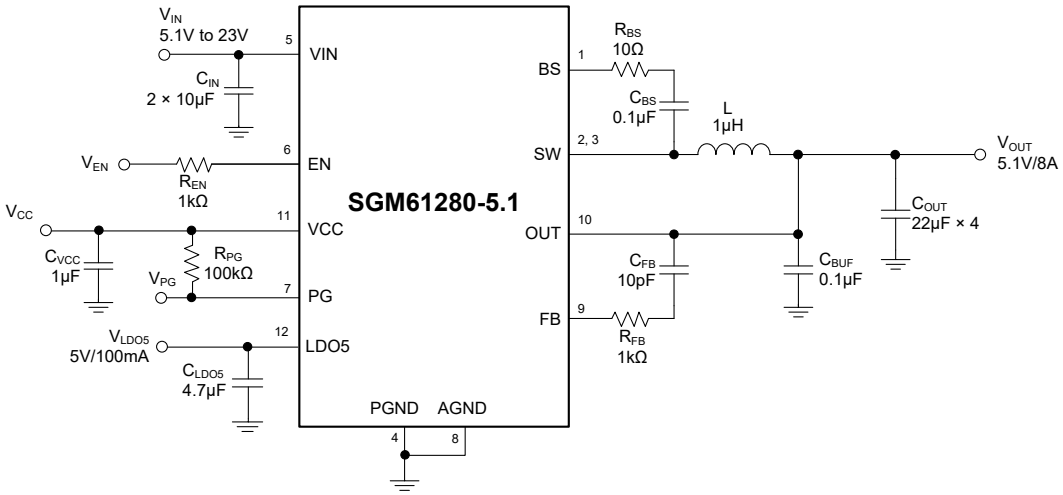


Figure 3. SGM61280-5.1 Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

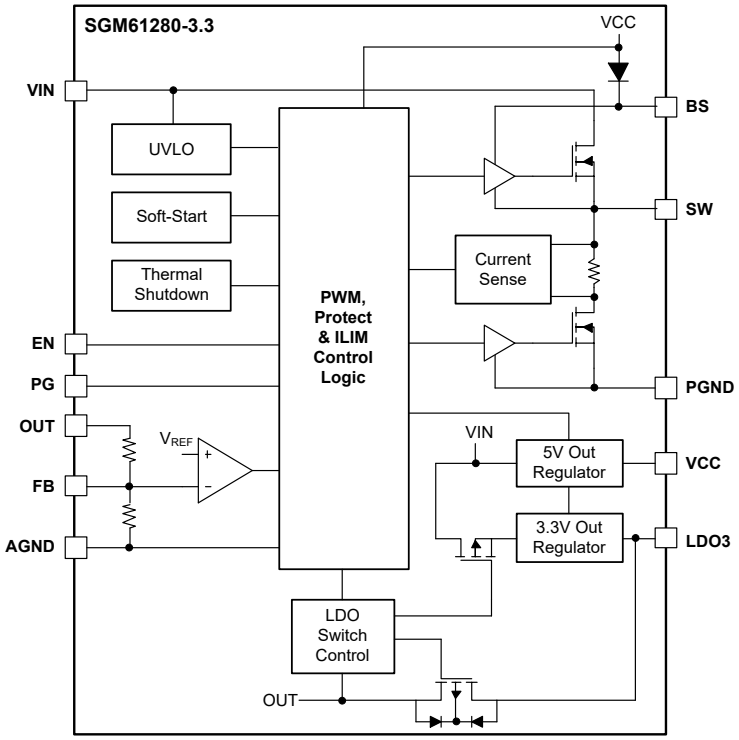


Figure 4. SGM61280-3.3 Block Diagram

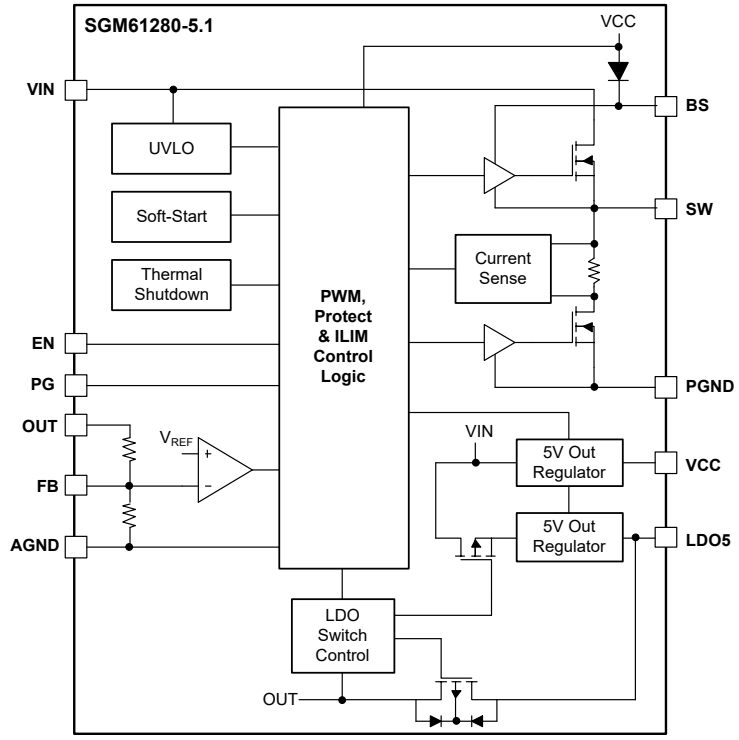


Figure 5. SGM61280-5.1 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61280 is a wide input voltage synchronous Buck converter with constant on-time (COT) control and integrated low R_{DSON} power MOSFETs. The COT control loop allows stable operation and fast transient response even with low ESR output ceramic capacitors and no complicated external compensation. It can deliver 8A output current due to its integrated synchronous buck converter with low R_{DSON} switches. The V_{IN} input range for SGM61280-3.3 is from 4.5V to 23V and for SGM61280-5.1 is from 5.1V to 23V.

The proprietary technology used in the COT control for this device, provides excellent load and line regulation and very fast transient response along with high flexibility.

Transient response is almost instantaneous because the COT is not clock-based unlike other methods using clocked PWM where the loop reacts to the events in the next clock cycles. Therefore, the inductor current reacts to deviations immediately to keep the output in regulation.

This device can employ both low ESR (like POSCAP or SP-CAP) and ultra-low ESR ceramic capacitors for output capacitance.

A linear regulator with 100mA output capacity is provided in the device (3.3V for the SGM61280-3.3 and 5.0V for the SGM61280-5.1). If V_{OUT} exceeds 3.1V (for 3.3V) or 4.7V (for 5.0V), the regulator source will automatically switch from the input (V_{IN}) to the output (V_{OUT}) through OUT pin to minimize the losses.

Under-Voltage Lockout (UVLO)

The input voltage (V_{IN}) is continuously monitored and if it falls below the under-voltage lockout falling threshold, the device will shut down. The UVLO is necessary to avoid device malfunction due to low supply voltage such as insufficient gate voltage for turning the power switches to fully on-state.

The UVLO is non-latching and if V_{IN} exceeds the under-voltage lockout rising threshold (if EN is logic high), device will exit shutdown and resume switching.

Enable Input (EN)

The active-high EN input pin can be used to enable or shutdown the device and to allow the audio avoid mode (AAM). If EN is a logic low voltage (below 0.5V), device will shut down. If EN is a logic high (above 0.6V) and $V_{IN} > V_{UVLO}$, the device will be enabled.

This pin is also used to activate the audio avoid mode (AAM) to prevent audio noise at light loads. If the EN voltage is in the 0.6V to 1.9V range, the device is allowed to enter AAM during light load PFM to prevent acoustic noise.

The LDOx output and VCC are in on-state as long as $V_{IN} > V_{UVLO}$. See Table 1 for the SGM61280 power logic.

Table 1. SGM61280 Regulator States vs. EN Input

Device	EN	VCC	V_{OUT}	LDOx
SGM61280-3.3 and SGM61280-5.1	High	ON	Enabled	ON
	Low	ON	Disabled	ON

Bootstrap Circuit (C_{BS} and R_{BS})

The high-side (HS) switch gate driver needs a voltage higher than V_{IN} to turn on the gate of the high-side N-MOSFET switch (for example, 5V + V_{IN} or higher). The external bootstrap capacitor (C_{BS}) is used to provide this higher voltage for supplying the HS gate driver. C_{BS} is charged through the internal bootstrap diode from VCC when the low-side (LS) switch turns on and SW node is at around 0V. When the LS switch turns off and HS switch turns on, the SW voltage will rise to the V_{IN} rail voltage and the C_{BS} voltage will supply the HS driver.

Refer to Figure 2 and Figure 3 for C_{BS} and R_{BS} combinations. Use a 0.1μF ceramic capacitor (C_{BS}) with lower ESR and a series 10Ω resistor (R_{BS}) between the BS and the SW pins for bootstrapping.

The R_{BS} helps to control the turn-on time of the HS switch and is good to compromise the switching loss and the EMI radiation. The gate driver is designed for fast turn-on and minimal switching loss (that is, for good efficiency). But the additional resistance of the R_{BS} can slow down the turn-on (V_{SW} rising) to reduce the EMI at the expense of small increase in the switching loss due to the longer turn-on time of the HS switch.

DETAILED DESCRIPTION (continued)

Soft-Start

An internal 0.7ms (TYP) soft-start ramp circuit is implemented to gradually increase the PWM reference voltage for output regulation, in order to limit the startup inrush current from the source and to prevent unwanted over-current protection trips during power-up. This timer starts when EN goes high (if $V_{IN} > V_{UVLO}$) or when V_{IN} exceeds the under-voltage lockout rising threshold if EN is already high.

VCC and LDO3/LDO5 (Linear Regulators)

VCC regulator is powered from VIN to power the internal circuitry and the gate drivers. It should be decoupled with a 1μF ceramic capacitor close to the device.

The LDO3 (3.3V) or LDO5 (5.0V) can deliver 100mA to external loads. The LDO should be decoupled with at least 4.7μF ceramic capacitor. When V_{OUT} exceeds above 3.1V (SGM61280-3.3) or 4.7V (SGM61280-5.1), the source of the LDO will automatically switch from VIN to OUT by an internal MOSFET to minimize LDO losses.

Power Good Indicator Output (PG)

The PG pin is an open-drain output with a pull-up resistor which will go to logic high if the output voltage is near its expected value. It is recommended to connect a 100kΩ pull-up resistor to a high rail which is not larger than 5V. V_{PG} will be pulled low, if V_{OUT} drops below 85% (TYP) of its nominal value and will go high if it exceeds 90% of the nominal regulation value.

PG is held low during soft-start state. To avoid false signaling, PG responds with a 10μs delay and changes state if at the end of this delay, the new state is still valid.

Output Over/Under-Voltage Protection

An over-voltage protection (OVP) is triggered if the V_{OUT} exceeds the over-voltage threshold (above regulation) for about 20μs or longer. Upon OVP trip, the HS switch remains off and the LS switch remains on until the inductor current drops to zero and then the device will shut down.

Output voltage is also protected against under-voltage protection (UVP). If the output voltage falls and remains below the under-voltage threshold for about 20μs, the device will shut down.

After OVP or UVP, the device will shut down in latch-off mode and will not restart automatically. An EN toggle or V_{IN} power cycling is needed to restart the device.

Pulse Frequency Modulation Mode (PFM)

In light loads, the SGM61280 can enter the PFM mode to keep the efficiency high. Light load condition is detected at the CCM and DCM boundary condition in which inductor valley current reaches to zero due to the output current drop.

In PFM, upon detection of zero inductor current, the LS switch turns off and the output capacitor will take longer time to discharge (t_{OFF} extends) until the V_{OUT} (or V_{FB}) drops to the level needed to begin a new cycle (HS turn on or t_{ON} pulse).

Audio Avoid Mode (AAM)

To avoid acoustic noise when the PFM frequency drops below audible range (20kHz), the AAM can be activated by bringing the EN voltage between 0.6V and 1.9V. In this mode, a special diode emulation mode will be activated to keep the minimum switching period to about 30μs (about 33.3kHz), which is called audio avoid mode. This mode can keep the switching frequency above the hearing range even in no load condition.

Output Current Limit (OCP)

A cycle-by-cycle valley current detection is implemented to limit the output current. During T_{OFF} portion of each cycle (in which LS is conducting), the current of the synchronous rectifier (LS switch) is monitored by measuring its drain-to-source voltage that is proportional to its current. This measurement is temperature compensated for better accuracy. If the valley current exceeds the threshold, the one-shot timer that produces the constant on-time (for the t_{ON} period) will be disabled and not allowed until the inductor current, which is going through LS during t_{OFF}, drops below the valley current limit. During current limiting, the output voltage will drop because the required load current is not supplied by the inductor. If the output voltage drops below the output UVP level (see **Output Over/Under-Voltage Protection** section), the device will shut down and stop switching to avoid over temperature.

Thermal Shutdown

The die temperature (T_J) is constantly monitored for over-temperature protection (OTP). If T_J exceeds the T_{SD} threshold (+150°C, TYP), the device shuts down to avoid damage. OTP is a latch-off mode protection and an EN toggle or V_{IN} power cycling is needed to restart the device.

LAYOUT

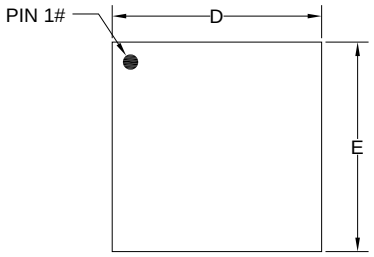
Designing a good PCB layout has a significant impact on the performance of a switching power supply. For the SGM61280, the layout design can be more critical due to the high switching frequency, high output current and more sensitivity of the COT controllers to the noise. One of the goals of a good layout is minimizing the EMI radiations and the influence (coupling) of the switching noise on the sensitive feedback routes. The voltage gradients induced on the ground planes or other sensitive routes should be minimized to avoid switching instability and deviation from regulation point.

The following layout guidelines are recommended to get the best performance from the SGM61280.

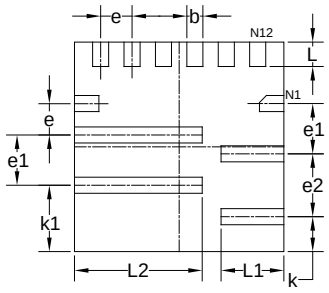
- Consider short, straight, and wide copper traces for the main current paths.
- Place the input capacitor and the output capacitor close to the device with the shortest possible connection traces.
- Keep the SW node area minimal. Also keep this node and the components directly connecting to it away from sensitive copper traces and feedback elements (such as FB and OUT pins). Avoid using vias for SW node and make it thick and short for high current.
- Along with the SW, the PGND pin serves as a main heatsinking path. Connect PGND to a large ground plane and stitch it with thermal vias to ground planes on the other layers and specifically to the back side of the PCB for heat sinking and noise reduction.
- Feedback route must be wide and away from the SW node. The input of the 100mA LDO is supplied directly from the OUT feedback line.
- For less parasitic inductance, use multiple vias under the device on near VIN, PGND and the decoupling capacitors pads.

PACKAGE OUTLINE DIMENSIONS

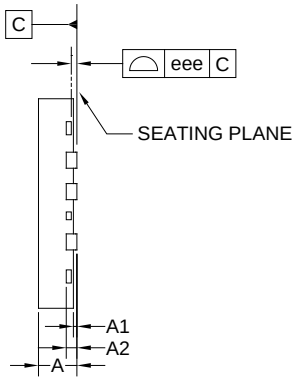
UTQFN-3×3-12AL



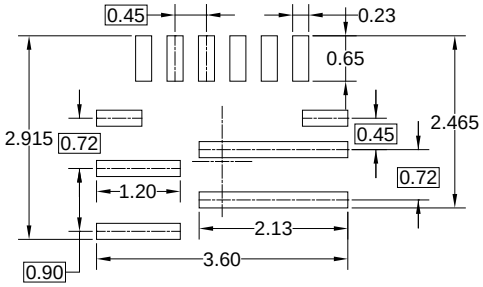
TOP VIEW



BOTTOM VIEW



SIDE VIEW



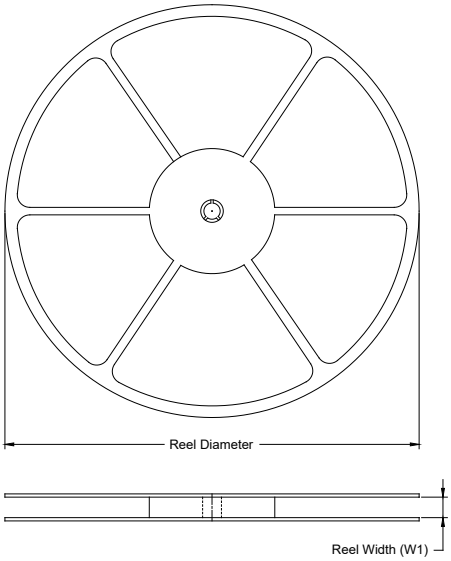
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.510	0.550	0.600
A1	0.000	-	0.050
A2	0.152 REF		
b	0.180	0.230	0.280
D	2.900	3.000	3.100
E	2.900	3.000	3.100
e	0.450 BSC		
e1	0.720 BSC		
e2	0.900 BSC		
k	0.500 REF		
k1	0.950 REF		
L	0.250	0.350	0.450
L1	0.800	0.900	1.000
L2	1.730	1.830	1.930
eee	-	0.080	-

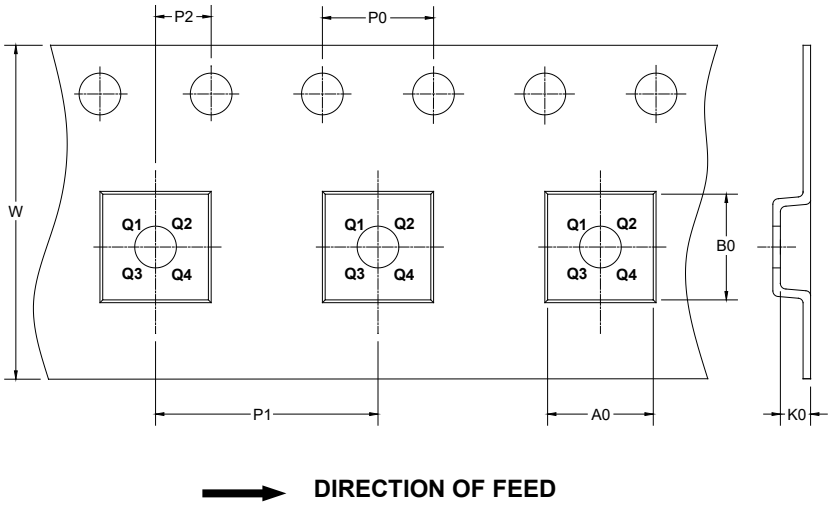
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



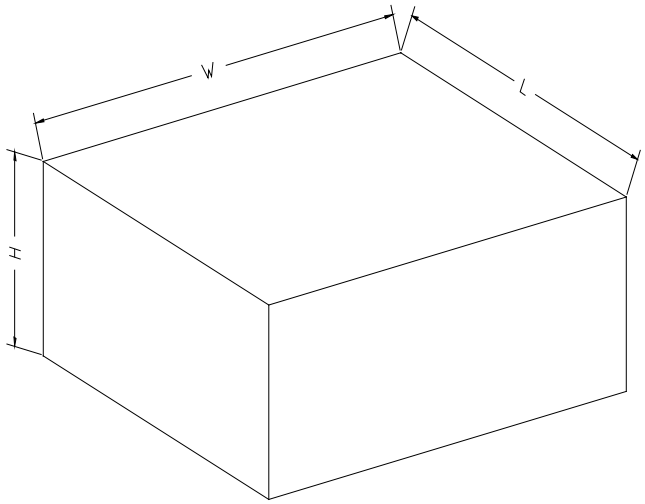
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTQFN-3×3-12AL	13"	12.4	3.30	3.30	0.80	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002