具有快速瞬态响应的 TPS7A03 毫微功耗 I_Q、200nA、200mA、低压降稳压器

1 特性

- 超低 I_Q：200nA（典型值），即使处于压降状态
- 关断 I_Q：3nA（典型值）
- 出色的瞬态响应（1mA 至 50mA）
  - 建立时间小于 10µs
  - 80mV 下冲
- 封装：
  - 1.0mm × 1.0mm X2SON
  - SOT23-5
  - 0.64mm x 0.64mm DSBGA（预发布）
- 输入电压范围：1.5V 至 6.0V
- 输出电压范围：0.8V 至 5.0V（固定）
- 输出精度：在工作温度范围内为 1.5%
- 智能使能端下拉
- 超低压降：
  - 在 200mA 下为 270mV（最大值）(V_{OUT} = 3.3V)
- 与 1µF 或更大的电容器一起工作时保持稳定

2 应用

- 可穿戴电子产品
- 恒温器、烟雾和热量探测器
- 燃气表、热量表和水表
- 血糖监测仪和脉动式血氧计
- 住宅断路器和故障指示灯
- 楼宇安全和视频监控设备
- EPOS 读卡器

3 说明

TPS7A03 是一款超小型、超低静态电流低压降线性稳压器 (LDO)，可提供 200mA 的电流以及出色的瞬态性能。

TPS7A03 具有超低 I_Q (200nA)，专为将超低静态电流作为关键参数的 应用 而设计。此器件即使在压降模式下也能保持低 I_Q 消耗，以进一步延长电池寿命。在关断模式或禁用模式下，该器件消耗超低 (
3nA I_Q)，有助于延长电池货架期。TPS7A03 输出电压范围为 0.8V 至 5.0V，步长为 50mV，以支持更低的现代微控制器 (MCU) 内核电压。

TPS7A03 配备 具有内部控制下拉电阻的智能使能电路，该电阻即使在 EN 引脚悬空时也能保持 LDO 处于禁用状态，有助于最大限度减少用于下拉 EN 引脚的外部组件。此电路还有助于在器件处于禁用状态时最大限度减小外部下拉电路中流过的电流。

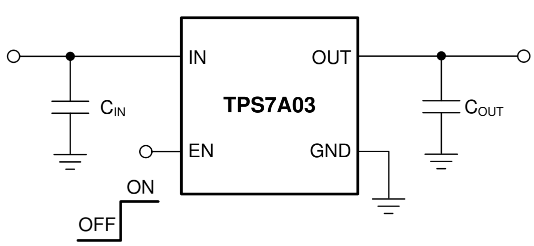
TPS7A03 的额定工作温度范围为 T_J = –40°C 至 +125°C。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TPS7A03	X2SON (4)	1.00mm × 1.00mm
	DSBGA (4)[(2)]	0.64mm × 0.64mm
	SOT-23 (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。
(2) 预发布封装。

典型应用电路



目录

4 修订历史记录

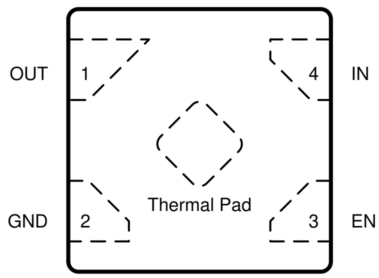
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2019) to Revision B	Page
• 已更改 将 DBV (SOT23-5) 封装从“预发布”更改为“生产数据”	1

Changes from Original (July 2019) to Revision A	Page
• 已更改 将器件状态从“预告信息”更改为“生产数据”	1

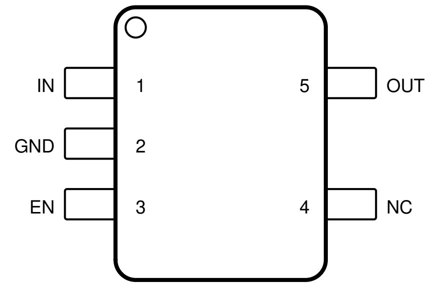
5 Pin Configuration and Functions

DQN Package
1-mm × 1-mm, 4-pin X2SON
Top View



Not to scale

DBV Package
5-Pin SOT-23
Top View



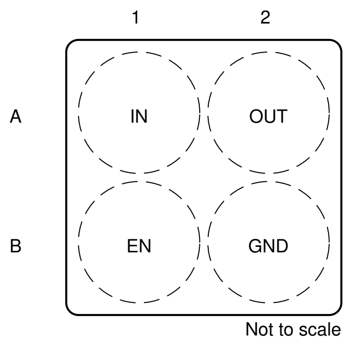
Not to scale

Pin Functions: DQN, DBV

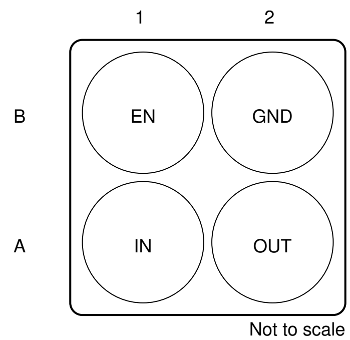
PIN			I/O(1)	DESCRIPTION
NAME	DQN	DBV		
EN	3	3	Input	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low or floating this pin disables the device. This pin features an internal pulldown resistor, which is disconnected when EN is driven high externally and the device has started up.
GND	2	2	—	Ground pin. This pin must be connected to ground on the board.
IN	4	1	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible.
NC	—	4	—	No connect pin. This pin is not internally connected. Connect to ground or leave floating.
OUT	1	5	Output	Regulated output pin. A 0.5-µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1-µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible; see the *Recommended Operating Conditions* table.
Thermal pad		—	—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to ground.

(1) NC = No internal connection.

YCH Package (Preview)
4-Pin DSBGA, 0.35-mm Pitch
Top View



YCH Package (Preview)
4-Pin DSBGA, 0.35-mm Pitch
Bottom View



Pin Functions: YCH

PIN		I/O	DESCRIPTION
NAME	YCH		
EN	B1	Input	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low or floating this pin disables the device. This pin features an internal pulldown resistor, which is disconnected when EN is driven high externally and the device has started up.
GND	B2	—	Ground pin. This pin must be connected to ground and the thermal pad.
IN	A1	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground; see the *Recommended Operating Conditions* table. Place the input capacitor as close to input of the device as possible.
OUT	A2	Output	Regulated output pin. A 0.5-µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1-µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible; see the *Recommended Operating Conditions* table.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.5	V
	V_{EN}	–0.3	6.5	
	V_{OUT}	–0.3	V_{IN} + 0.3 or 5.5(2)	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum is V_{IN} + 0.3 V or 5.5 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.5		6.0	V
V_{EN}	Enable voltage	0		6.0	V
V_{OUT}	Output voltage	0.8		5.0	V
I_{OUT}	Output current	0		200	mA
C_{IN}	Input capacitor		1		µF
C_{OUT}	Output capacitor(1) (2)	1	1	22	µF
F_{EN}	EN toggle frequency			10	kHz
T_J	Operating junction temperature	–40		125	°C

(1) Effective output capacitance of 0.5 µF minimum required for stability.
(2) 22 µF is the maximum derated capacitance that can be used for stability.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A03			UNIT
		DQN (X2SON)	DBV (SOT-23-5)	YCH (DSBGA)	
		4 PINS	5 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179.1	181.9	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	137.6	53.0	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	116.3	88.1	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	27.1	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	116.3	52.7	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	112.3	N/A	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Nominal accuracy	T_J = 25°C, V_{OUT} ≥ 1.5 V, 1 µA(1) ≤ I_{OUT} ≤ 1 mA		–1		1	%
	Nominal accuracy	T_J = 25°C; V_{OUT} < 1.5 V		–15		15	mV
	Accuracy over temperature	V_{OUT} ≥ 1.5 V	T_J = –40°C to +125°C	–1.5		1.5	%
	Accuracy over temperature	V_{OUT} < 1.5 V	T_J = –40°C to +125°C	–20		20	mV
$\Delta V_{OUT}(\Delta V_{IN})$	Line regulation	$V_{OUT(nom)}$ + 0.5 V ≤ V_{IN} ≤ 6.0 V(2)	T_J = –40°C to +125°C			5	mV
$\Delta V_{OUT}(\Delta I_{OUT})$	Load regulation(3)	1 mA ≤ I_{OUT} ≤ 200 mA, V_{IN} = $V_{OUT(nom)}$ + 0.5 V(2)	T_J = –40°C to +85°C		20	38	mV
			T_J = –40°C to +125°C			50	mV
I_{GND}	Ground current	I_{OUT} = 0 mA	T_J = 25°C		200	250	nA
			T_J = –40°C to +85°C			300	nA
I_{GND}/I_{OUT}	Ground current vs load current	20 µA ≤ I_{OUT} < 1 mA	T_J = 25°C		1		%
		1 mA ≤ I_{OUT} ≤ 100 mA	T_J = 25°C		0.25		%
		I_{OUT} ≥ 100 mA	T_J = 25°C		0.15		%
$I_{GND(DO)}$	Ground current in dropout(1)	I_{OUT} = 0 mA, V_{IN} = 95% x $V_{OUT(NOM)}$	T_J = 25°C		220		nA
I_{SHDN}	Shutdown current	V_{EN} = 0 V, 1.5 V ≤ V_{IN} ≤ 5.0 V, T_J = 25°C			3	10	nA
I_{CL}	Output current limit	V_{OUT} = 90% × $V_{OUT(nom)}$	V_{OUT} < 2.5V, V_{IN} = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 1.0 V	240	450	750	mA
			V_{OUT} ≥ 2.5V, V_{IN} = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.5 V	240	450	750	mA
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V			65		mA
V_{DO}	Dropout voltage(4)	T_J = –40°C to +85°C	0.8 V ≤ V_{OUT} < 1.0 V			1050	mV
			1.0 V ≤ V_{OUT} < 1.2 V			790	mV
			1.2 V ≤ V_{OUT} < 1.5 V			650	mV
			1.5 V ≤ V_{OUT} < 1.8 V			490	mV
			1.8 V ≤ V_{OUT} < 2.5 V			400	mV
			2.5 V ≤ V_{OUT} < 3.3 V			310	mV
			3.3 V ≤ V_{OUT} ≤ 5.0 V			270	mV
		T_J = –40°C to +125°C	0.8 V ≤ V_{OUT} < 1.0 V			1100	mV
			1.0 V ≤ V_{OUT} < 1.2 V			850	mV
			1.2 V ≤ V_{OUT} < 1.5 V			700	mV
			1.5 V ≤ V_{OUT} < 1.8 V			560	mV
			1.8 V ≤ V_{OUT} < 2.5 V			450	mV
			2.5 V ≤ V_{OUT} < 3.3 V			360	mV
			3.3 V ≤ V_{OUT} ≤ 5.0 V			310	mV
PSRR	Power-supply rejection ratio	f = 1 kHz, I_{OUT} = 30 mA			55		dB
V_N	Output voltage noise	BW = 10 Hz to 100 kHz, V_{OUT} = 0.8 V, I_{OUT} = 30 mA			130		$µV_{RMS}$
V_{UVLO}	UVLO threshold	V_{IN} rising		1.23	1.3	1.47	V
		V_{IN} falling		1.0	1.12	1.41	V

(1) Specified by design
(2) V_{IN} = 2.0 V for V_{OUT} ≤ 1.5 V.
(3) Load Regulation is normalized to the output voltage at I_{OUT} = 1 mA.
(4) Dropout is measured by ramping V_{IN} down until V_{OUT} = $V_{OUT(nom)}$ x 95%, with I_{OUT} = 200 mA.

Electrical Characteristics (continued)

Specified at T_J = –40°C to +125°C, $V_{IN} = V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(HYST)}$	UVLO hysteresis	V_{IN} hysteresis		180		mV
$V_{EN(HI)}$	EN pin logic high voltage		1.1			V
$V_{EN(LOW)}$	EN pin logic low voltage				0.3	V
I_{EN}	EN pin leakage current	$V_{EN} = V_{IN}$ = 6.0 V		10		nA
$R_{EN(PULLDOWN)}$	Smart enable pulldown resistor	V_{EN} = 0.3 V		500		KΩ
$R_{PULLDOWN}$	Pulldown resistor	V_{IN} = 3.3 V, device disabled		60		Ω
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		145		

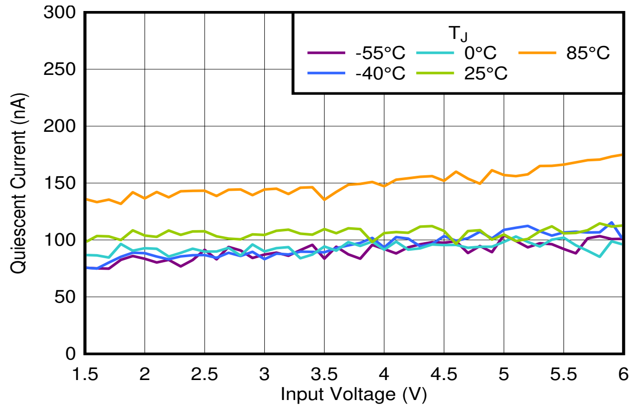
6.6 Switching Characteristics

Specified at T_J = –40°C to +125°C, $V_{IN} = V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, $V_{EN} = V_{IN}$, and $C_{IN} = C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	From EN assertion to V_{OUT} = 90% × $V_{OUT(nom)}$	0.8V ≤ V_{OUT} ≤ 1.5 V		500	800	µs
			1.5V < V_{OUT} ≤ 3.0 V		750	1200	
			3.0V < V_{OUT} ≤ 5.0 V		1200	1600	

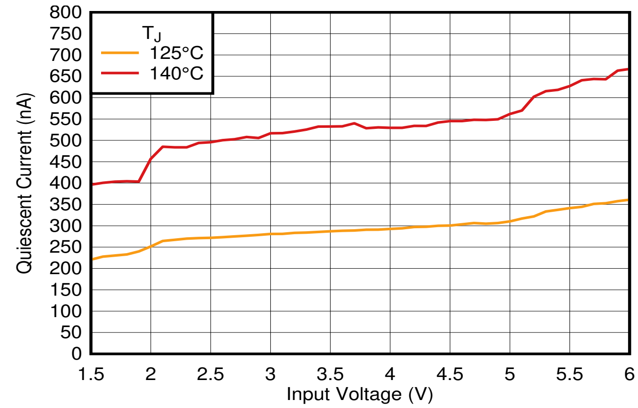
6.7 Typical Characteristics

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



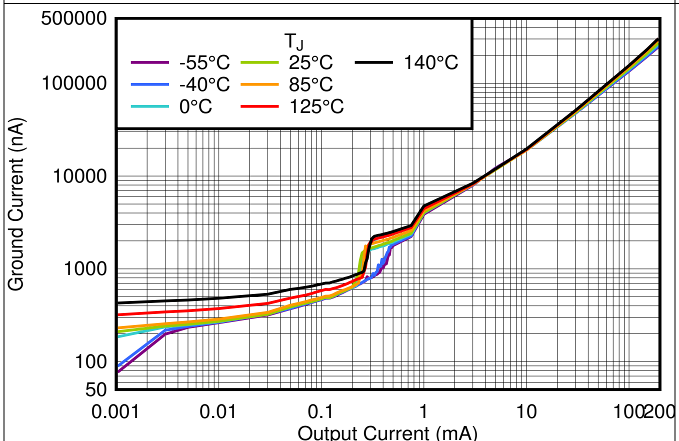
V_{OUT} = 1.8 V, V_{IN} = V_{EN} = 2.3 V

图 1. I_Q vs V_{IN} and Temperature



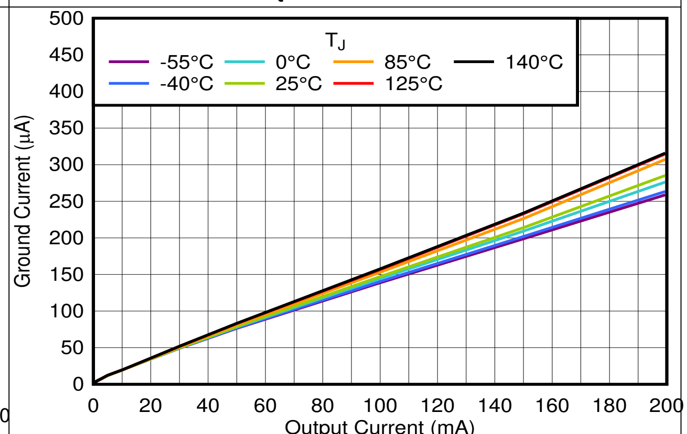
I_{OUT} = 0 mA, V_{EN} = V_{IN}

图 2. I_Q vs V_{IN} and Temperature



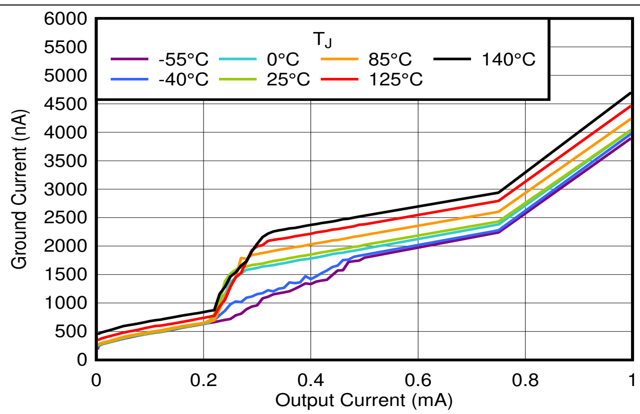
V_{OUT} = 1.8 V, V_{IN} = V_{EN} = 2.3 V

图 3. I_Q vs I_{OUT} and Temperature up to 200 mA



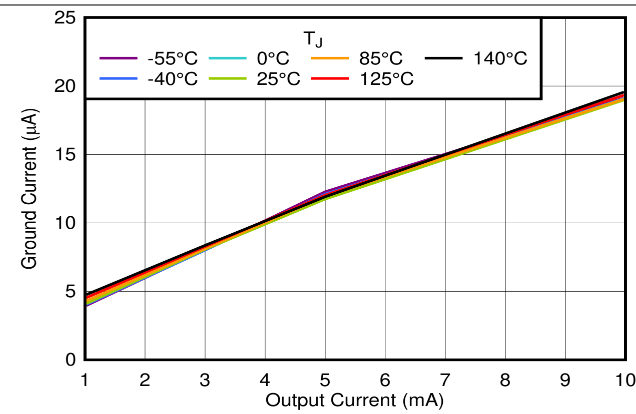
V_{OUT} = 1.8 V, V_{IN} = V_{EN} = 2.3 V

图 4. I_Q vs I_{OUT} and Temperature Up to 200 mA



V_{OUT} = 1.8 V, V_{IN} = V_{EN} = 2.3 V

图 5. I_Q vs I_{OUT} and Temperature Up to 1 mA

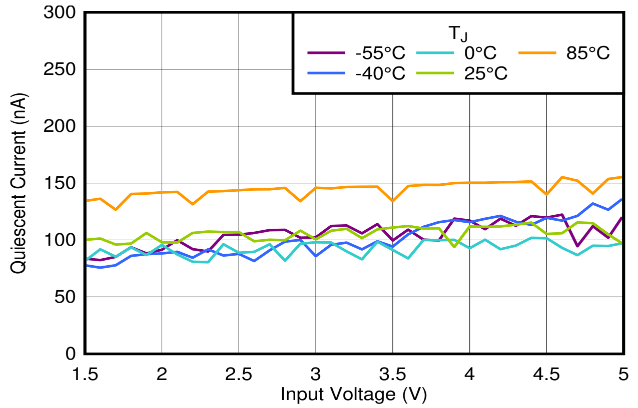


V_{OUT} = 1.8 V, V_{IN} = V_{EN} = 2.3 V

图 6. I_Q vs I_{OUT} and Temperature for 1 mA to 10 mA

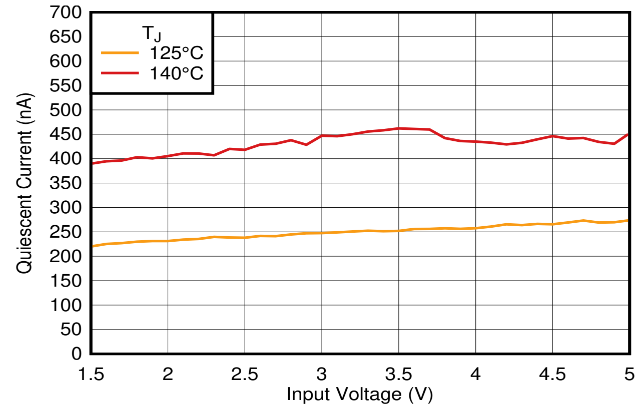
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



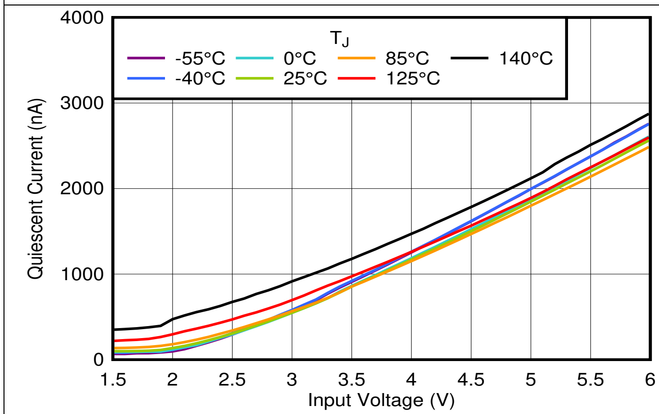
V_{OUT} = 5.0 V, V_{IN} = V_{EN}

图 7. I_Q in Dropout vs V_{IN} and Temperature



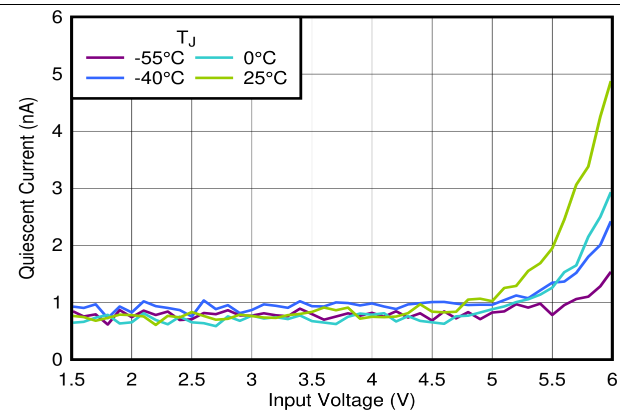
V_{OUT} = 5.0 V, V_{IN} = V_{EN}

图 8. I_Q in Dropout vs V_{IN} and Temperature



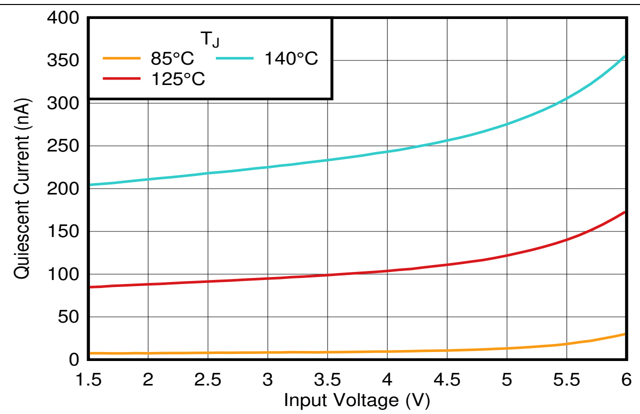
I_{OUT} = 0 mA, V_{EN} = 1.1 V

图 9. I_Q vs V_{IN} and Temperature



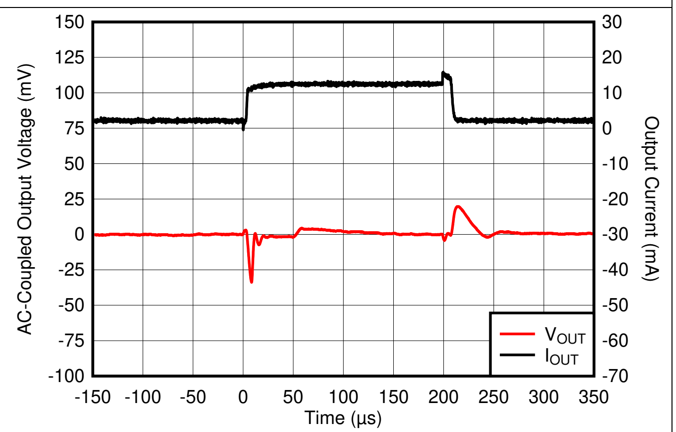
V_{EN} = 0 V

图 10. I_{SHDN} vs V_{IN} and Temperature



V_{EN} = 0 V

图 11. I_{SHDN} vs V_{IN} and Temperature

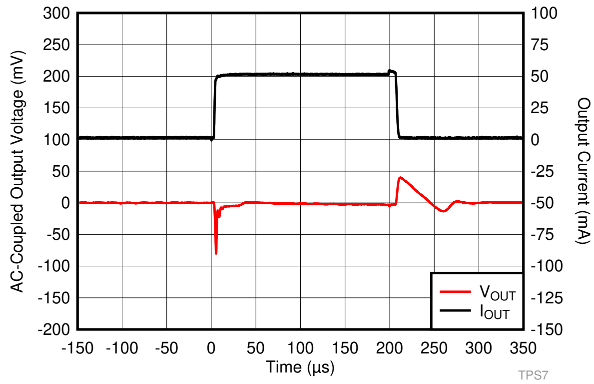


V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 12. I_{OUT} Transient From 1 mA to 10 mA

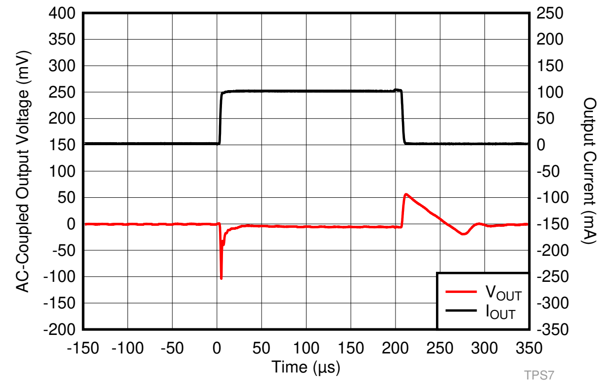
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



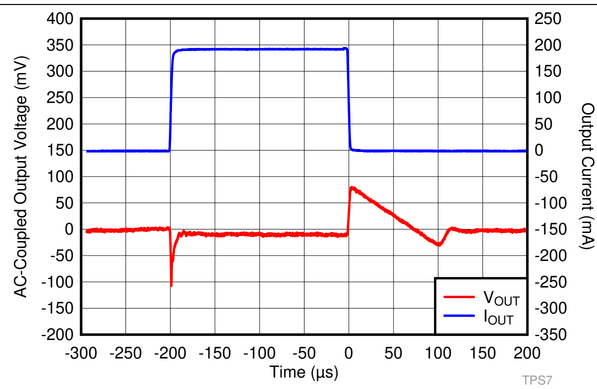
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 13. I_{OUT} Transient From 1 mA to 50 mA



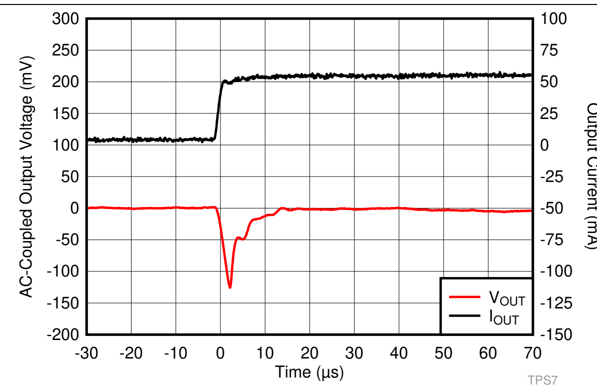
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 14. I_{OUT} Transient From 1 mA to 100 mA



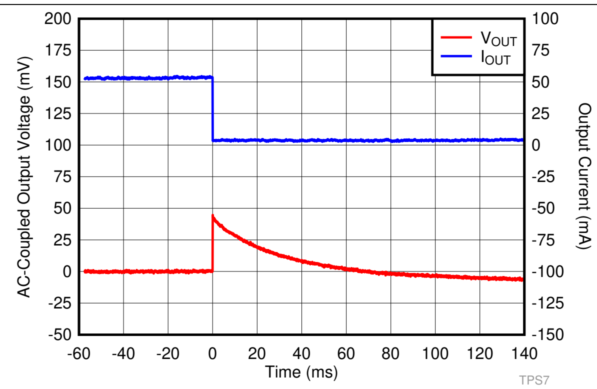
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 15. I_{OUT} Transient From 1 mA to 200 mA



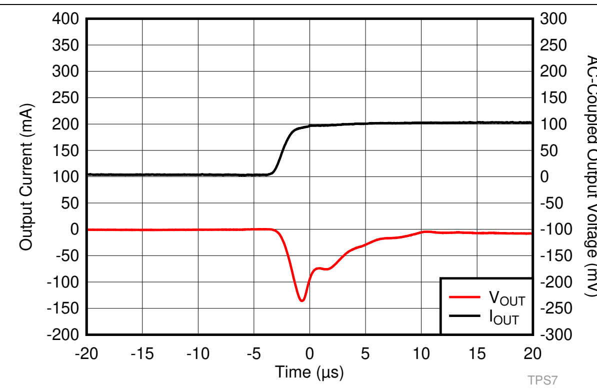
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 16. I_{OUT} Transient From 0 mA to 50 mA



V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 17. I_{OUT} Transient From 50 mA to 0 mA

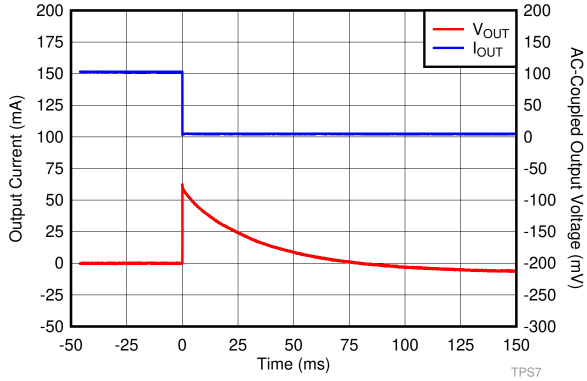


V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 18. I_{OUT} Transient From 0 mA to 100 mA

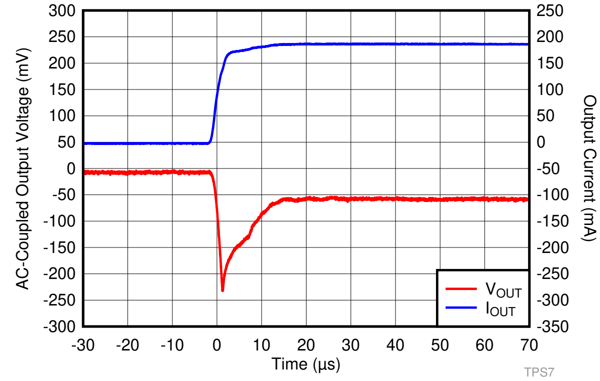
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



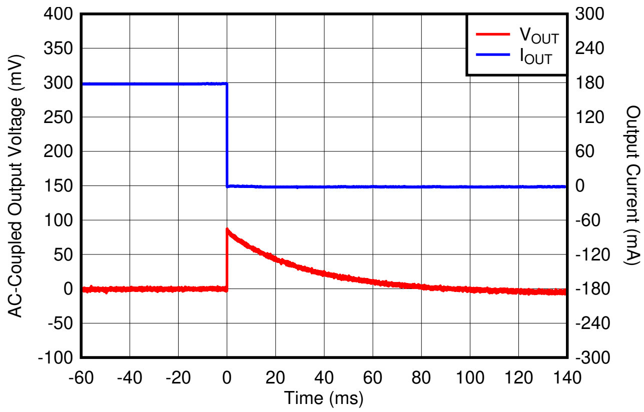
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 19. I_{OUT} Transient From 100 mA to 0 mA



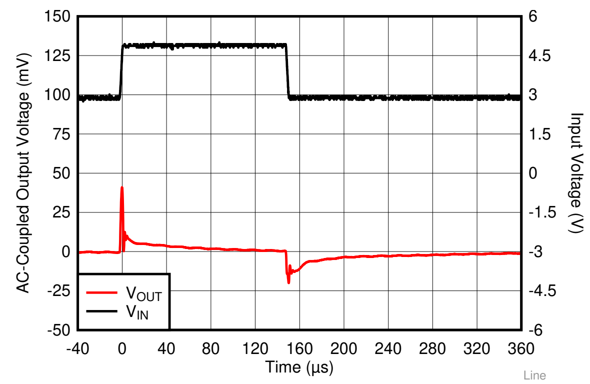
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 20. I_{OUT} Transient From 0 mA to 200 mA



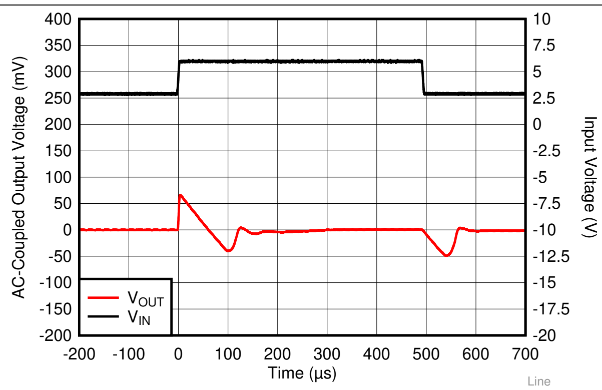
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF, t_r = t_f = 1 µs

图 21. I_{OUT} Transient From 200 mA to 0 mA



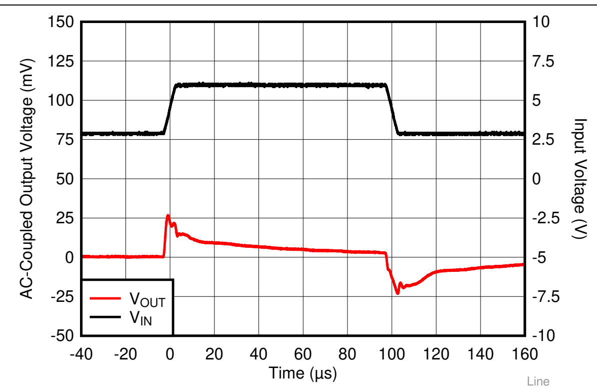
V_{OUT} = 1.8 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF, slew rate = 1 V/µs

图 22. V_{IN} Transient From 2.8 V to 4.8 V



V_{OUT} = 1.8 V, I_{OUT} = 1 mA, C_{OUT} = 1 µF, slew rate = 1 V/µs

图 23. V_{IN} Transient From 2.8 V to 6.0 V

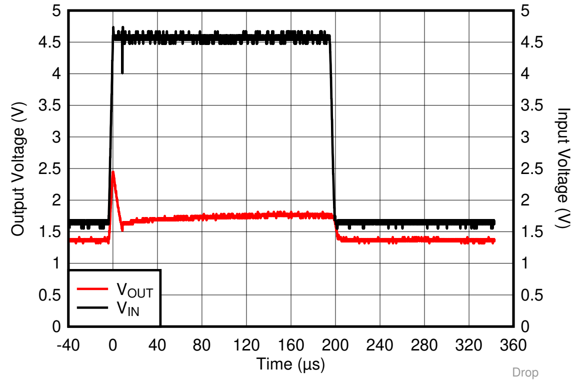


V_{OUT} = 1.8 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF, slew rate = 1 V/µs

图 24. V_{IN} Transient From 2.8 V to 6.0 V

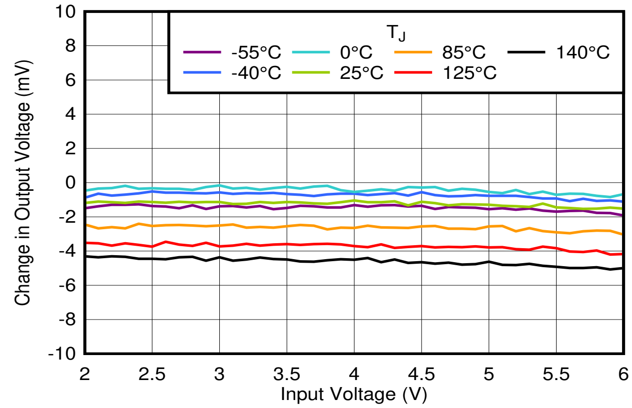
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



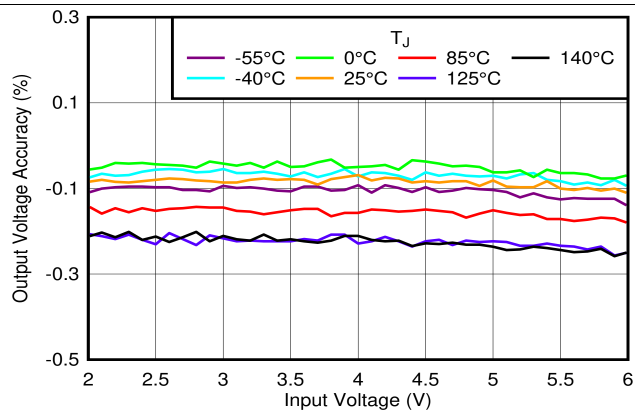
V_{OUT} = 1.8 V, I_{OUT} = 100 mA, C_{OUT} = 1 µF, slew rate = 1 V/µs

图 25. V_{IN} Transient From 1.5 V to 4.5 V



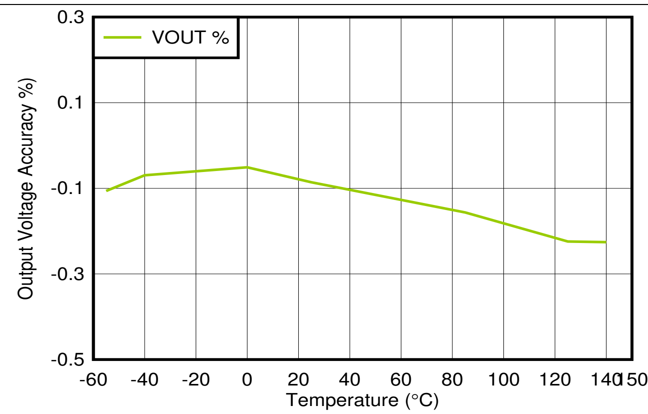
V_{OUT} = 1.8 V, I_{OUT} = 1 mA

图 26. Line Regulation vs V_{IN} and Temperature



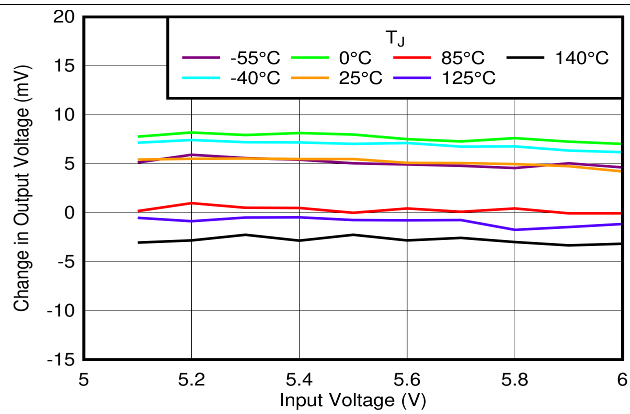
V_{OUT} = 1.8 V, I_{OUT} = 1 mA

图 27. Output Accuracy vs V_{IN} and Temperature



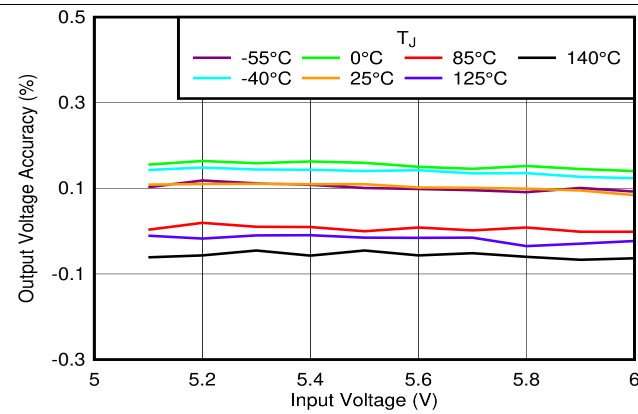
V_{OUT} = 1.8 V, I_{OUT} = 1 mA

图 28. Output Accuracy vs Temperature



V_{OUT} = 5.0 V, I_{OUT} = 1 mA

图 29. Line Regulation vs V_{IN} and Temperature

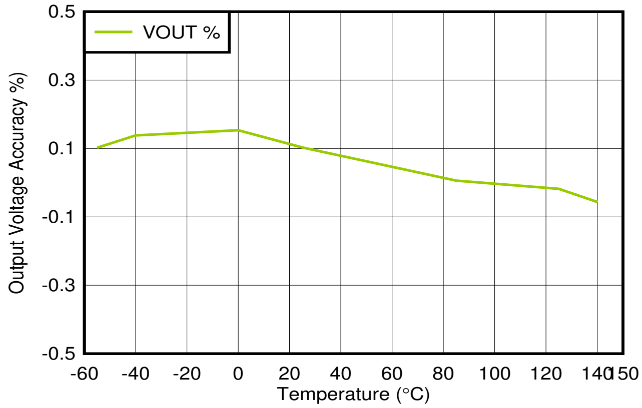


V_{OUT} = 5.0 V, I_{OUT} = 1 mA

图 30. Output Accuracy vs V_{IN} and Temperature

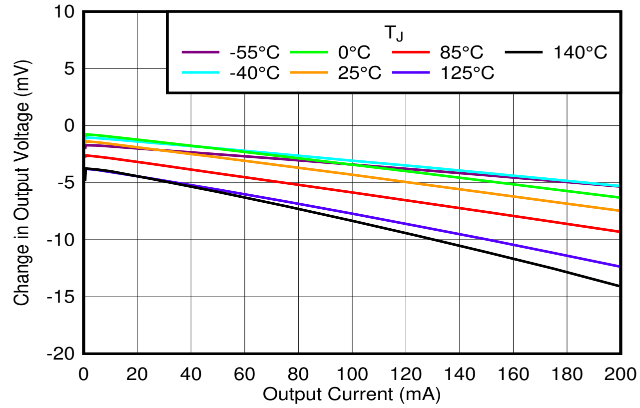
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



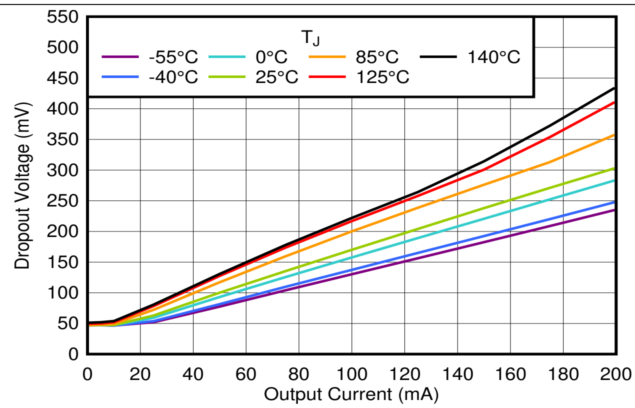
V_{OUT} = 5.0 V, I_{OUT} = 1 mA

图 31. Output Accuracy vs Temperature



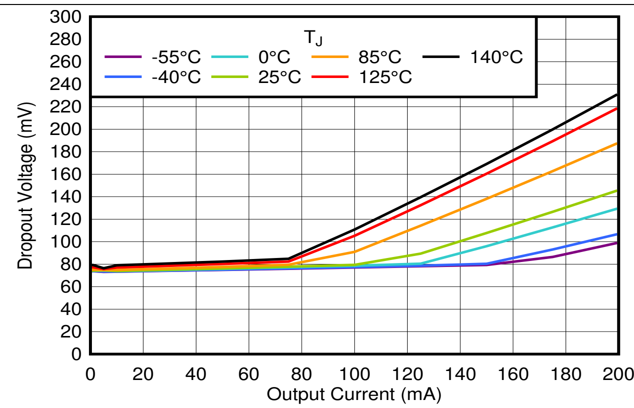
V_{OUT} = 1.8 V

图 32. Load Regulation vs V_{IN} and Temperature



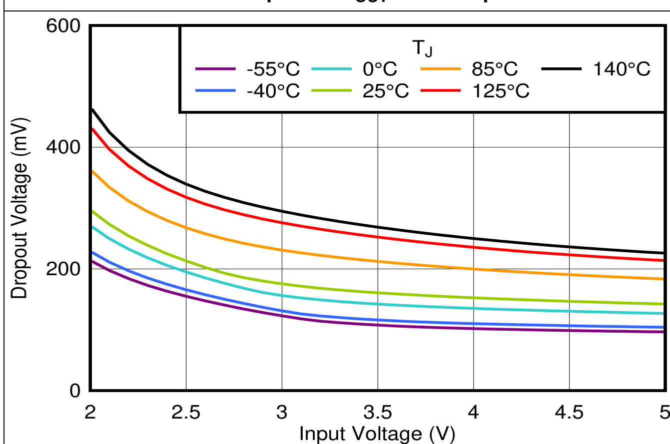
V_{OUT} = 1.8 V

图 33. Dropout vs I_{OUT} and Temperature



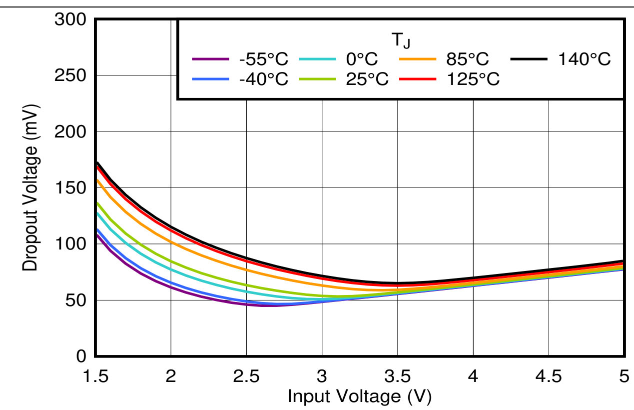
V_{OUT} = 5.0 V

图 34. Dropout vs I_{OUT} and Temperature



I_{OUT} = 200 mA

图 35. Dropout vs V_{IN} and Temperature

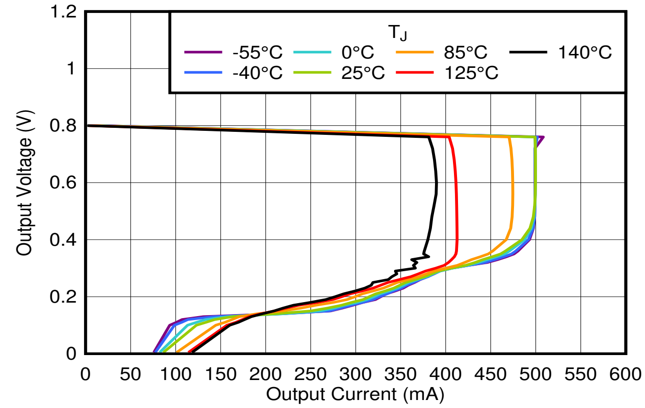


I_{OUT} = 50 mA

图 36. Dropout vs V_{IN} and Temperature

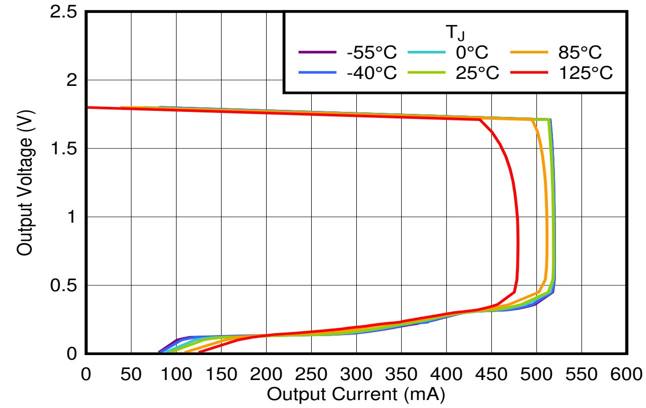
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



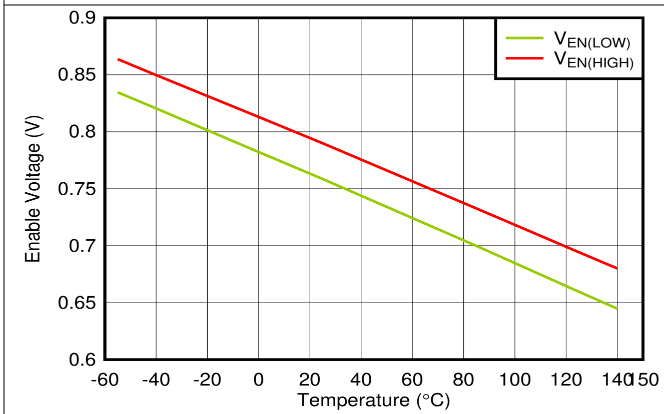
V_{OUT} = 0.8 V

图 37. Foldback Current Limit vs I_{OUT} and Temperature



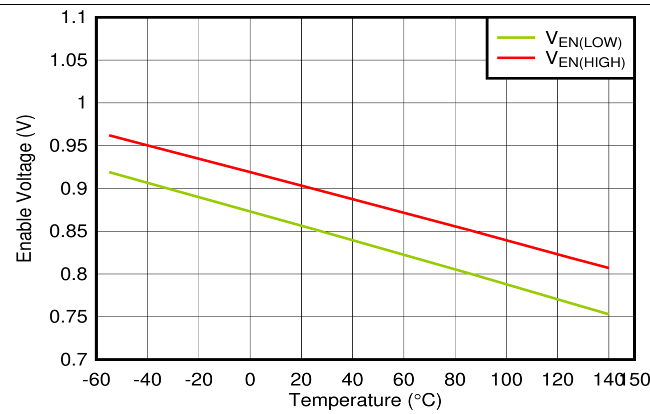
V_{OUT} = 1.8 V

图 38. Foldback Current Limit vs I_{OUT} and Temperature



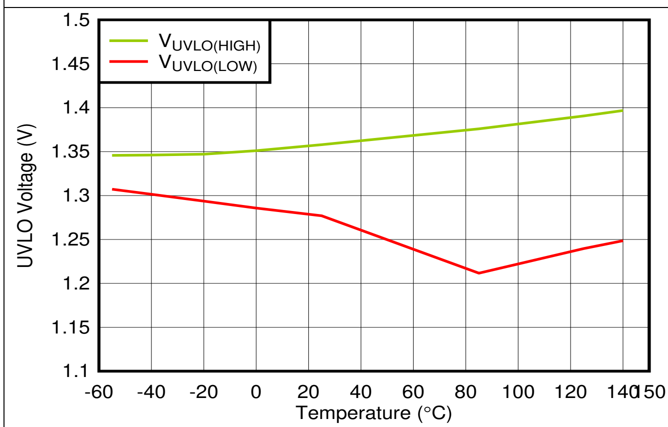
V_{OUT} = 0.8 V

图 39. EN High and Low Threshold vs Temperature



V_{OUT} = 5.0 V

图 40. EN High and Low Threshold vs Temperature



V_{OUT} = 5.0 V, I_{OUT} = 1 mA

图 41. UVLO Rising and Falling Threshold vs Temperature

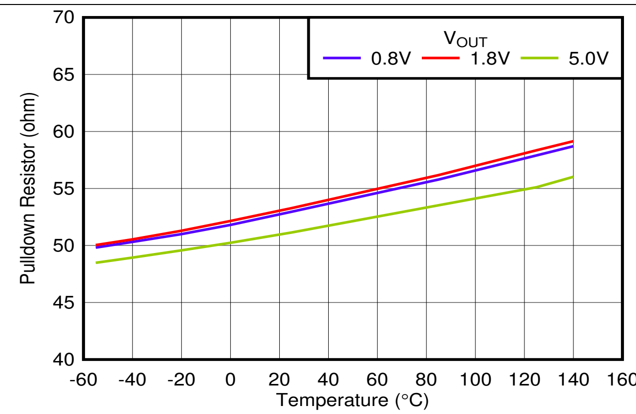


图 42. Pulldown Resistor vs Temperature and V_{OUT}

Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

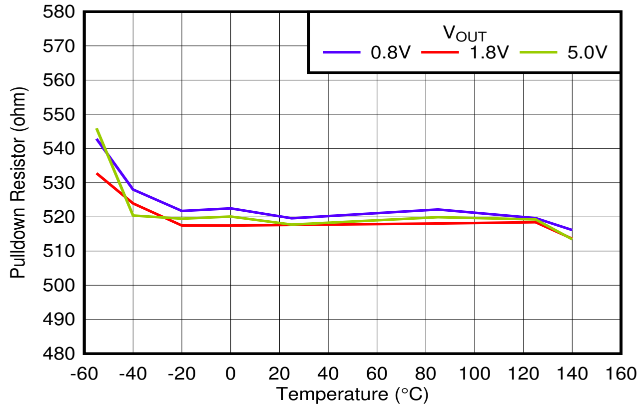
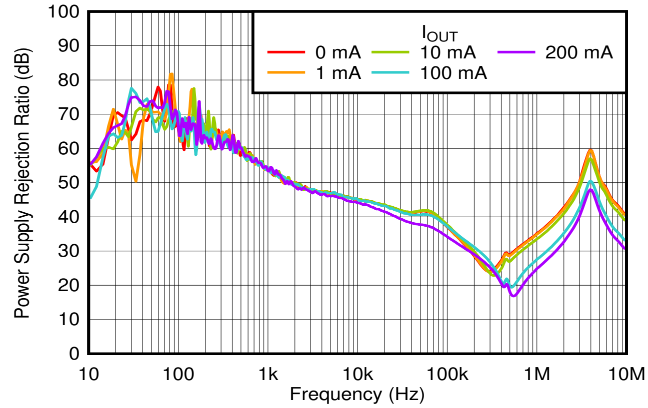
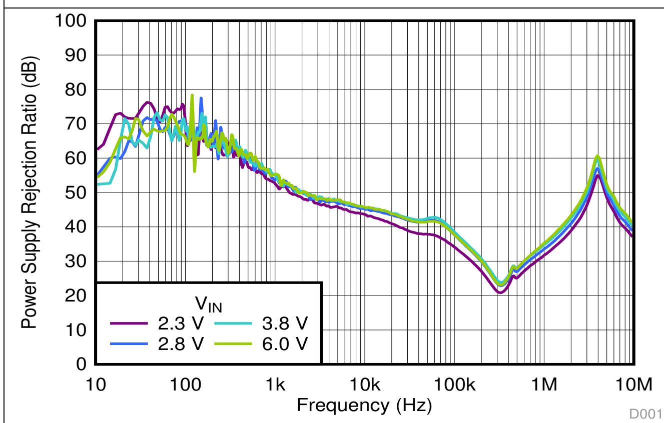


图 43. Smart Enable Pulldown Resistor vs Temperature and V_{OUT}



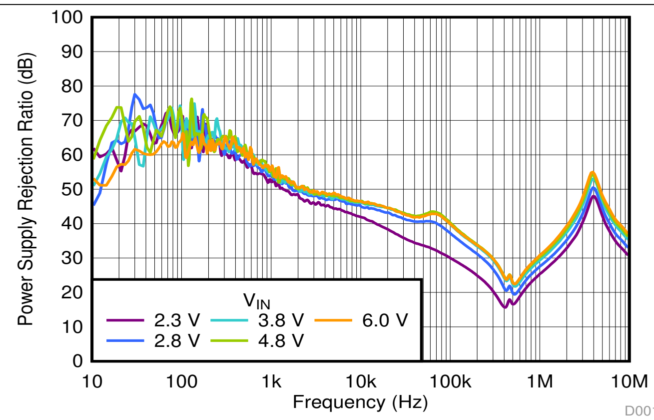
V_{IN} = 2.8 V, V_{OUT} = 1.8 V, C_{OUT} = 1 µF

图 44. PSRR vs Frequency and I_{OUT}



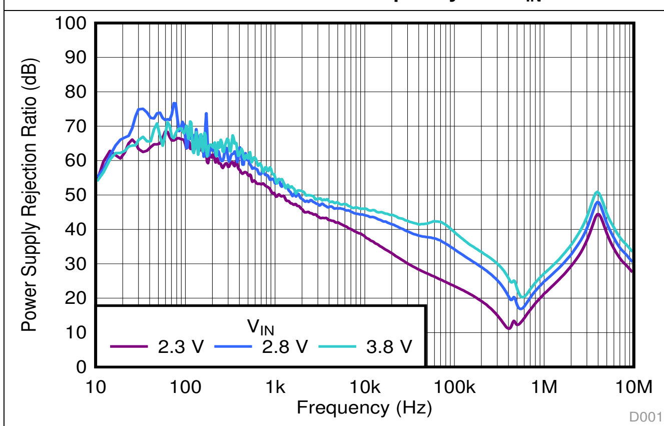
V_{OUT} = 1.8 V, I_{OUT} = 10 mA, C_{OUT} = 1 µF

图 45. PSRR vs Frequency and V_{IN}



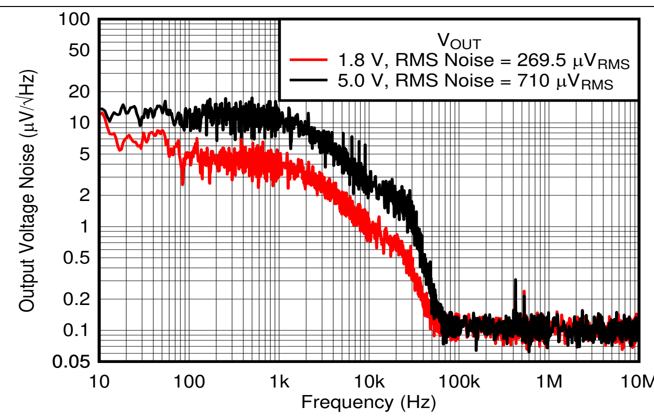
V_{OUT} = 1.8 V, I_{OUT} = 100 mA, C_{OUT} = 1 µF

图 46. PSRR vs Frequency and V_{IN}



V_{OUT} = 1.8 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF

图 47. PSRR vs Frequency and V_{IN}

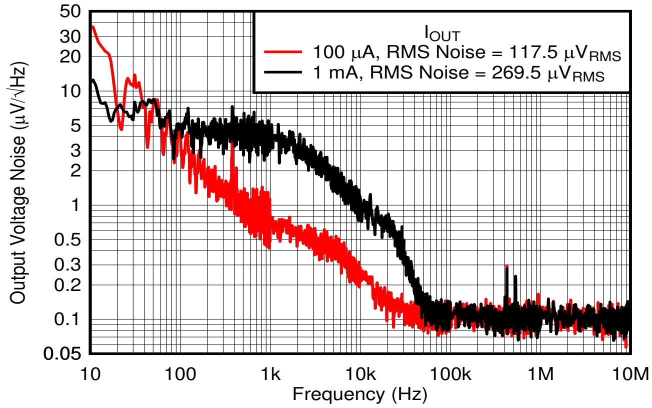


V_{IN} = V_{OUT}+ 1.0 V, I_{OUT} = 1 mA, C_{OUT} = 1 µF

图 48. Output Noise vs Frequency and V_{OUT}

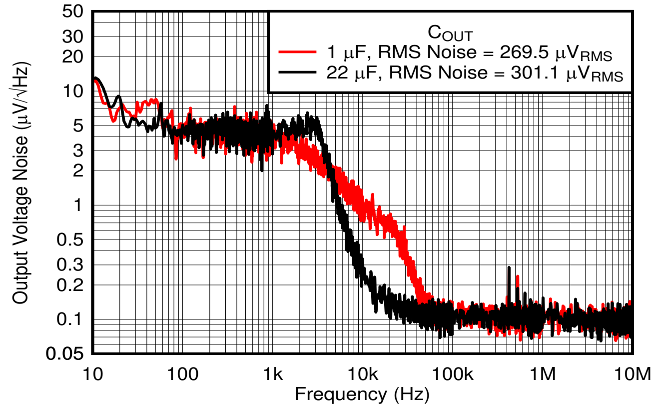
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



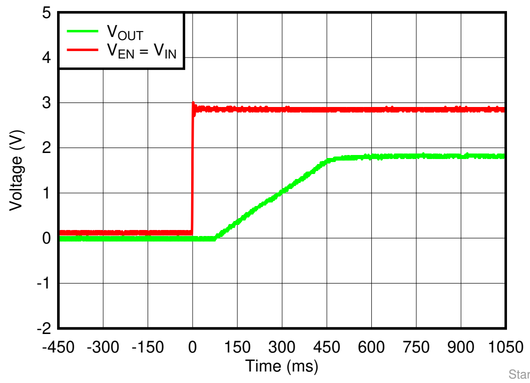
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 1 µF

图 49. Output Noise vs Frequency and I_{OUT}



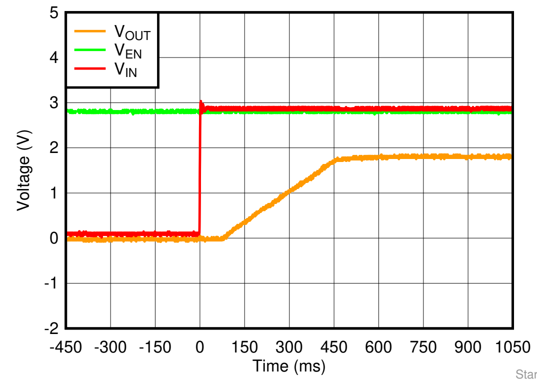
V_{OUT} = 1.8 V, V_{IN} = 2.8 V, I_{OUT} = 1 mA

图 50. Output Noise vs Frequency and C_{OUT}



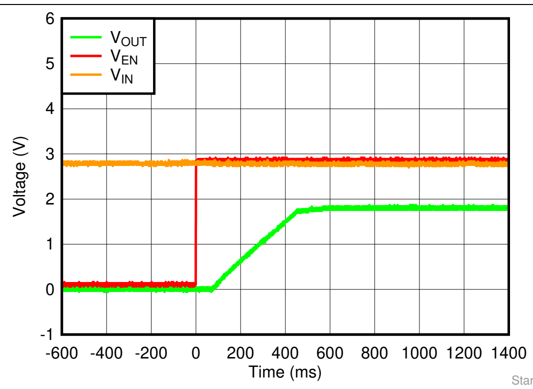
V_{OUT} = 1.8 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF

图 51. Startup With V_{EN} = V_{IN}



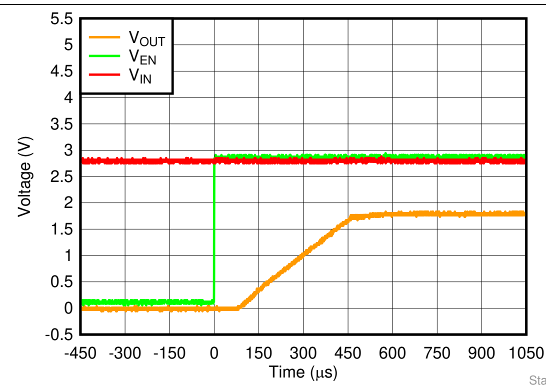
V_{OUT} = 1.8 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF

图 52. Startup With V_{EN} Before V_{IN}



V_{OUT} = 1.8 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF

图 53. Startup With V_{EN} After V_{IN}

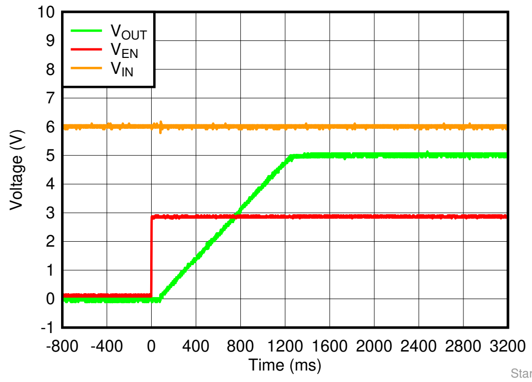


V_{OUT} = 1.8 V, I_{OUT} = 0 mA, C_{OUT} = 1 µF

图 54. Startup With V_{EN} After V_{IN}

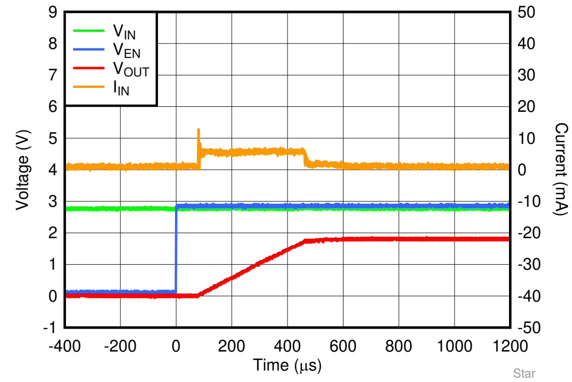
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



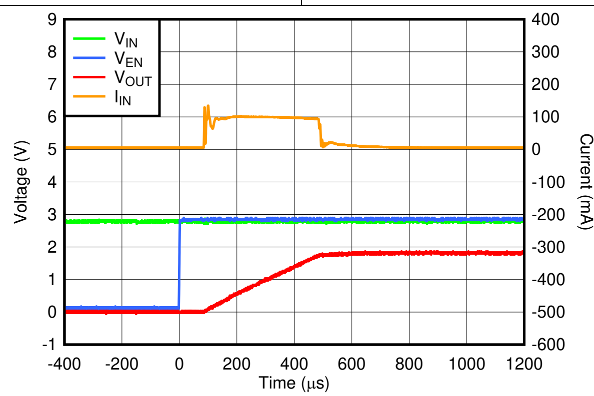
V_{OUT} = 5.0 V, I_{OUT} = 200 mA, C_{OUT} = 1 µF

图 55. Startup With V_{EN} After V_{IN}



V_{OUT} = 1.8 V, I_{OUT} = 0 mA

图 56. Startup Inrush Current With C_{OUT}= 1 µF



V_{OUT} = 1.8 V, I_{OUT} = 0 mA

图 57. Startup Inrush Current With C_{OUT}= 22 µF

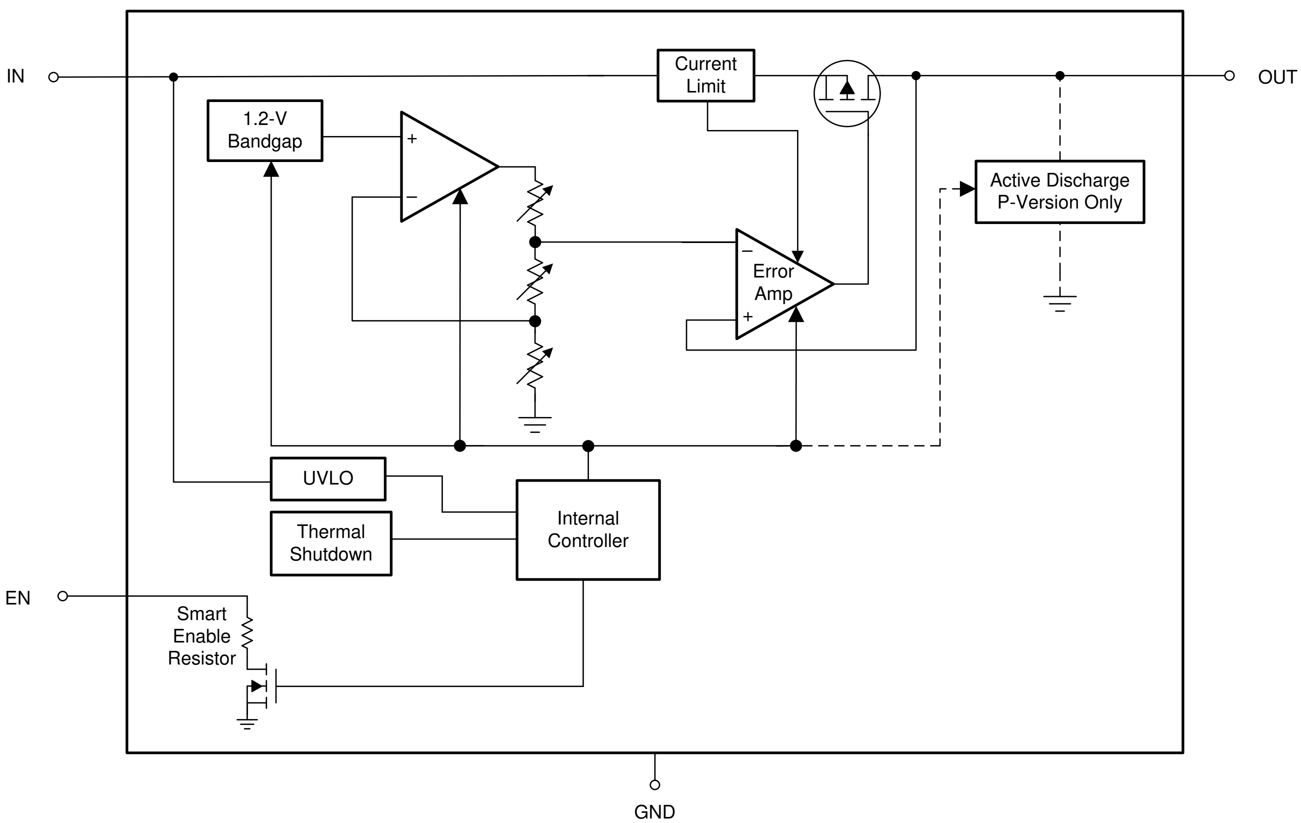
7 Detailed Description

7.1 Overview

The TPS7A03 is a ultra-low I_Q linear voltage regulator that is optimized for excellent transient performance. These characteristics make the device ideal for most battery-powered applications.

This low-dropout linear regulator (LDO) offers active discharge, foldback current limit, shutdown, and thermal protection capability.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Excellent Transient Response

The TPS7A03 includes several innovative circuits to ensure excellent transient response. Dynamic biasing increases the I_Q for a short duration during transients to extend the closed-loop bandwidth and improve the output response time to transients.

Adaptive biasing increases the I_Q as the DC load current increases, extending the bandwidth of the loop. The response time across the output voltage range is constant because a buffered reference topology is used, which keeps the control loop in unity gain at any output voltage.

These features give the device a wide loop bandwidth during transients that ensures excellent transient response while maintaining low I_Q in steady-state conditions.

7.3.2 Active Discharge (P-Version Only)

The device has an internal pulldown MOSFET that connects a $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin or by the undervoltage lockout (UVLO).

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

7.3.3 Low I_Q in Dropout

In most LDOs the I_Q significantly increases when the device is placed into dropout, which is especially true for low I_Q LDOs. The TPS7A03 helps to reduce the battery discharge by detecting when the device is operating in dropout conditions and maintaining a low I_Q.

7.3.4 Smart Enable

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

7.3.5 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

Feature Description (continued)

7.3.6 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 0.5 V.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 58 shows a diagram of the foldback current limit.

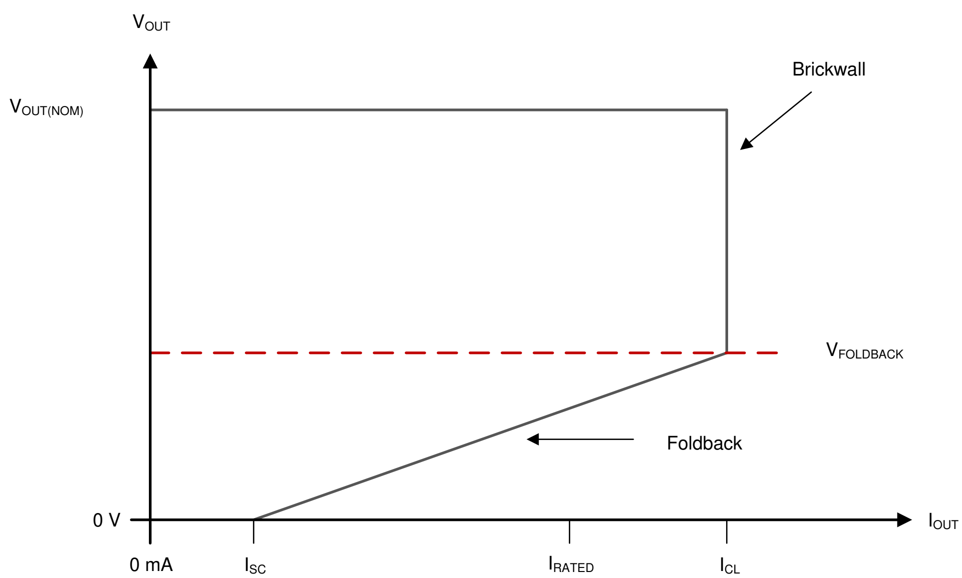


Figure 58. Foldback Current Limit

7.3.7 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.8 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

Feature Description (continued)

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in 图 59 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

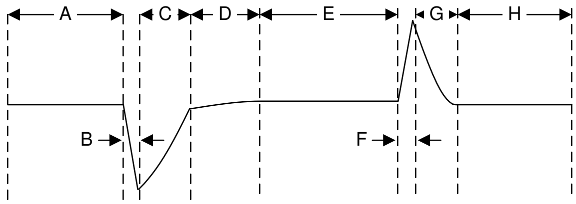


图 59. Load Transient Waveform

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

Application Information (接下页)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

8.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. 图 60 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

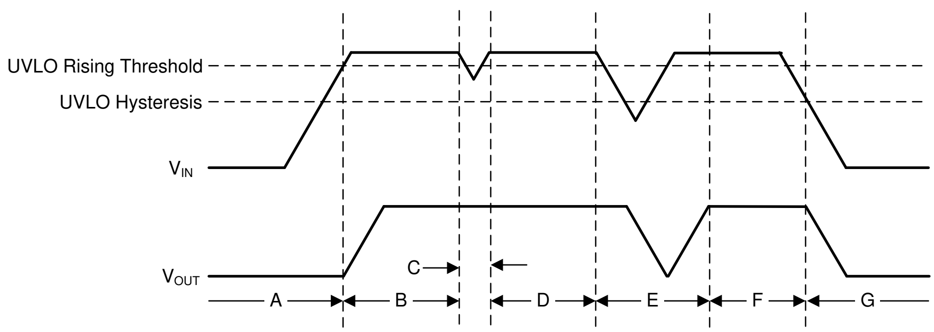


图 60. Typical UVLO Operation

8.1.5 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use 公式 2 to approximate P_D:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A03 allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

Application Information (接下页)

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to 公式 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A). 公式 4 rearranges 公式 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

8.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 公式 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in 公式 2
- T_T is the temperature at the center-top of the device package, and
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (5)

8.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in 图 61 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by 公式 4. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN} - V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

Application Information (接下页)

图 61 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Thermal Information* table.

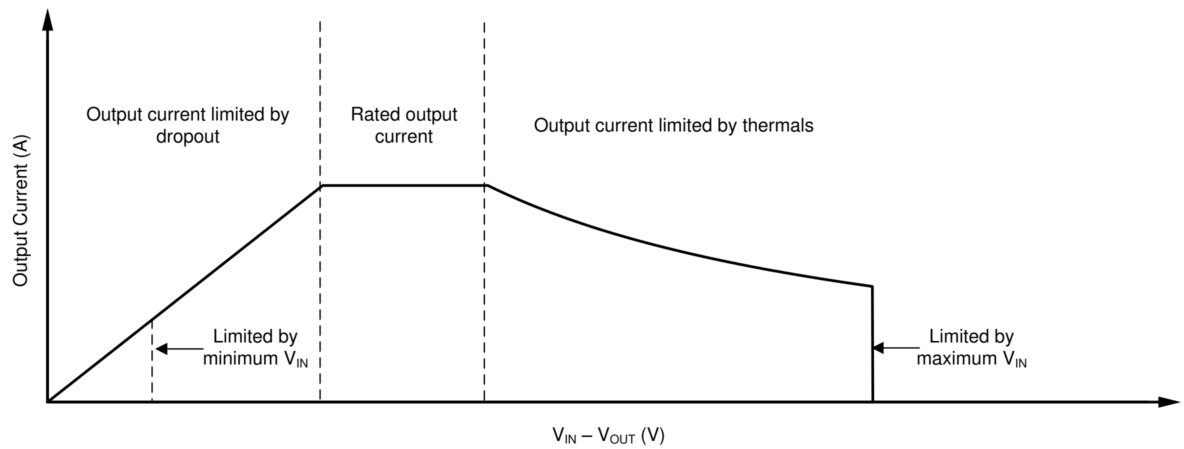


图 61. Region Description of Continuous Operation Regime

8.2 Typical Application

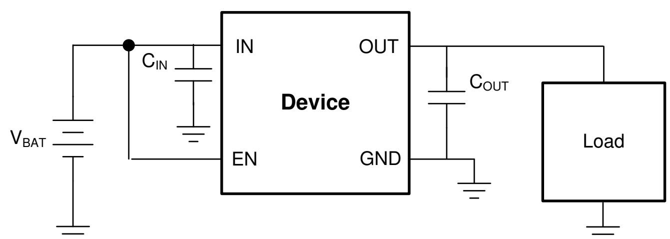


图 62. Operation From a Battery Input Supply

8.2.1 Design Requirements

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V to 3.0 V (two 1.5-V batteries)
Output voltage	1.0 V, ±1%
Input current	200 mA, maximum
Output load	10-mA DC
Maximum ambient temperature	70°C

8.2.2 Detailed Design Procedure

For this design example, the 1.0-V, fixed-version TPS7A0310 is selected. A dual AA Alkaline battery was used, thus a 1.0-µF input capacitor is recommended to minimize transient currents drawn from the battery. A 1.0-µF output capacitor is also recommended for excellent load transient response. The dropout voltage (V_{DO}) is kept within the TPS7A02 dropout voltage specification for the 1.0-V output voltage option to keep the device in regulation under all load and temperature conditions for this design. Use the recommend 1-µF input and output capacitor because the input source has a high equivalent series resistor (ESR) of 600 mΩ (typ). The very small ground current consumed by the regulator maintains a high current efficiency as compared to the load current consumed by the system, as shown in 图 63 which allows for long battery life. 公式 6 can be used to calculate the current efficiency (I_η) of this system.

$$I_\eta(\%) = I_{OUT} / (I_{OUT} + I_Q) \times 100 \quad (6)$$

8.2.3 Application Curve

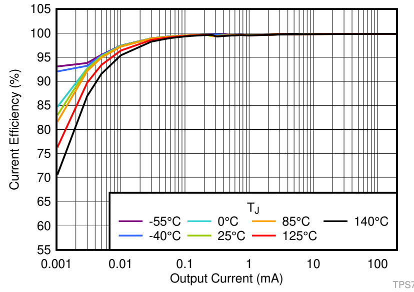


图 63. Current Efficiency vs I_{OUT} and Temperature

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.5 V to 6.0 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.5 V. TI highly recommends using a 1-µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

10.2 Layout Examples

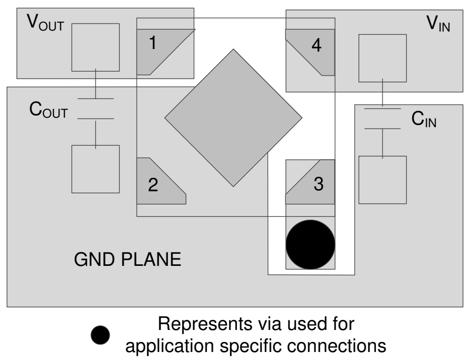


图 64. Layout Example for the DQN Package

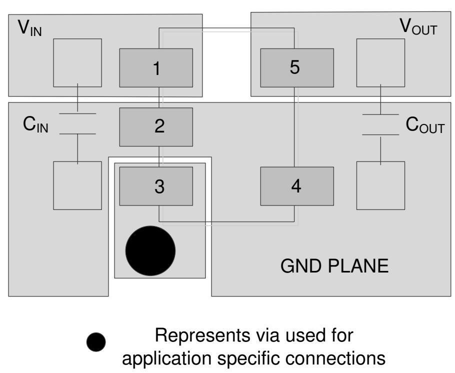


图 65. Layout Example for the DBV Package

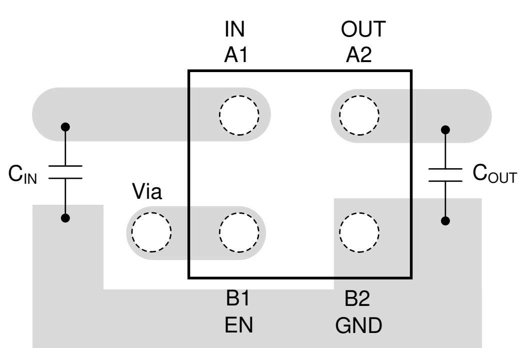


图 66. Layout Example for the YCH Package

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

表 **3.** 器件命名规则 (1)(2)

产品	V_{OUT}
TPS7A03**xx(x)Pyyyz**	**XX(X)** 是标称输出电压。对于分辨率为 100mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，28 = 2.8V；125 = 1.25V）。 **P** 表示有源输出放电功能。TPS7A03 系列的所有产品在器件处于禁用状态时都可以对输出进行主动放电。 **YYY** 为封装标识符。 **Z** 为封装数量。R 表示卷（3000 片），T 表示带（250 片）。

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问器件产品文件夹（www.ti.com.cn）。
(2) 可提供 1.0V 至 3.3V 范围内的输出电压（以 50mV 为单位增量）。更多详细信息及可用性，请联系制造商。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

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11.4 商标

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11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A0309PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2FFT	Samples
TPS7A0310PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GO	Samples
TPS7A0312PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21QF	Samples
TPS7A0312PYCHR	ACTIVE	DSBGA	YCH	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	H	Samples
TPS7A0313PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2FGT	Samples
TPS7A0315PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21UF	Samples
TPS7A0315PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GM	Samples
TPS7A03185PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HP	Samples
TPS7A0318DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2CET	Samples
TPS7A0318PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21VF	Samples
TPS7A0318PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	G3	Samples
TPS7A0318PYCHR	ACTIVE	DSBGA	YCH	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	J	Samples
TPS7A0320PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	22NT	Samples
TPS7A0320PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GK	Samples
TPS7A0321PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2FHT	Samples
TPS7A0322DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IO	Samples
TPS7A0322PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21RF	Samples
TPS7A0322PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GP	Samples
TPS7A0323PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21SF	Samples
TPS7A0323PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A0325DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K9	Samples
TPS7A0325DQNR3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	K9	Samples
TPS7A0325PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21NF	Samples
TPS7A0325PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GN	Samples
TPS7A0325PDQNR3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GN	Samples
TPS7A0325PYCHR	ACTIVE	DSBGA	YCH	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	K	Samples
TPS7A0328DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	29RT	Samples
TPS7A0328DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IG	Samples
TPS7A0328PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21OF	Samples
TPS7A0328PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GL	Samples
TPS7A0328PYCHR	ACTIVE	DSBGA	YCH	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L	Samples
TPS7A0330PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21WF	Samples
TPS7A0330PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	G4	Samples
TPS7A0330PYCHR	ACTIVE	DSBGA	YCH	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	N	Samples
TPS7A0331PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21XF	Samples
TPS7A0331PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GR	Samples
TPS7A0333DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	29ST	Samples
TPS7A0333DQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	IH	Samples
TPS7A0333PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21PF	Samples
TPS7A0333PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	G5	Samples
TPS7A0333PDQNR3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	G5	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A0333PYCHR	ACTIVE	DSBGA	YCH	4	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	Q	Samples
TPS7A0336PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	21TF	Samples
TPS7A0350PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2FIT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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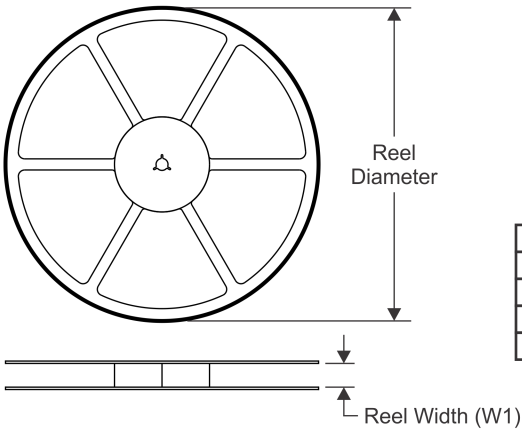
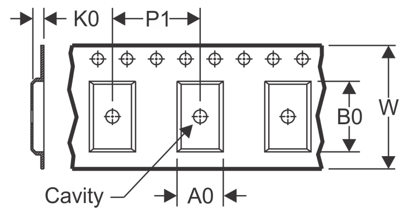
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

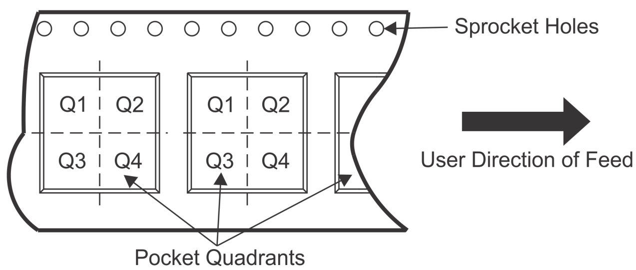


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

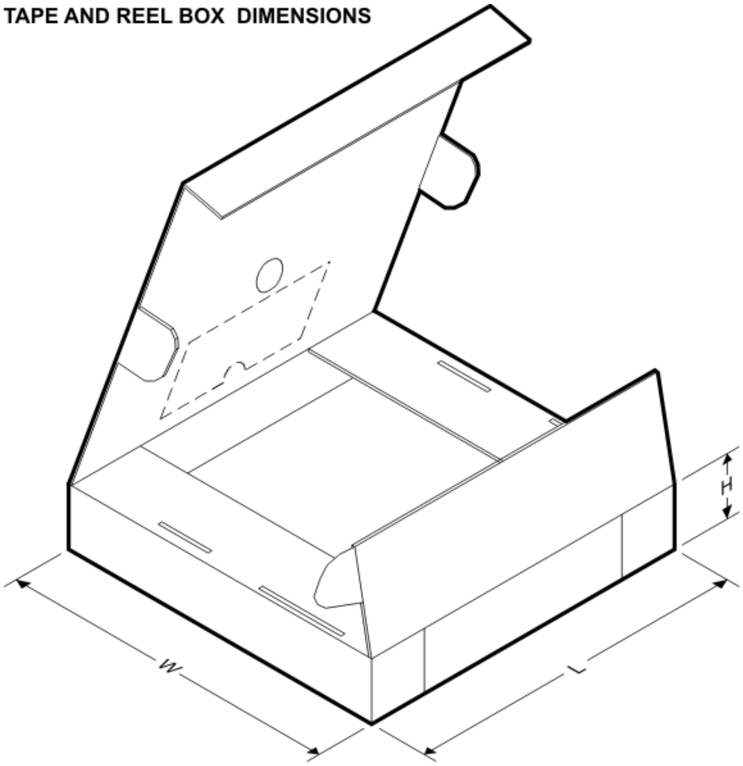


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A0309PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0310PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0310PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0312PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0312PYCHR	DSBGA	YCH	4	12000	180.0	8.4	0.72	0.72	0.42	2.0	8.0	Q1
TPS7A0313PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0315PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0315PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0315PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A03185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A03185PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0318DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0318PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0318PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0318PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0318PYCHR	DSBGA	YCH	4	12000	180.0	8.4	0.72	0.72	0.42	2.0	8.0	Q1
TPS7A0320PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0320PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A0320PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0321PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0322DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0322PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0322PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0322PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0323PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0323PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0323PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0325DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0325DQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
TPS7A0325PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0325PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0325PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0325PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
TPS7A0325PYCHR	DSBGA	YCH	4	12000	180.0	8.4	0.72	0.72	0.42	2.0	8.0	Q1
TPS7A0328DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0328DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0328PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0328PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0328PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0328PYCHR	DSBGA	YCH	4	12000	180.0	8.4	0.72	0.72	0.42	2.0	8.0	Q1
TPS7A0330PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0330PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0330PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0330PYCHR	DSBGA	YCH	4	12000	180.0	8.4	0.72	0.72	0.42	2.0	8.0	Q1
TPS7A0331PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0331PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0331PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0331PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0333DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0333DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0333PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0333PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7A0333PDQNR	X2SON	DQN	4	3000	178.0	8.4	1.13	1.13	0.53	4.0	8.0	Q2
TPS7A0333PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TPS7A0333PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
TPS7A0333PYCHR	DSBGA	YCH	4	12000	180.0	8.4	0.72	0.72	0.42	2.0	8.0	Q1
TPS7A0336PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7A0350PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

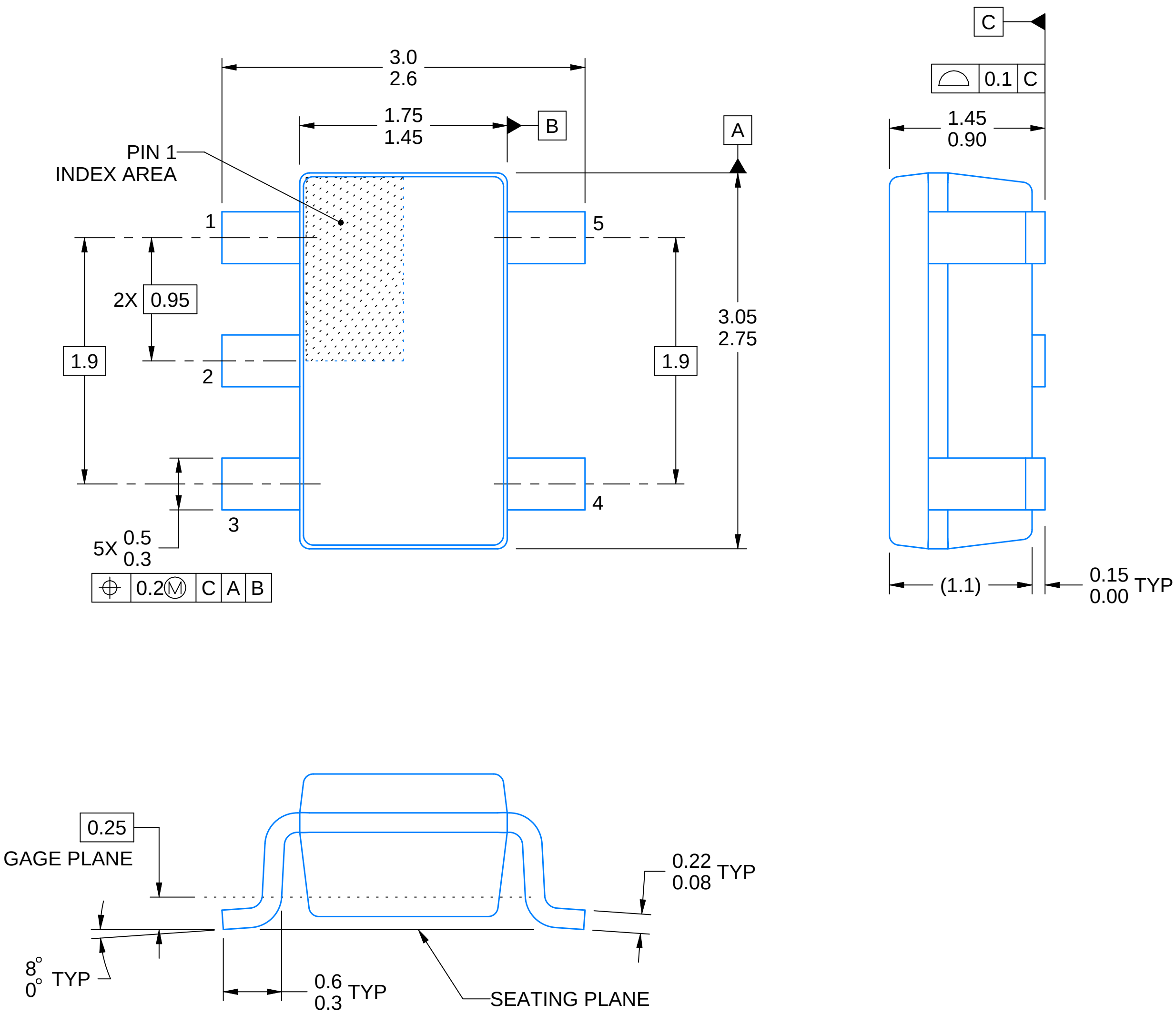
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A0309PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0310PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0310PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0312PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0312PYCHR	DSBGA	YCH	4	12000	182.0	182.0	20.0
TPS7A0313PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0315PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0315PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0315PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A03185PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A03185PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0318DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0318PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0318PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0318PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0318PYCHR	DSBGA	YCH	4	12000	182.0	182.0	20.0
TPS7A0320PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0320PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0320PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0321PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A0322DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0322PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0322PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0322PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0323PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0323PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0323PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0325DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0325DQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0325PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0325PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0325PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0325PDQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0325PYCHR	DSBGA	YCH	4	12000	182.0	182.0	20.0
TPS7A0328DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0328DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0328PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0328PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0328PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0328PYCHR	DSBGA	YCH	4	12000	182.0	182.0	20.0
TPS7A0330PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0330PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0330PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0330PYCHR	DSBGA	YCH	4	12000	182.0	182.0	20.0
TPS7A0331PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0331PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0331PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0331PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0333DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0333DQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0333PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0333PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS7A0333PDQNR	X2SON	DQN	4	3000	205.0	200.0	33.0
TPS7A0333PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0333PDQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TPS7A0333PYCHR	DSBGA	YCH	4	12000	182.0	182.0	20.0
TPS7A0336PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7A0350PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0



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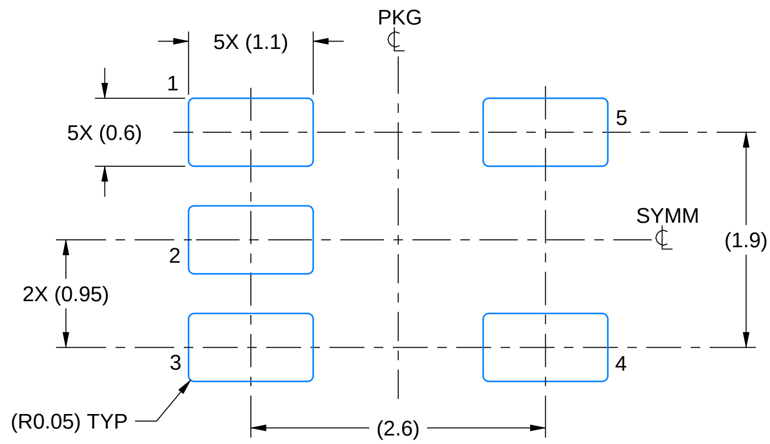
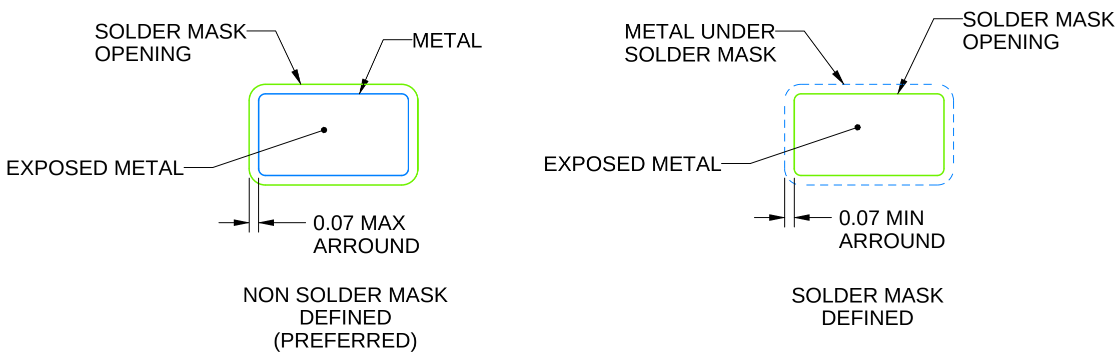
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



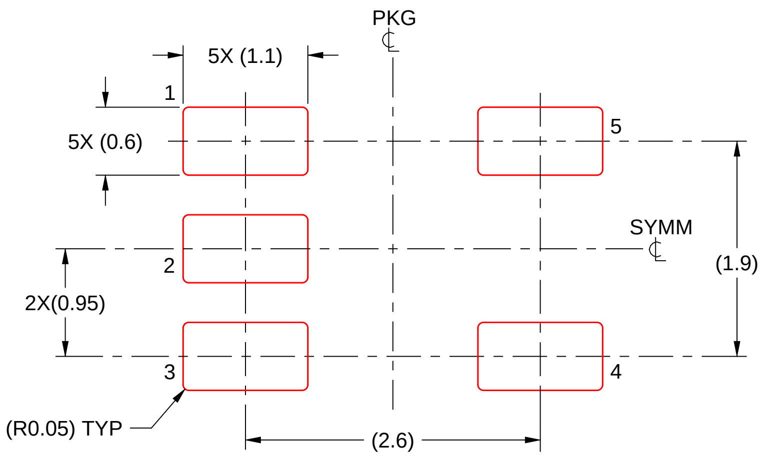
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



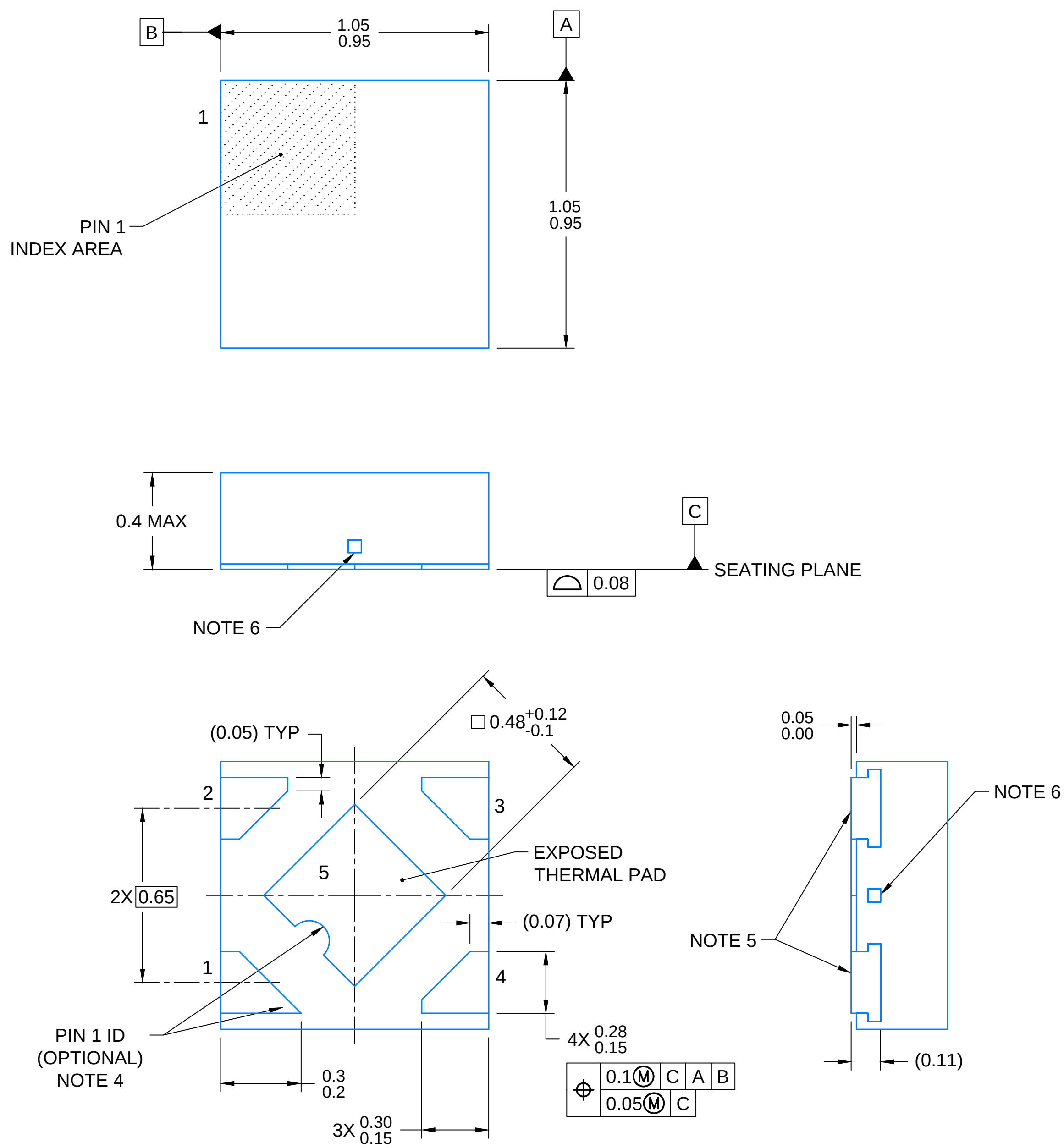
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

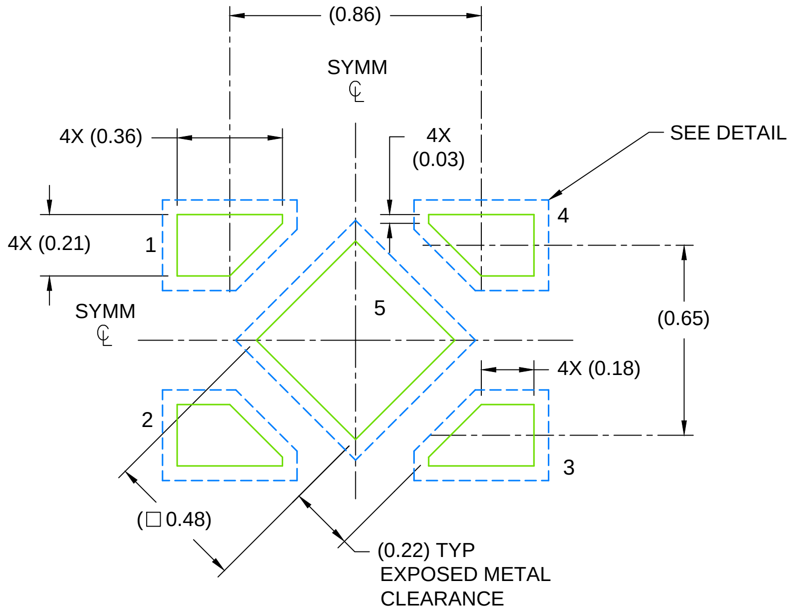
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



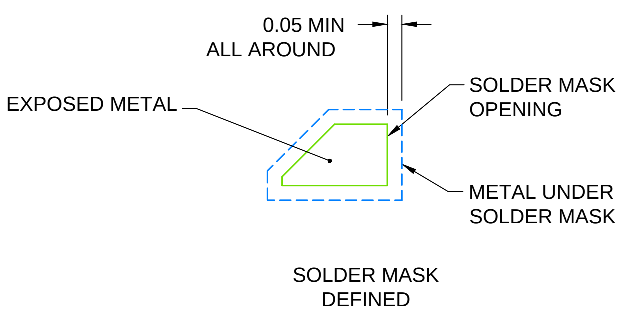
4215302/E 12/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X

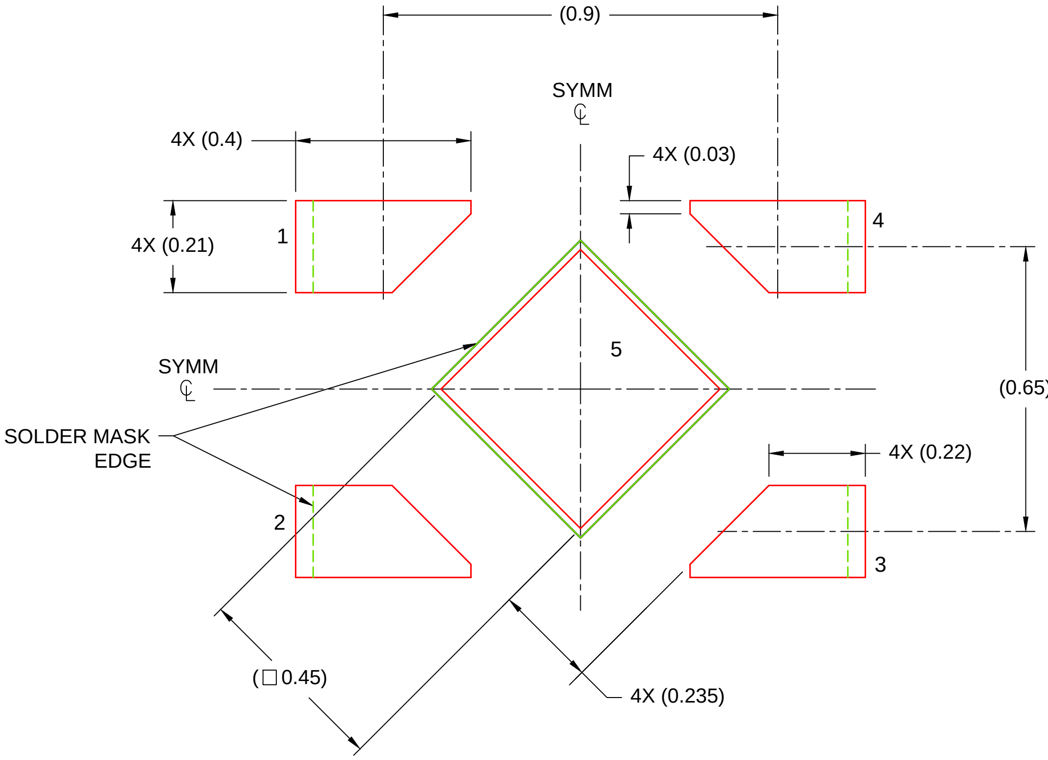


SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

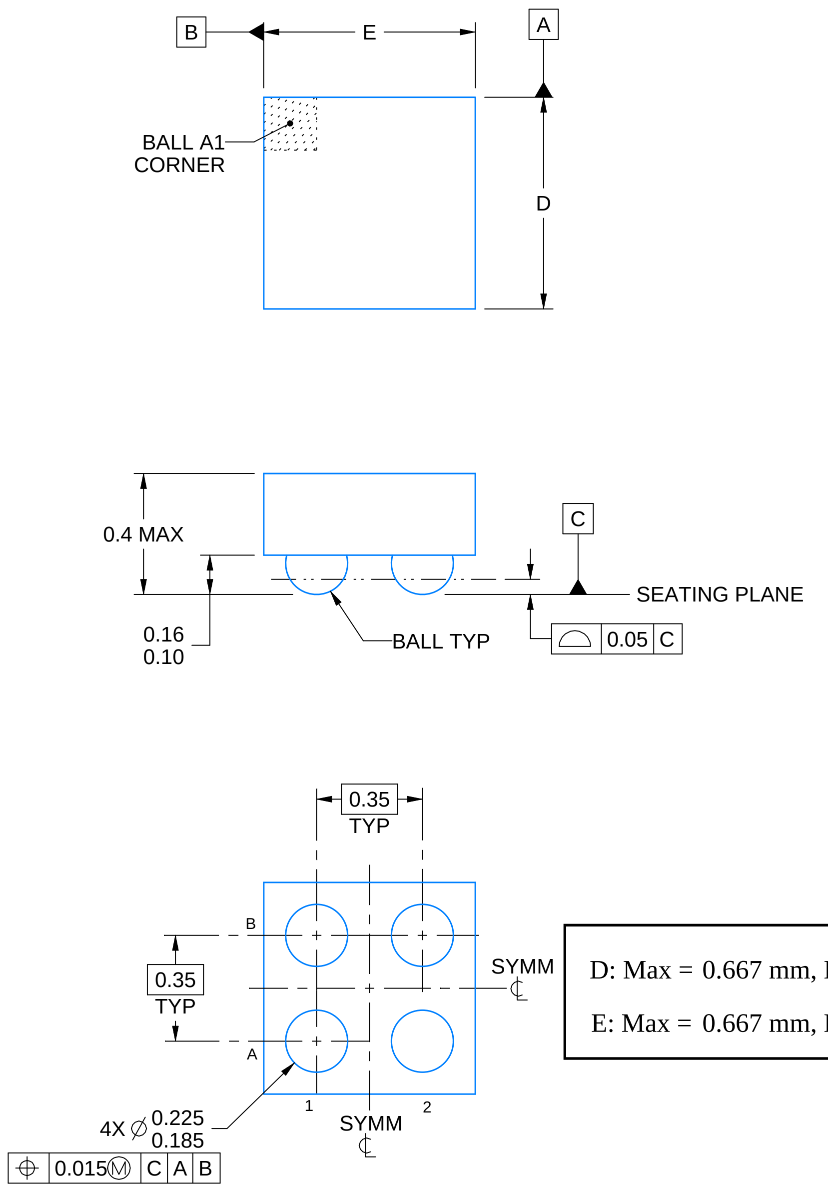
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YCH0004

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



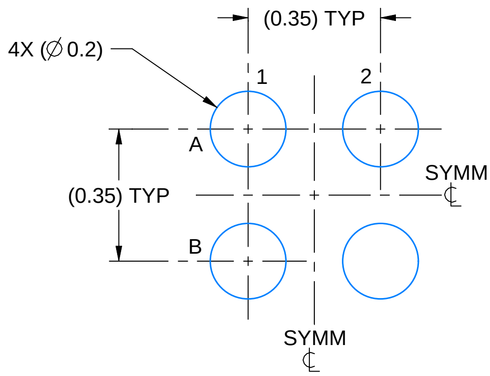
D: Max = 0.667 mm, Min =0.607 mm

E: Max = 0.667 mm, Min =0.607 mm

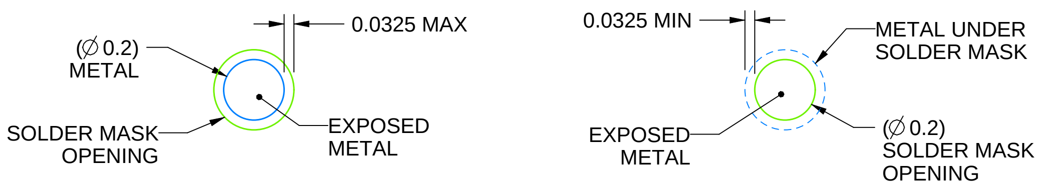
4224061/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



NON-SOLDER MASK DEFINED

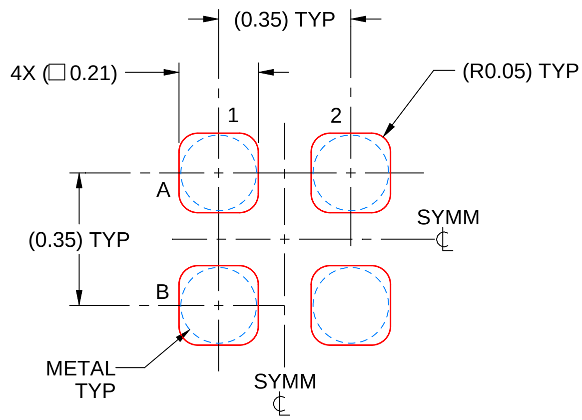
SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DETAILS
NOT TO SCALE

4224061/A 12/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4224061/A 12/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.