High Voltage Latch-Up Proof, Quad SPST Switches

ADG5412/ADG5413

FEATURES

Latch-up proof
8 kV human body model (HBM) ESD rating
Low on resistance (<10 Ω)
±9 V to ±22 V dual-supply operation
9 V to 40 V single-supply operation
48 V supply maximum ratings
Fully specified at ±15 V, ±20 V, +12 V, and +36 V
V_{SS} to V_{DD} analog signal range

APPLICATIONS

Relay replacement
Automatic test equipment
Data acquisition
Instrumentation
Avionics
Audio and video switching
Communication systems

FUNCTIONAL BLOCK DIAGRAMS

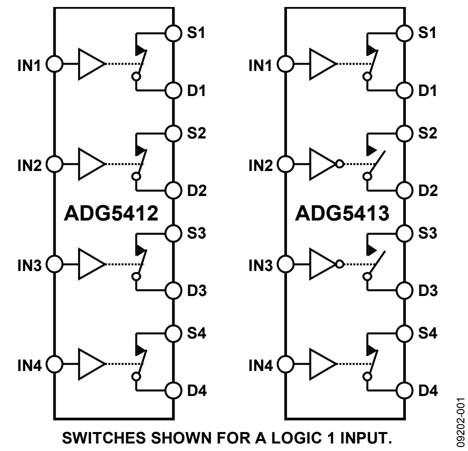

Figure 1.

GENERAL DESCRIPTION

The ADG5412/ADG5413 contain four independent single-pole/single-throw (SPST) switches. The ADG5412 switches turn on with Logic 1. The ADG5413 has two switches with digital control logic similar to that of the ADG5412; however, the logic is inverted on the other two switches. Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The ADG5412 and ADG5413 do not have a V_L pin. The digital inputs are compatible with 3 V logic inputs over the full operating supply range.

The on-resistance profile is very flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals. High switching speed also makes the devices suitable for video signal switching. The ADG5413 exhibits break-before-make switching action for use in multiplexer applications.

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON}.
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG5412/ADG5413 can be operated from dual supplies up to ±22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG5412/ADG5413 can be operated from a single rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: V_{INH} = 2.0 V, V_{INL} = 0.8 V.
6. No V_L logic power supply required.

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7/2010—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	9.8			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 24
	11	14	16	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.7	0.9	1.1	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	1.2			Ω typ	V_S = ±10 V, I_S = −10 mA
	1.6	2	2.2	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓ 10 V; see Figure 27
	±0.25	±0.75	±6	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓ 10 V; see Figure 27
	±0.25	±0.75	±6	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±10 V; see Figure 23
	±0.4	±2	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	2.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	202	236	262	ns max	V_S = 10 V; see Figure 31
t_{OFF}	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	145	170	182	ns max	V_S = 10 V; see Figure 31
Break-Before-Make Time Delay, t_D (ADG5413 Only)	15			ns typ	R_L = 300 Ω, C_L = 35 pF
			6	ns min	V_{S1} = V_{S2} = 10 V; see Figure 30
Charge Injection, Q_{INJ}	240			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 25
Total Harmonic Distortion + Noise	0.009			% typ	R_L = 1 kΩ, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 28
−3 dB Bandwidth	167			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 29
Insertion Loss	−0.7			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
C_S (Off)	18			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	18			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	60			pF typ	V_S = 0 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45			µA typ	Digital inputs = 0 V or V_{DD}
	55		70	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	9			Ω typ	V_S = ±15 V, I_S = −10 mA; see Figure 24
	10	13	15	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	V_S = ±15 V, I_S = −10 mA
	0.7	0.9	1.1	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	1.5			Ω typ	V_S = ±15 V, I_S = −10 mA
	1.8	2.2	2.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓ 15 V; see Figure 27
	±0.25	±0.75	±6	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓ 15 V; see Figure 27
	±0.25	±0.75	±6	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±15 V; see Figure 23
	±0.4	±2	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	2.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	158			ns typ	R_L = 300 Ω, C_L = 35 pF
	187	217	240	ns max	V_S = 10 V; see Figure 31
t_{OFF}	110			ns typ	R_L = 300 Ω, C_L = 35 pF
	138	154	170	ns max	V_S = 10 V; see Figure 31
Break-Before-Make Time Delay, t_D (ADG5413 Only)	12			ns typ	R_L = 300 Ω, C_L = 35 pF
			5	ns min	V_{S1} = V_{S2} = 10 V; see Figure 30
Charge Injection, Q_{INJ}	310			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 25

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Total Harmonic Distortion + Noise	0.007			% typ	R_L = 1 kΩ, 20 V p-p, f = 20 Hz to 20 kHz; see Figure 28
−3 dB Bandwidth	160			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 29
Insertion Loss	−0.6			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
C_S (Off)	17			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	17			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	60			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50			µA typ	Digital inputs = 0 V or V_{DD}
	70		110	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	19			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 24
	22	27	31	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.8	1	1.2	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	4.4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	5.5	6.5	7.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 27
	±0.25	±0.75	±6	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 27
	±0.25	±0.75	±6	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V/10 V; see Figure 23
	±0.4	±2	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	2.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	225			ns typ	R_L = 300 Ω, C_L = 35 pF
	296	358	403	ns max	V_S = 8 V; see Figure 31
t_{OFF}	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	187	222	247	ns max	V_S = 8 V; see Figure 31

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Break-Before-Make Time Delay, t_D (ADG5413 Only)	70			ns typ	R_L = 300 Ω, C_L = 35 pF
			38	ns min	V_{S1} = V_{S2} = 8 V; see Figure 30
Charge Injection, Q_{INJ}	95			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 25
Total Harmonic Distortion + Noise	0.07			% typ	R_L = 1 kΩ, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 28
−3 dB Bandwidth	180			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 29
Insertion Loss	−1.3			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
C_S (Off)	22			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	22			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	58			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	40			μA typ	Digital inputs = 0 V or V_{DD}
			65	μA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	10.6			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA; see Figure 24
	12	15	17	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	0.7	0.9	1.1	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	2.7			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	3.2	3.8	4.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 27
	±0.25	±0.75	±6	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 27
	±0.25	±0.75	±6	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V/30 V; see Figure 23
	±0.4	±2	±12	nA max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			µA typ	$V_{IN} = V_{GND}$ or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	2.5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	180			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	220	230	248	ns max	$V_S = 18$ V; see Figure 31
t_{OFF}	130			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	169	167	174	ns max	$V_S = 18$ V; see Figure 31
Break-Before-Make Time Delay, t_D (ADG5413 Only)	25			ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
			8	ns min	$V_{S1} = V_{S2} = 18$ V; see Figure 30
Charge Injection, Q_{INJ}	280			pC typ	$V_S = 18$ V, $R_S = 0\ \Omega$, $C_L = 1$ nF; see Figure 32
Off Isolation	−78			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−70			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; Figure 25
Total Harmonic Distortion + Noise	0.03			% typ	$R_L = 1$ kΩ, 18 V p-p, f = 20 Hz to 20 kHz; see Figure 28
−3 dB Bandwidth	174			MHz typ	$R_L = 50\ \Omega$, $C_L = 5$ pF; see Figure 29
Insertion Loss	−0.8			dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 29
C_S (Off)	18			pF typ	$V_S = 18$ V, f = 1 MHz
C_D (Off)	18			pF typ	$V_S = 18$ V, f = 1 MHz
C_D (On), C_S (On)	58			pF typ	$V_S = 18$ V, f = 1 MHz
POWER REQUIREMENTS					$V_{DD} = 39.6$ V
I_{DD}	80			µA typ	Digital inputs = 0 V or V_{DD}
	100		130	µA max	
V_{DD}			9/40	V min/V max	GND = 0 V, $V_{SS} = 0$ V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
$V_{DD} = +15$ V, $V_{SS} = −15$ V				
TSSOP ($\theta_{JA} = 112.6$°C/W)	89	59	37	mA maximum
LFCSP ($\theta_{JA} = 30.4$°C/W)	160	94	49	mA maximum
$V_{DD} = +20$ V, $V_{SS} = −20$ V				
TSSOP ($\theta_{JA} = 112.6$°C/W)	95	63	39	mA maximum
LFCSP ($\theta_{JA} = 30.4$°C/W)	170	98	50	mA maximum
$V_{DD} = 12$ V, $V_{SS} = 0$ V				
TSSOP ($\theta_{JA} = 112.6$°C/W)	61	43	29	mA maximum
LFCSP ($\theta_{JA} = 30.4$°C/W)	110	70	42	mA maximum
$V_{DD} = 36$ V, $V_{SS} = 0$ V				
TSSOP ($\theta_{JA} = 112.6$°C/W)	80	54	35	mA maximum
LFCSP ($\theta_{JA} = 30.4$°C/W)	144	87	47	mA maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	278 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
16-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

[1] Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

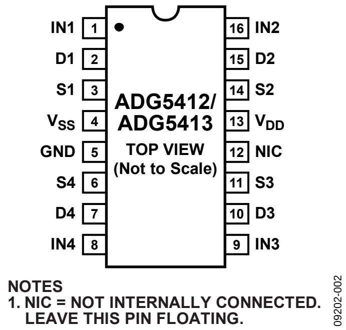

Figure 2. TSSOP Pin Configuration

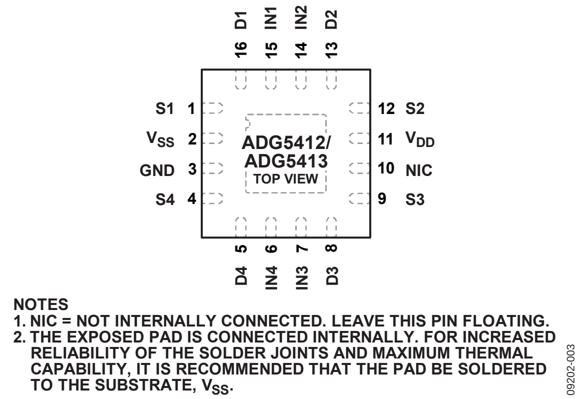

Figure 3. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	IN1	Logic Control Input 1.
2	16	D1	Drain Terminal 1. This pin can be an input or output.
3	1	S1	Source Terminal 1. This pin can be an input or output.
4	2	V_{SS}	Most Negative Power Supply Potential.
5	3	GND	Ground (0 V) Reference.
6	4	S4	Source Terminal 4. This pin can be an input or output.
7	5	D4	Drain Terminal 4. This pin can be an input or output.
8	6	IN4	Logic Control Input 4.
9	7	IN3	Logic Control Input 3.
10	8	D3	Drain Terminal 3. This pin can be an input or output.
11	9	S3	Source Terminal 3. This pin can be an input or output.
12	10	NIC	Not Internally Connected. Leave this pin floating.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	S2	Source Terminal 2. This pin can be an input or output.
15	13	D2	Drain Terminal 2. This pin can be an input or output.
16	14	IN2	Logic Control Input 2.
	EP	Exposed Pad	The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 8. ADG5412 Truth Table

INx	Switch Condition
1	On
0	Off

Table 9. ADG5413 Truth Table

INx	S1, S4	S2, S3
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

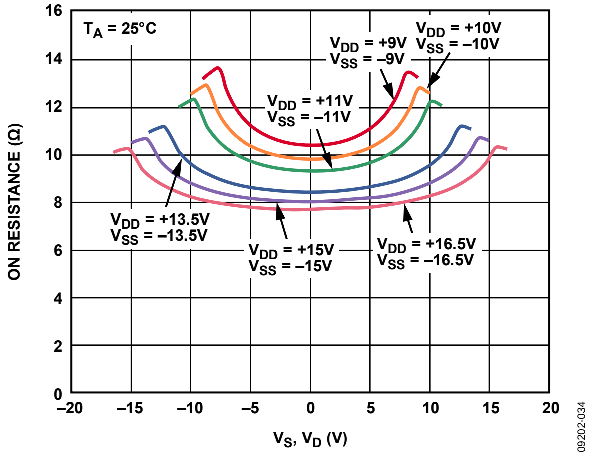

Figure 4. R_{ON} as a Function of V_S, V_D (Dual Supply)

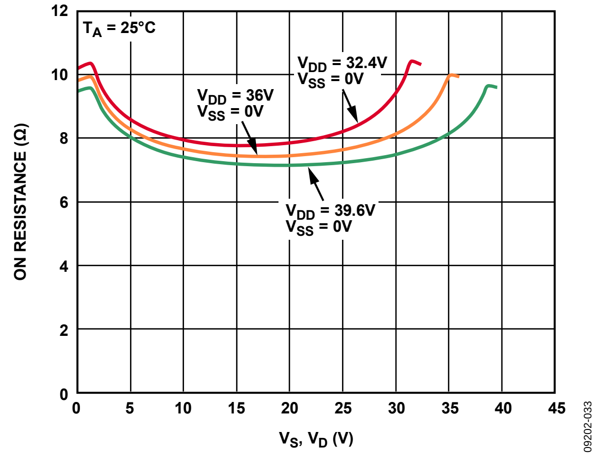

Figure 7. R_{ON} as a Function of V_S, V_D (Single Supply)

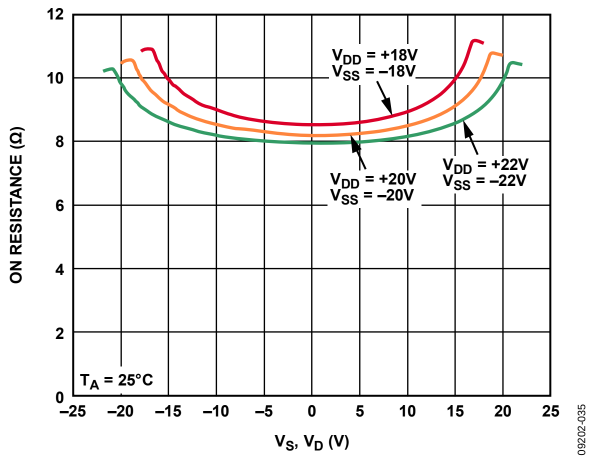

Figure 5. R_{ON} as a Function of V_S, V_D (Dual Supply)

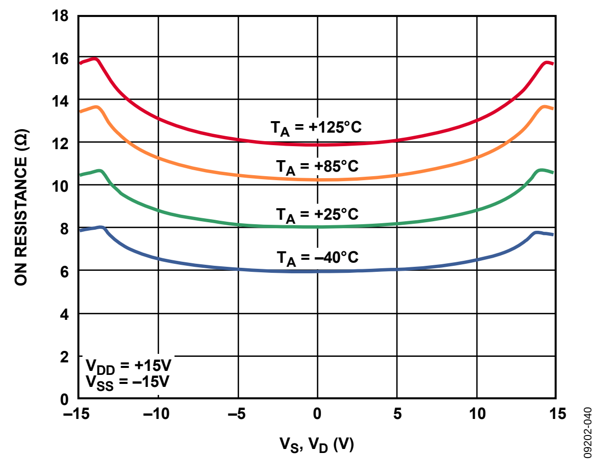

Figure 8. R_{ON} as a Function of V_S (V_D) for Different Temperatures, ±15 V Dual Supply

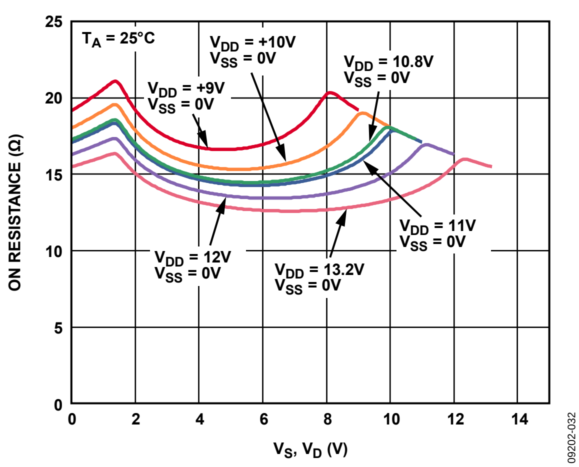

Figure 6. R_{ON} as a Function of V_S, V_D (Single Supply)

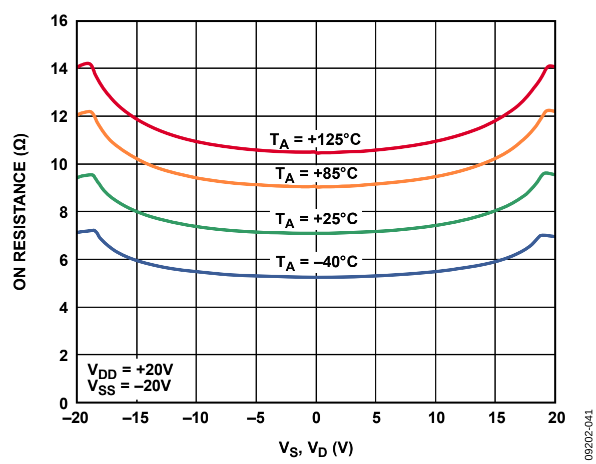

Figure 9. R_{ON} as a Function of V_S (V_D) for Different Temperatures, ±20 V Dual Supply

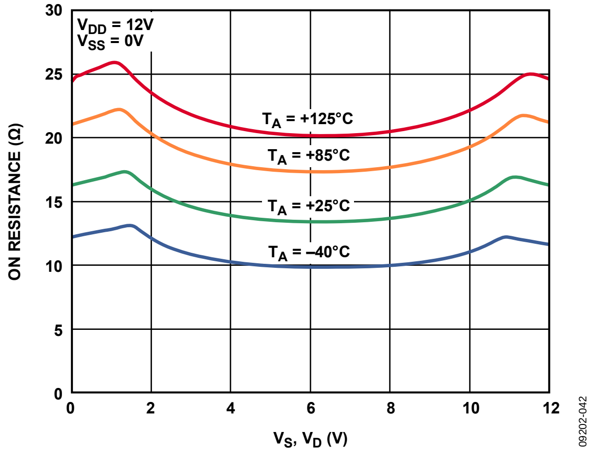

Figure 10. R_{ON} as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

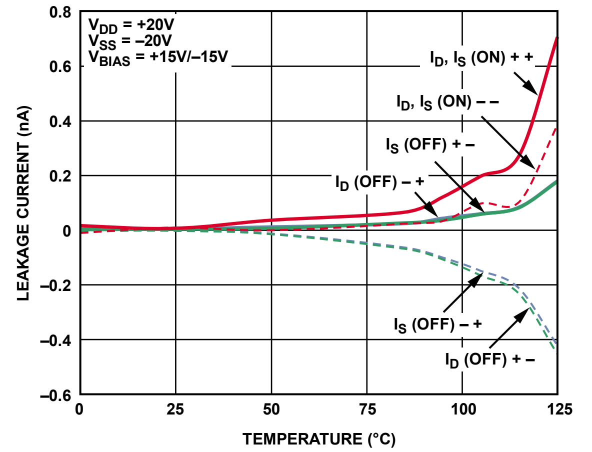

Figure 13. Leakage Currents vs. Temperature, ±20 V Dual Supply

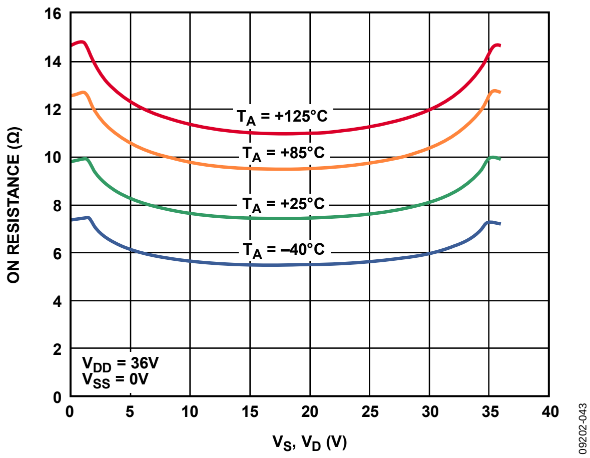

Figure 11. R_{ON} as a Function of V_S (V_D) for Different Temperatures, 36 V Single Supply

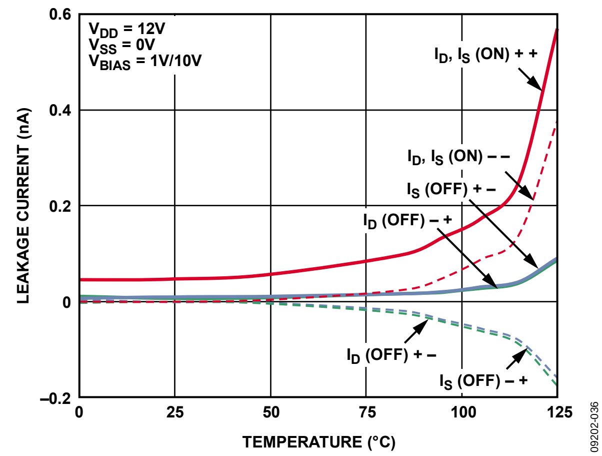

Figure 14. Leakage Currents vs. Temperature, 12 V Single Supply

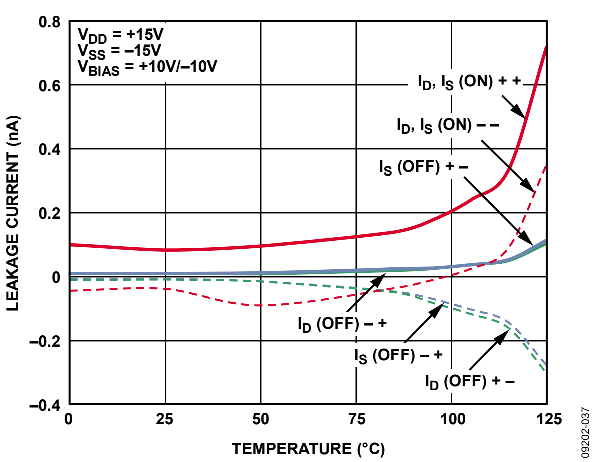

Figure 12. Leakage Currents vs. Temperature, ±15 V Dual Supply

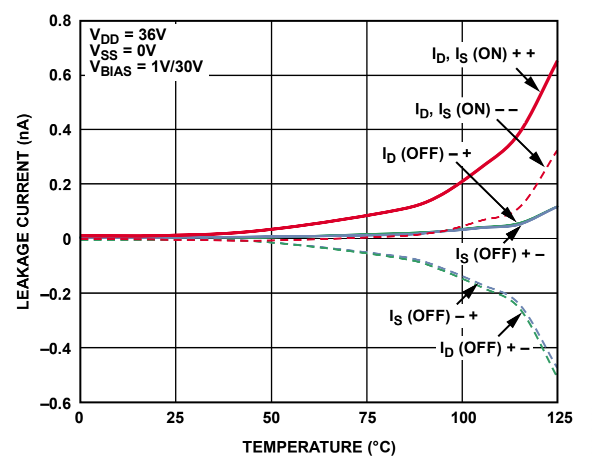

Figure 15. Leakage Currents vs. Temperature, 36 V Single Supply

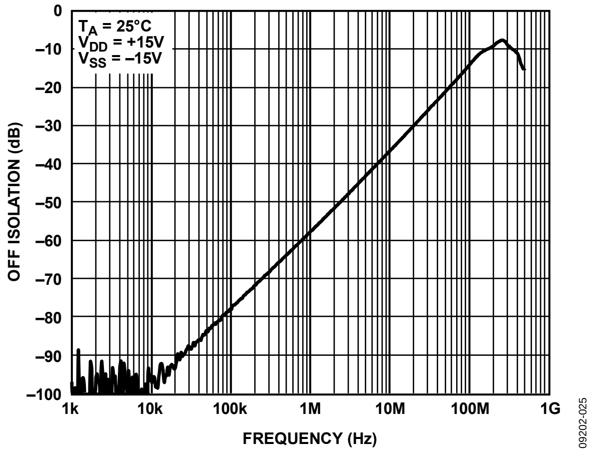

Figure 16. Off Isolation vs. Frequency, ±15 V Dual Supply

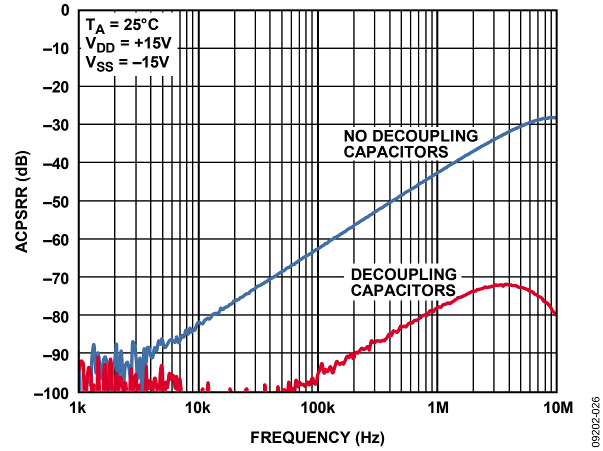

Figure 19. ACPSRR vs. Frequency, ±15 V Dual Supply

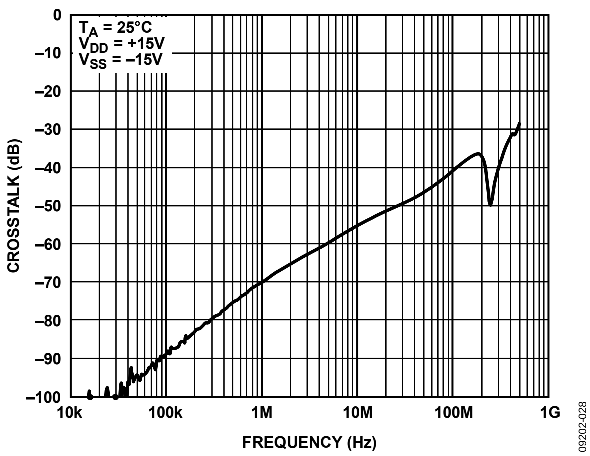

Figure 17. Crosstalk vs. Frequency, ±15 V Dual Supply

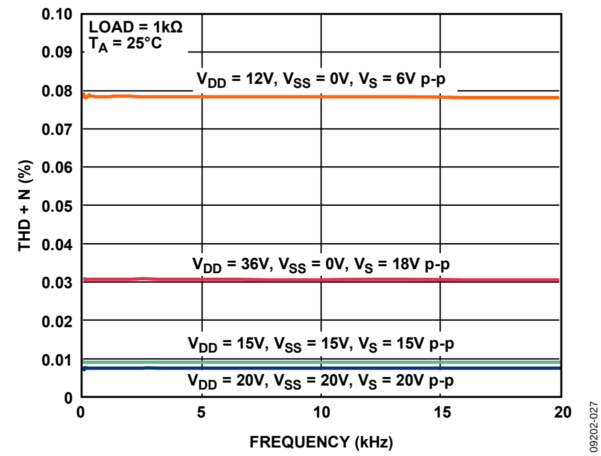

Figure 20. THD + N vs. Frequency, ±15 V Dual Supply

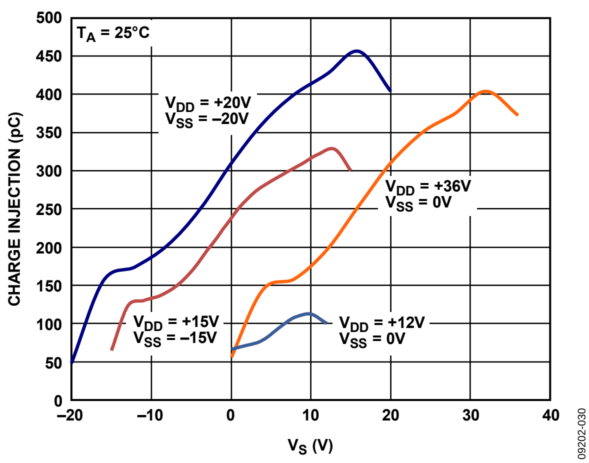

Figure 18. Charge Injection vs. Source Voltage

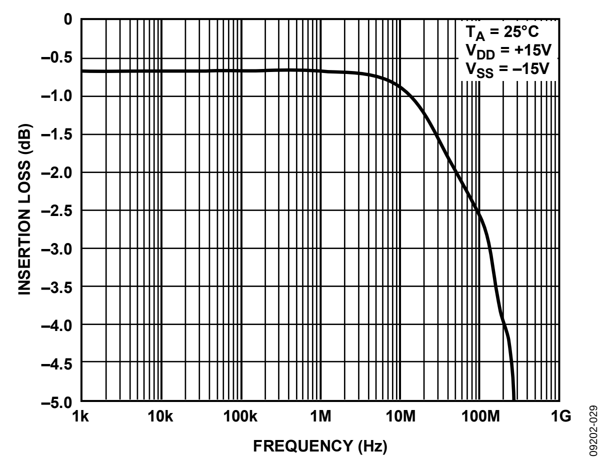

Figure 21. Bandwidth

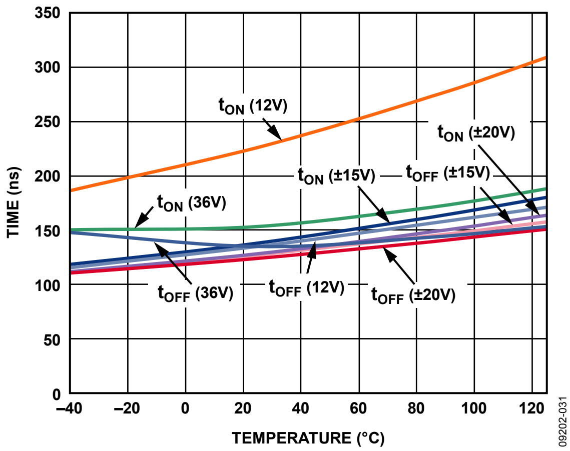

Figure 22. t_{ON}, t_{OFF} Times vs. Temperature

TEST CIRCUITS

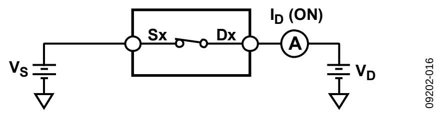

Figure 23. On Leakage

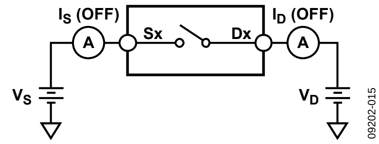

Figure 27. Off Leakage

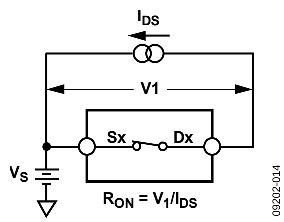

Figure 24. On Resistance

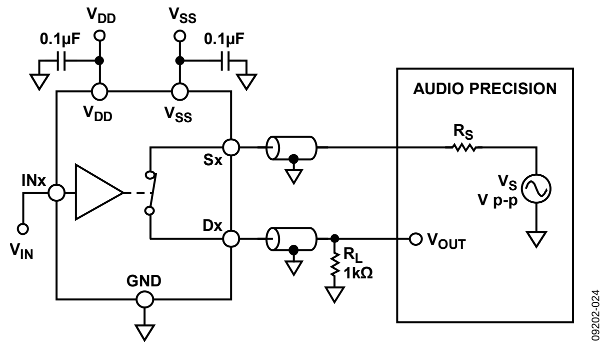

Figure 28. THD + Noise

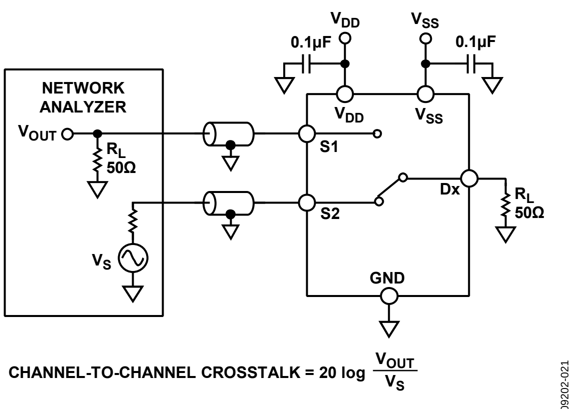

Figure 25. Channel-to-Channel Crosstalk

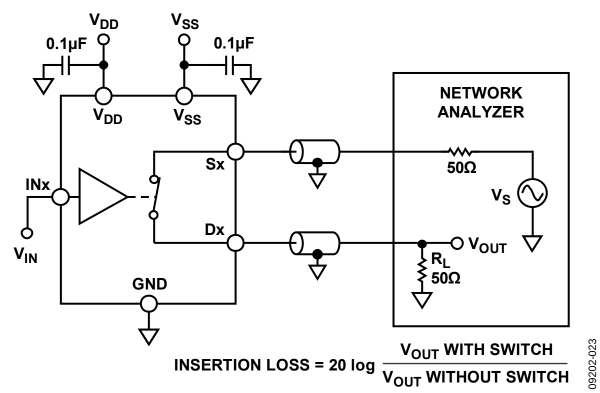

Figure 29. Bandwidth

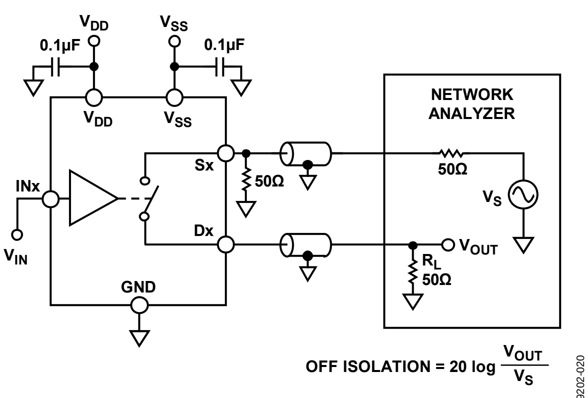

Figure 26. Off Isolation

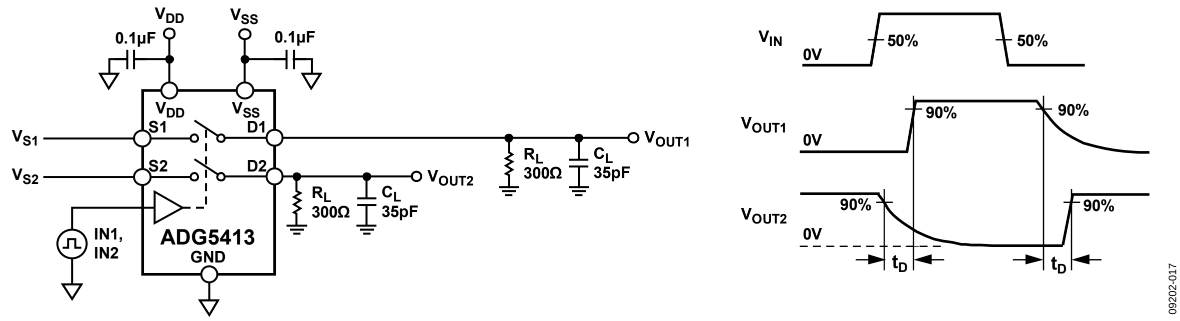

Figure 30. Break-Before-Make Time Delay, t_D

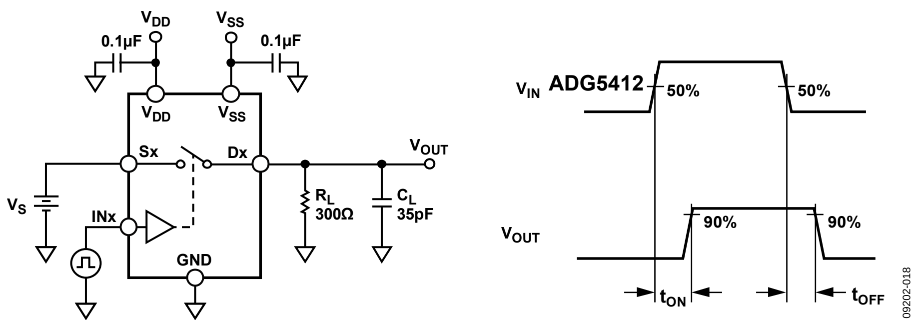

Figure 31. Switching Times

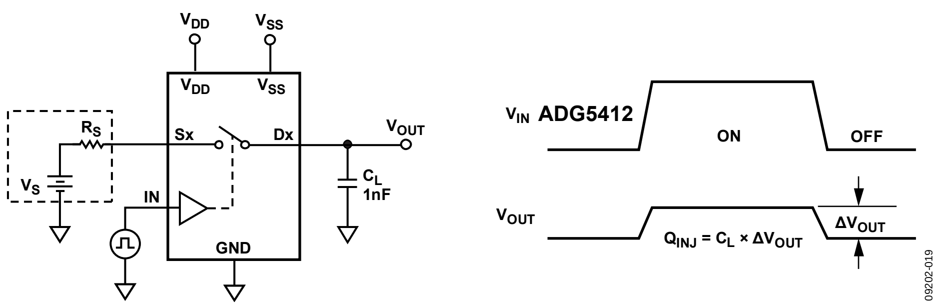

Figure 32. Charge Injection

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} represents the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} represents the delay between applying the digital control input and the output switching on.

t_{OFF}
t_{OFF} represents the delay between applying the digital control input and the output switching off.

t_D
t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

TRENCH ISOLATION

In the ADG5412 and ADG5413, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

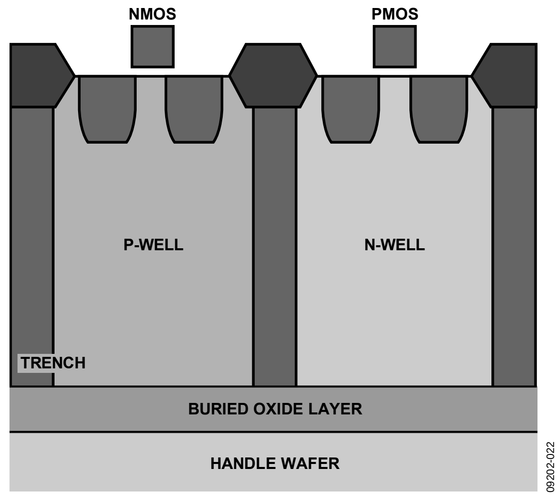

Figure 33. Trench Isolation

APPLICATIONS INFORMATION

The high voltage latch-up proof family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADG5412/ADG5413 high voltage switches allow single-supply operation from 9 V to 40 V and dual-supply operation from ±9 V to ±22 V. The ADG5412/ADG5413 (as well as other select devices within the same family) achieve an 8 kV human body model ESD rating, which provides a robust solution eliminating the need for separate protect circuitry designs in some applications.

OUTLINE DIMENSIONS

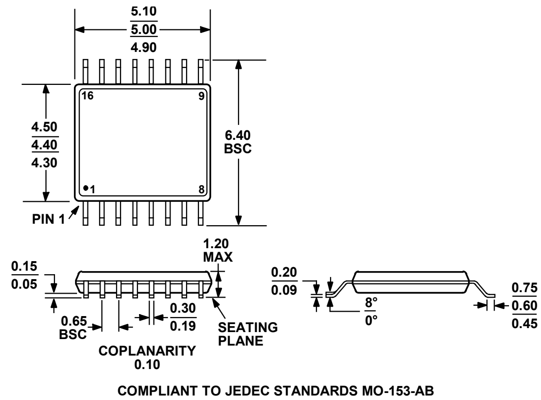

Figure 34. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

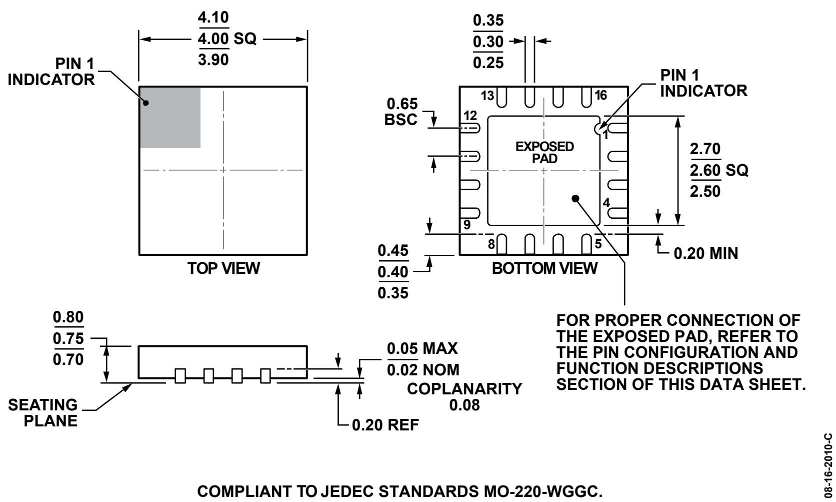

Figure 35. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1], [2]	Temperature Range	Package Description	Package Option
ADG5412BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5412BRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5412BCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17
ADG5413BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5413BRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5413BCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-17
EVAL-16TSSOPEBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The EVAL-16TSSOPEBZ can be used to test the ADG5412 and the ADG5413.