2.7V-5.5V Vin 2A Synchronous Step Down Convertor

FEATURES

- Input Voltage Range: 2.7V-5.5V
- Up to 2A Peak Output Current
- Low Shutdown Current 0.8uA
- Low Quiescent operating Current: 23uA
- +/- 1.5% Feedback Reference Voltage
- 1.5MHz Switching Frequency
- 100/60 mohm Internal Power Switch
- 100% Duty Cycle Mode
- Adjustable output voltage from 0.6 V to 5 V
- Active output discharge
- Programmable Soft Start Time
- Power Good Indicator
- Integrated Protection Feature
  - Cycle-by-cycle current limit
  - Under-voltage Lockout
  - HICCUP Over load Protection
  - Thermal Shutdown Protection:160°C
- DFN-8L1.5mm*2mm Package
- Available in a Wettable Flank Package
- AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Battery-Powered Devices
- Solid state driver
- Automotive Infotainment

DESCRIPTION

The SCT2120Q is a monolithic, step-down switch-mode converter with built-in internal power MOSFETs. The device achieves 2A of peak output current from a 2.7V to 5.5V input voltage range, with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V

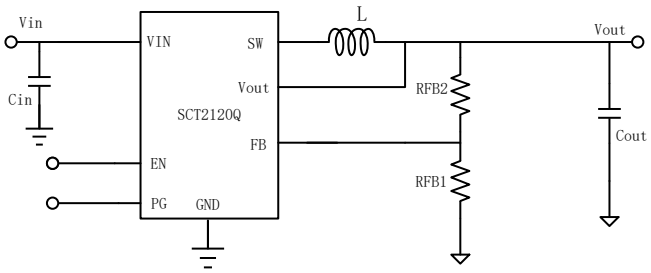
Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown.

The SCT2120Q operates in power saving mode, which maintains high efficiency during light load operation.

It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2120Q requires a minimal number of external components and is available in a space-saving DFN-8L1.5mm*2mm package.

TYPICAL APPLICATION



Typical Application

Efficiency

REVISION HISTORY

Revision 0.6: Customer Preview

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT2120QFTA	2120Q	DFN-8L1.5mm*2mm

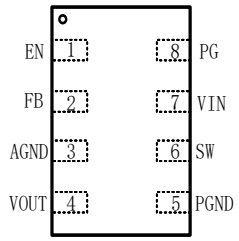
1) For Tape & Reel, Add Suffix R (e.g. SCT2120QFTAR)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN, PG, VOUT, SW,FB	-0.3	6	V
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: DFN-8L 1.5mm x 2mm, Plastic

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
EN	1	Enable logic input. Connect high to enable device
FB	2	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage
AGND	3	Analog Ground pin
VOUT	4	Output Pin
PGND	5	Power Ground pin
SW	6	Switch output. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time.
VIN	7	Power supply input pin
PG	8	Power-good indicator. The output of PG is an open drain that connects to VIN via an internal pull-up resistor. PG goes high if the output voltage is within ±10% of the nominal voltage.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	2.7	5.5	V
V_{OUT}	Output voltage range	0.6	5	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-2	+2	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(2)	-0.5	+0.5	kV

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	DFN-8L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	
Ψ_{JB}	Junction-to-board characterization parameter(1)	TBD	
$R_{\theta JCtop}$	Junction to case thermal resistance(1)	TBD	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	TBD	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2120Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2120Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=5V, T_J=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		2.7		5	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising		2.7		V
	Hysteresis			200		mV
I_{SD}	Shutdown current			800		nA
I_Q	Quiescent current from VIN	no load, no switching		23		uA
V_{FB}	Reference voltage of FB	Tj=25 °C	0.591	0.6	0.609	V
I_{FB}	FB pin leakage current				100	nA
Power switch						
R_{HS}	High-side switch on resistance			100		mΩ
R_{LS}	Low-side switch on resistance			60		mΩ
$ILIM_{HS}$	High-side peak current limit			3.2		A
$ILIM_{LS}$	High-side peak current limit			3		A
Soft start						
T_{SS}	Soft-start Time			1.5		mS
EN & PG						
V_{ENH}	High-level Threshold voltage		1.2			V
V_{ENL}	Low- level Threshold voltage				0.4	V
R_{EN}	EN Pull down resistance			2		MΩ
R_{DIS}	Output Discharge resistance			150		Ω
V_{PGTL}	Power Good Lower Threshold voltage	FB rinsing(Reference to V_{FB})		95		%
		FB falling(Reference to V_{FB})		90		%
V_{PGTH}	Power Good Upper Threshold voltage	FB rinsing(Reference to V_{FB})		110		%
		FB falling(Reference to V_{FB})		105		%
V_{PGTL}	Power Good Logic Low Level Voltage	IPG=-1mA			0.4	V
R_{PG}	Power Good Internal Pull up resistor			550		KΩ
T_{PGD}	Power Good Delay			80		uS
Switching Frequency						
F_{SW}	Switching frequency	Vin=5V,Vout=1.2V,CCM		1.5		MHz
t_{ON_MIN}	Minimum on-time			60		ns
t_{OFF_MIN}	Minimum off-time			100		ns
Protection						
T_{SD}	Thermal shutdown threshold			160		°C
	Hysteresis			20		°C

FUNCTIONAL BLOCK DIAGRAM

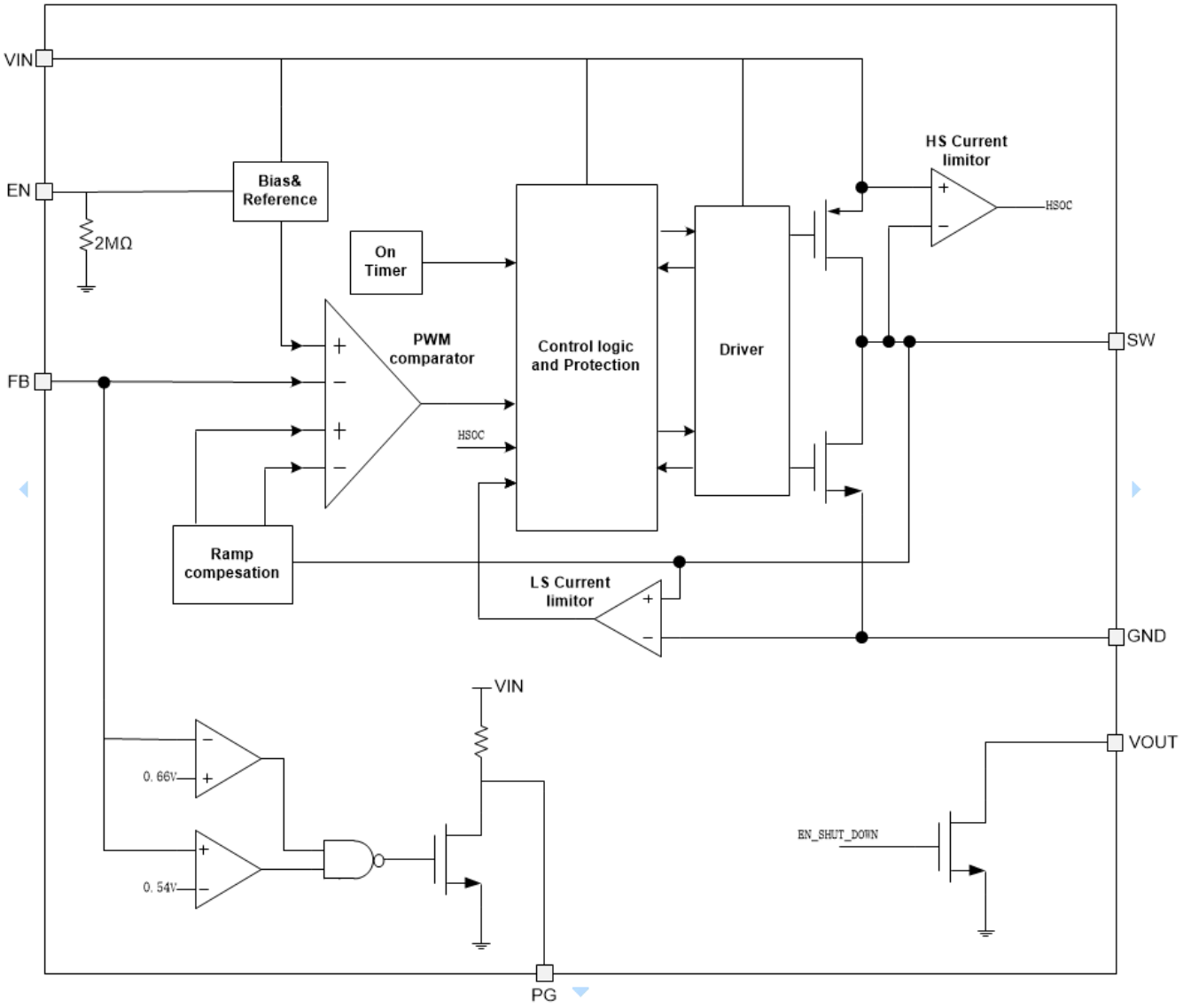


Figure 1. Functional Block Diagram

OPERATION

Constant On-time Control

The SCT2120Q device is 2.7-5.5V input, 2A output, synchronous step-down converters with internal power MOSFETs. Constant on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range. SCT2120Q turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2120Q turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S} \quad (1)$$

Where:

VOUT is the output voltage.
VIN is the input voltage.
fs is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.6V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 100ns typical.

Power Saving Mode (PSM)

The SCT2120Q is designed with Power Save Mode (PSM) at light load conditions for high power efficiency. The regulator automatically reduces the switching frequency and extends Toff while no Ton changing during the light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually nearing zero current, this is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only by output capacitor, when FB voltage is lower than 0.6V, the next ON cycle begins. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following equation (2):

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON} \quad (2)$$

Where:

TON is on-time

Under Voltage Lockout UVLO

The SCT2120Q Under Voltage Lock Out (UVLO) default startup threshold is typical 2.7V with VIN rising and shutdown threshold is 2.5V with VIN falling.

Enable(EN)

EN is a digital control pin that can turn the regulator on and off. When EN is pulled below the falling threshold voltage (0.4V), the chip shuts down. Force EN above its rising threshold voltage (1.2V) to turn the part on. Leave

EN floating or pull it down to ground to disable the SCT2120Q. There is an internal 2MΩ resistor connected from the EN pin to ground. When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET provides a resistive discharge path for the output capacitor**.**

Soft Start(SS)

The SCT2120Q has a build in soft start that ramps up the output voltage in a controlled slew rate avoiding overshoot at startup. The soft start time is about 1.5ms typical.

Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the high-side MOSFET during the ON period and the low-side MOSFET during the OFF period. When the inductor current (I_L) reaches the high-side MOSFET peak current limit (typically 3.2A) during the ON period, the high-side MOSFET is forced off immediately to prevent the current from rising further. Then the low-side MOSFET turns on, and stays on until I_L drops below the low-side MOSFET valley current limit (typically 3A). If output loading continues to increase, output will drop below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles' soft-start period.

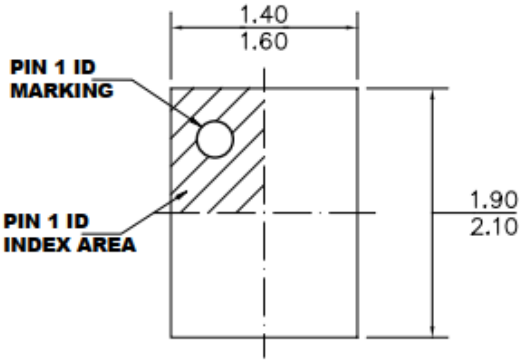
Power Good Indicator

The SCT2120Q has one power good (PG) output to indicate normal operation after the soft-start time. PG is an open drain of an internal pullup resistor 550KΩ. When FB is within ±10% of the regulation voltage (0.6V), PG is pulled up to VIN by the internal resistor. If the FB voltage is outside the ±10% window, PG is pulled to ground by an internal MOSFET.

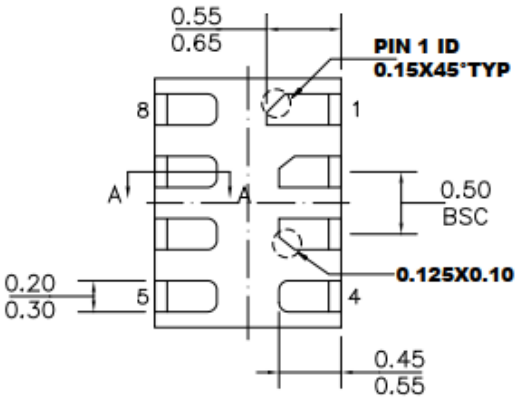
Thermal Shutdown

Once the junction temperature in the SCT2120Q exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

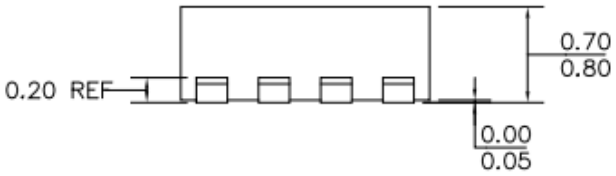
PACKAGE INFORMATION



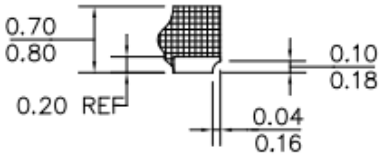
TOP VIEW



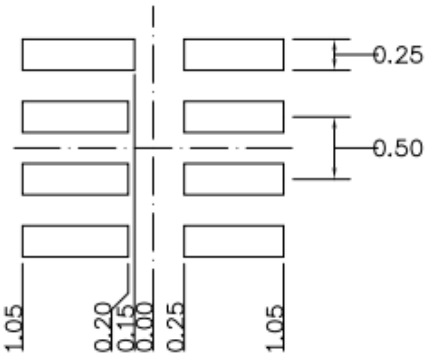
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

