# CSD25404Q3 -20V P 沟道 NexFET™ 功率 MOSFET

## 1 特性

- 超低 $Q_g$ 和 $Q_{gd}$
- 低热阻
- 低 $R_{DS(on)}$
- 无卤素
- 符合 RoHS 标准
- 无铅引脚镀层
- 小外形尺寸无引线 (SON) 3.3mm × 3.3mm 塑料封装

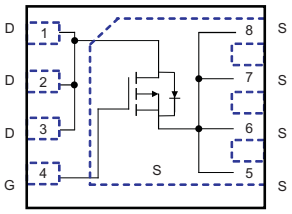
## 2 应用

- 直流-直流转换器
- 电池管理
- 负载开关
- 电池保护

## 3 说明

这款 -20V、5.5mΩ NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET) 旨在最大限度地降低功率转换和负载管理应用中的损耗。该器件采用 3.3mm × 3.3mm 小外形尺寸无引线 (SON) 封装，可提供出色的封装散热性能。

顶视图




产品概要

| $T_A$=25°C | | 典型值 | | 单位 |
|---|---|---|---|---|
| $V_{DS}$ | 漏源电压 | -20 | | V |
| $Q_g$ | 栅极电荷总量 (-4.5V) | 10.9 | | nC |
| $Q_{gd}$ | 栅漏栅极电荷 | 2.2 | | nC |
| $R_{DS(on)}$ | 漏源导通电阻 | $V_{GS}$ = –1.8V | 40 | mΩ |
| | | $V_{GS}$ = -2.5V | 10.1 | mΩ |
| | | $V_{GS}$ = -4.5V | 5.5 | mΩ |
| $V_{th}$ | 阈值电压 | -0.9 | | V |

订购信息(1)

| 器件 | 数量 | 包装介质 | 封装 | 运输 |
|---|---|---|---|---|
| CSD25404Q3 | 2500 | 13 英寸卷带 | SON 3.3mm × 3.3mm 塑料封装 | 卷带式 |
| CSD25404Q3T | 250 | 7 英寸卷带 | | |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

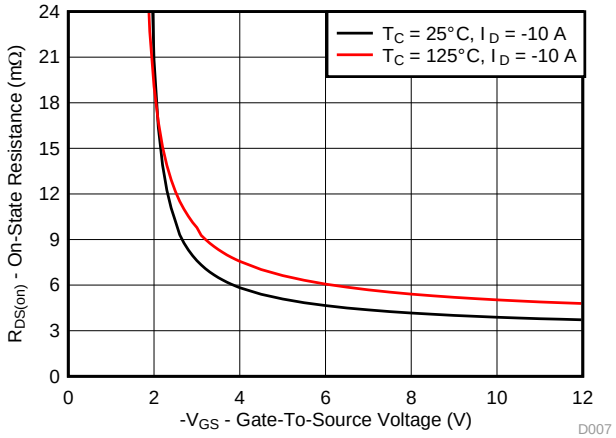
绝对最大额定值

| $T_A$ = 25°C | | 值 | 单位 |
|---|---|---|---|
| $V_{DS}$ | 漏源电压 | -20 | V |
| $V_{GS}$ | 栅源电压 | ±12 | V |
| $I_D$ | 持续漏极电流，$T_C$ = 25°C | –104 | A |
| | 持续漏极电流（受封装限制） | -60 | |
| | 持续漏极电流(1) | –18 | |
| $I_{DM}$ | 脉冲漏极电流(2) | –240 | A |
| $P_D$ | 功耗(1) | 2.8 | W |
| | 功耗，$T_C$ = 25°C | 96 | |
| $T_J$，$T_{stg}$ | 工作结温，储存温度 | -55 至 150 | °C |

(1) $R_{\theta JA}$ = 45°C/W，这是在厚度为 0.060" 的环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸$^2$ 铜过渡垫片（2 盎司）上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 1.3，脉冲持续时间 ≤ 100μs，占空比 ≤ 1%

$R_{DS(on)}$ 与 $V_{GS}$ 间的关系

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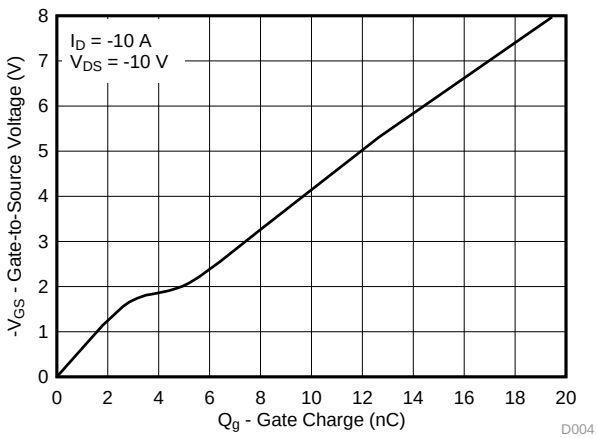
栅极电荷




D004

# 目录



## 4 修订历史记录

| 日期 | 修订版本 | 注释 |
|---|---|---|
| 2015 年 11 月 | * | 最初发布。 |

# 5 Specifications

## 5.1 Electrical Characteristics

($T_A$ = 25°C unless otherwise stated)

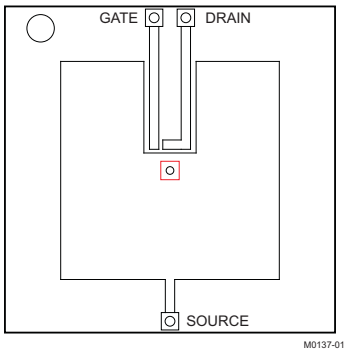
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-source voltage | $V_{GS}$ = 0 V, $I_D$ = –250 µA | –20 | | | V |
| $I_{DSS}$ | Drain-to-source leakage current | $V_{GS}$ = 0 V, $V_{DS}$ = –16 V | | | –1 | µA |
| $I_{GSS}$ | Gate-to-source leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | | | –100 | nA |
| $V_{GS(th)}$ | Gate-to-source threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA | –0.65 | –0.90 | –1.15 | V |
| $R_{DS(on)}$ | Drain-to-source on resistance | $V_{GS}$ = –1.8 V, $I_D$ = –1 A | | 40 | 150 | mΩ |
| | | $V_{GS}$ = –2.5 V, $I_D$ = –10 A | | 10.1 | 12.1 | mΩ |
| | | $V_{GS}$ = –4.5 V, $I_D$ = –10 A | | 5.5 | 6.5 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = –10 V, $I_D$ = –10 A | | 47 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{ISS}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = –10 V, $f$ = 1 MHz | | 1630 | 2120 | pF |
| $C_{OSS}$ | Output capacitance | | | 902 | 1170 | pF |
| $C_{RSS}$ | Reverse transfer capacitance | | | 52 | 68 | pF |
| $R_G$ | Series gate resistance | | | 0.8 | 2.4 | Ω |
| $Q_g$ | Gate charge total (–4.5 V) | $V_{DS}$ = –10 V, $I_D$ = –10 A | | 10.8 | 14.1 | nC |
| $Q_{gd}$ | Gate charge gate to drain | | | 2.2 | | nC |
| $Q_{gs}$ | Gate charge gate to source | | | 2.8 | | nC |
| $Q_{g(th)}$ | Gate charge at $V_{th}$ | | | 1.5 | | nC |
| $Q_{OSS}$ | Output charge | $V_{DS}$ = –10 V, $V_{GS}$ = 0 V | | 9.0 | | nC |
| $t_{d(on)}$ | Turn on delay time | $V_{DS}$ = –10 V, $V_{GS}$ = –4.5 V, $I_D$ = –10 A , $R_G$ = 5 Ω | | 13 | | ns |
| $t_r$ | Rise time | | | 8 | | ns |
| $t_{d(off)}$ | Turn off delay time | | | 35 | | ns |
| $t_f$ | Fall time | | | 13 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode forward voltage | $I_S$ = –10 A, $V_{GS}$ = 0 V | | –0.8 | –1 | V |
| $Q_{rr}$ | Reverse recovery charge | $V_{DS}$ = –10 V, $I_F$ = –10 A, di/dt = 200 A/µs | | 20.5 | | nC |
| $t_{rr}$ | Reverse recovery time | | | 26 | | ns |

## 5.2 Thermal Information

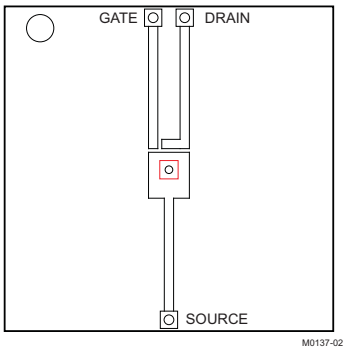
($T_A$ = 25°C unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-case thermal resistance(1) | | | 1.3 | °C/W |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance(1)(2) | | | 55 | °C/W |

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch$^2$ (6.45 cm$^2$), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch$^2$ (6.45 cm$^2$), 2 oz. (0.071 mm thick) Cu.




Max $R_{\theta JA}$ = 55°C/W when mounted on 1 inch$^2$ of 2 oz. Cu.




Max $R_{\theta JA}$ = 160°C/W when mounted on minimum pad area of 2 oz. Cu.

## 5.3 Typical MOSFET Characteristics

($T_A$ = 25°C unless otherwise stated)

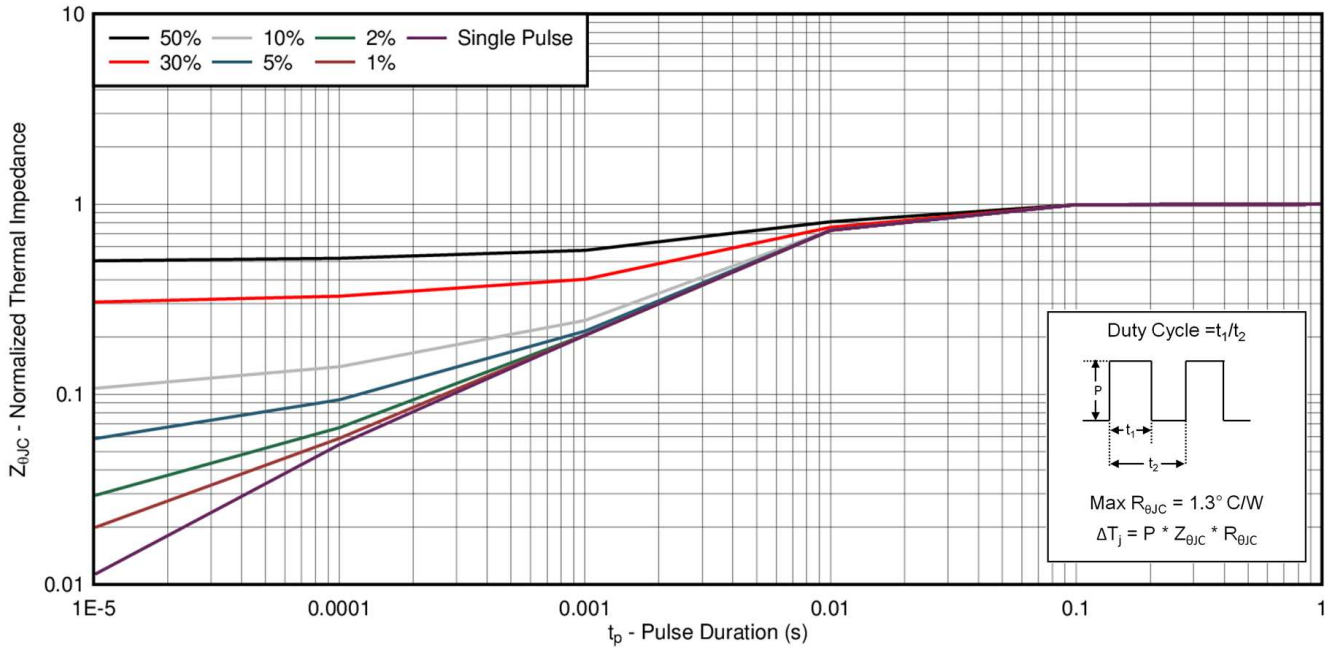



**Figure 1. Transient Thermal Impedance**

## Typical MOSFET Characteristics (continued)

($T_A$ = 25°C unless otherwise stated)

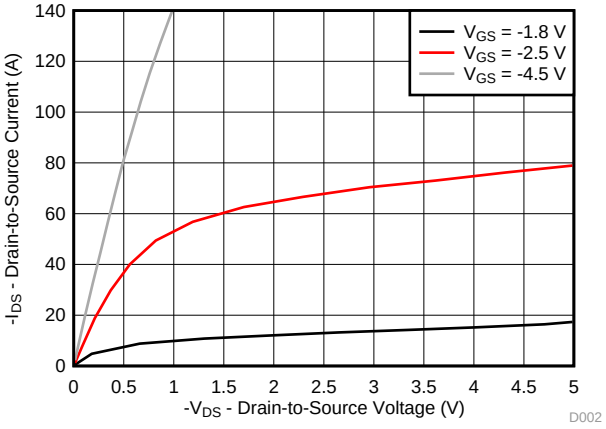
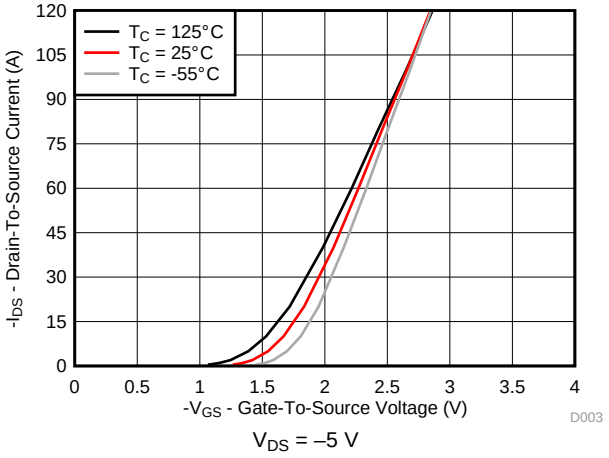
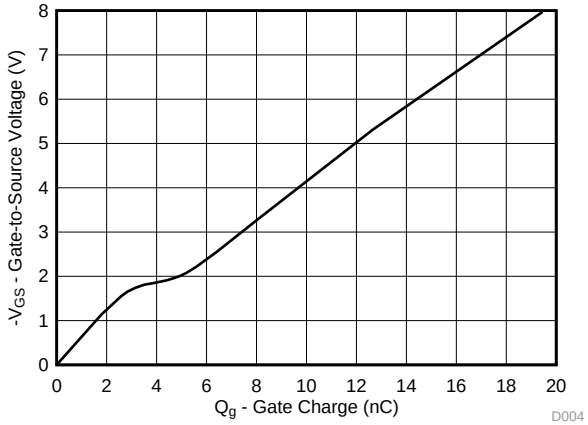



**Figure 2. Saturation Characteristics**




VDS = –5 V

**Figure 3. Transfer Characteristics**




ID = –10 A VDS = –10 V

**Figure 4. Gate Charge**

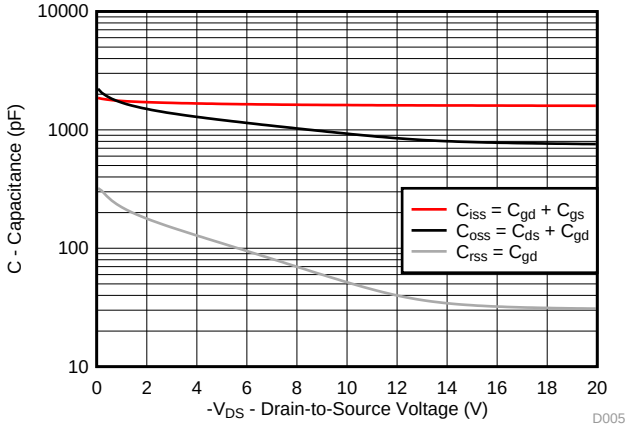
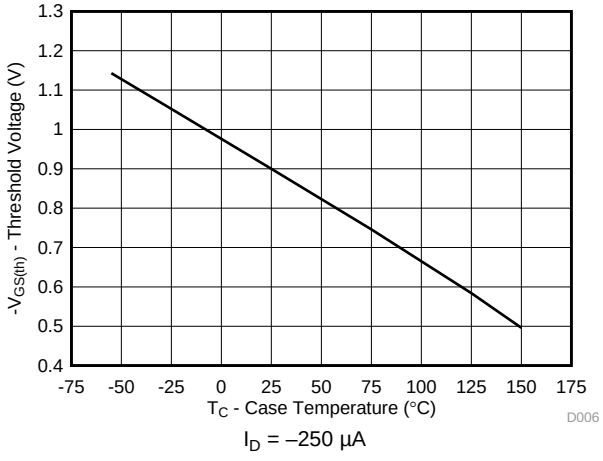



**Figure 5. Capacitance**




ID = –250 µA

**Figure 6. Threshold Voltage vs Temperature**

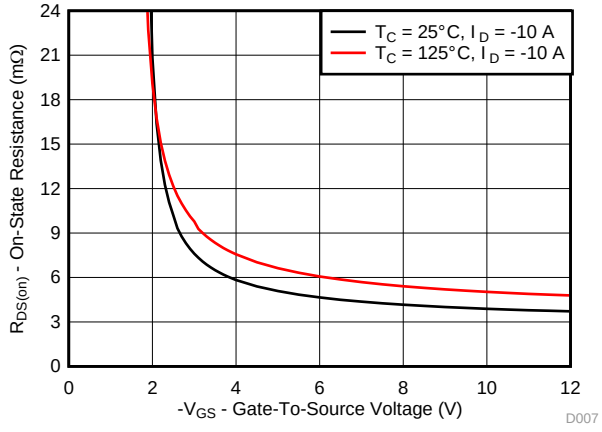
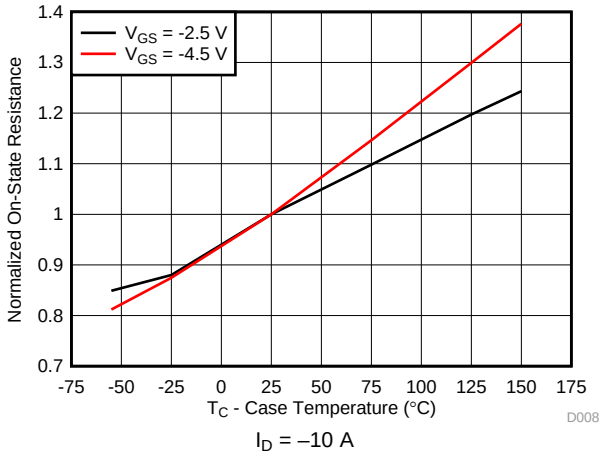



**Figure 7. On-State Resistance vs Gate-to-Source Voltage**

## Typical MOSFET Characteristics (continued)

($T_A$ = 25°C unless otherwise stated)




ID = –10 A

**Figure 8. Normalized On-State Resistance vs Temperature**

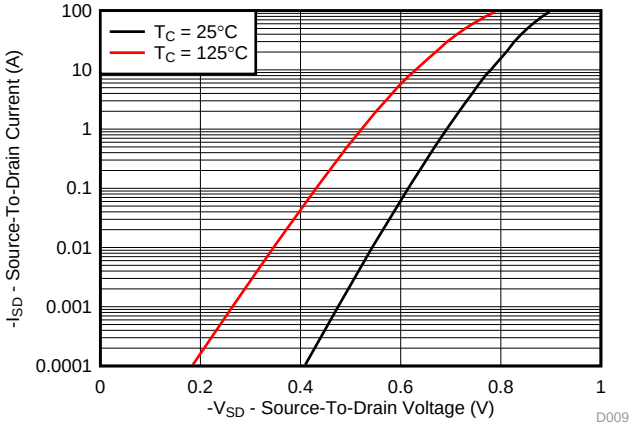
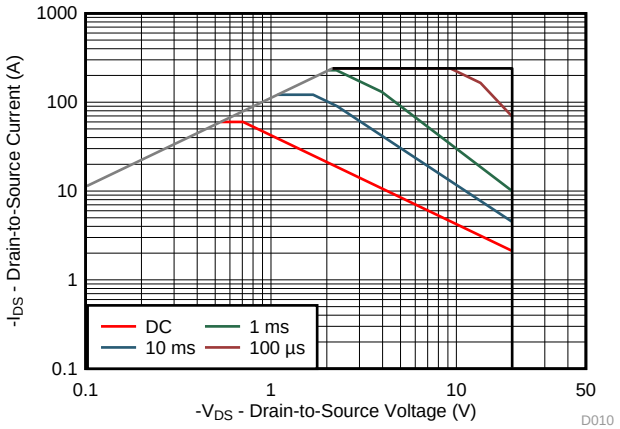



**Figure 9. Typical Diode Forward Voltage**




Single Pulse, Max $R_{\theta JC}$ = 1.3 °C/W

**Figure 10. Maximum Safe Operating Area**

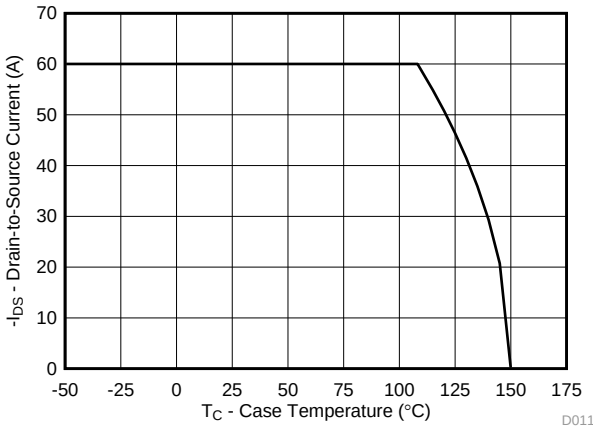



**Figure 11. Maximum Drain Current vs Temperature**

# 6 器件和文档支持

## 6.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 6.2 商标

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 6.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 6.4 Glossary

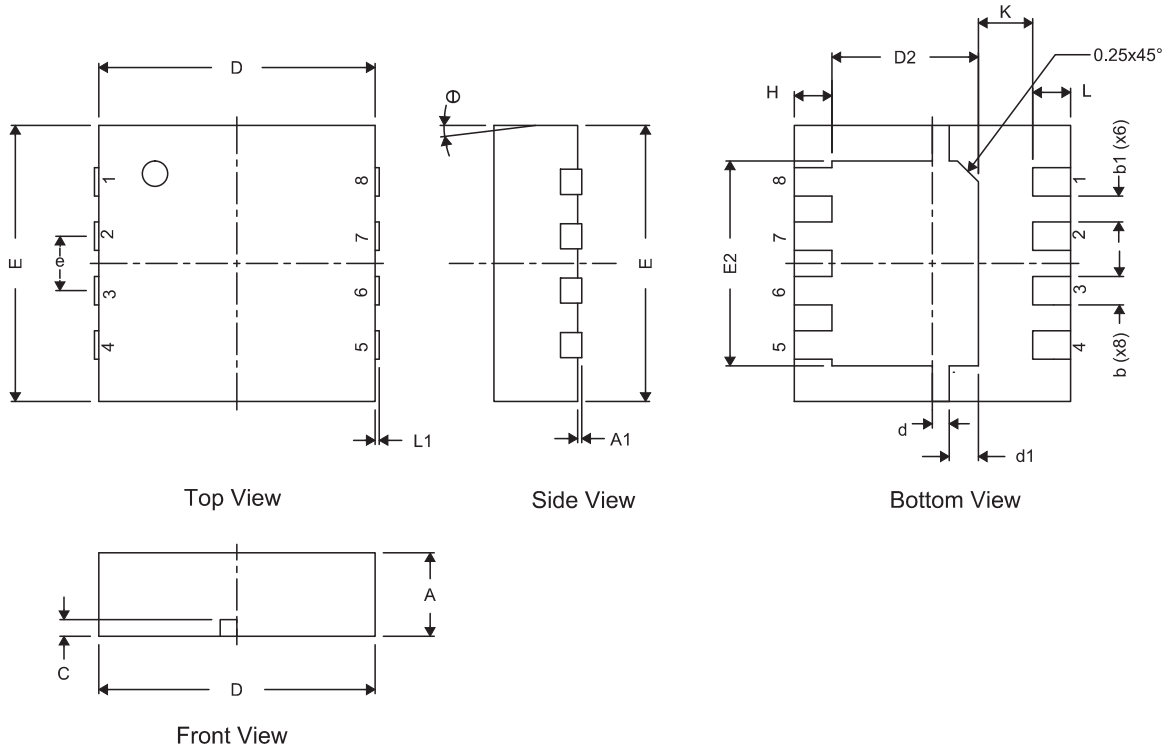
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 7 机械、封装和可订购信息

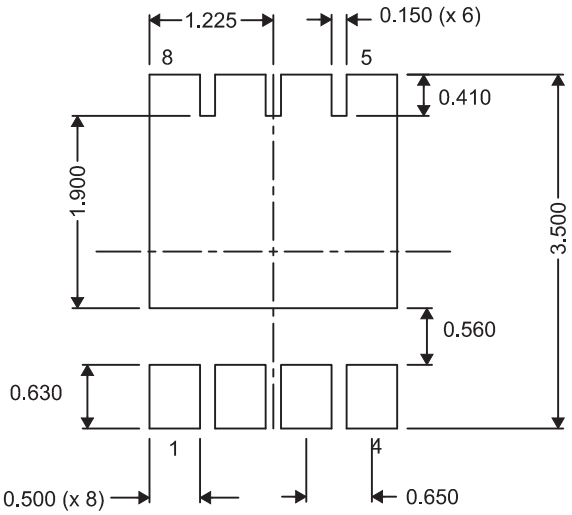
以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

## 7.1 CSD25404Q3 封闭尺寸



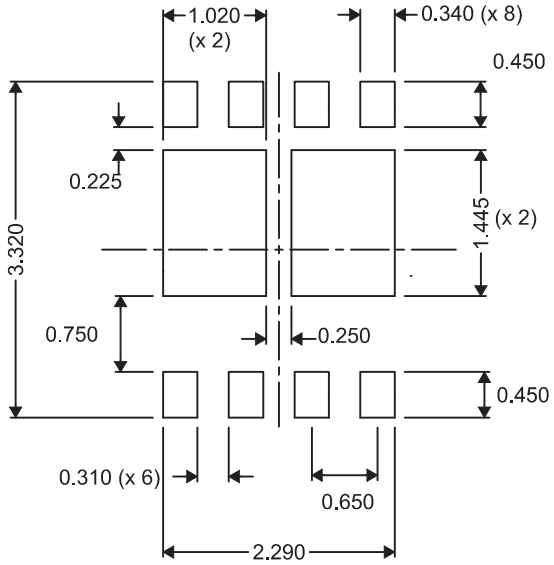

| DIM | 毫米 | | | 英寸 | | |
|---|---|---|---|---|---|---|
| | 最小值 | 标称值 | 最大值 | 最小值 | 标称值 | 最大值 |
| A | 0.950 | 1.000 | 1.100 | 0.037 | 0.039 | 0.043 |
| A1 | 0.000 | 0.000 | 0.050 | 0.000 | 0.000 | 0.002 |
| b | 0.280 | 0.340 | 0.400 | 0.011 | 0.013 | 0.016 |
| b1 | | 0.310（标称值） | | | 0.012（标称值） | |
| c | 0.150 | 0.200 | 0.250 | 0.006 | 0.008 | 0.010 |
| D | 3.200 | 3.300 | 3.400 | 0.126 | 0.130 | 0.134 |
| D2 | 1.650 | 1.750 | 1.800 | 0.065 | 0.069 | 0.071 |
| d | 0.150 | 0.200 | 0.250 | 0.006 | 0.008 | 0.010 |
| d1 | 0.300 | 0.350 | 0.400 | 0.012 | 0.014 | 0.016 |
| E | 3.200 | 3.300 | 3.400 | 0.126 | 0.130 | 0.134 |
| E2 | 2.350 | 2.450 | 2.550 | 0.093 | 0.096 | 0.100 |
| e | | 0.650 典型值 | | | 0.026 典型值 | |
| H | 0.35 | 0.450 | 0.550 | 0.014 | 0.018 | 0.022 |
| K | | 0.650 典型值 | | | 0.026 典型值 | |
| L | 0.35 | 0.450 | 0.550 | 0.014 | 0.018 | 0.022 |
| L1 | 0 | — | 0 | 0 | — | 0 |
| θ | 0 | — | 0 | 0 | — | 0 |

## 7.2 建议 PCB 布局



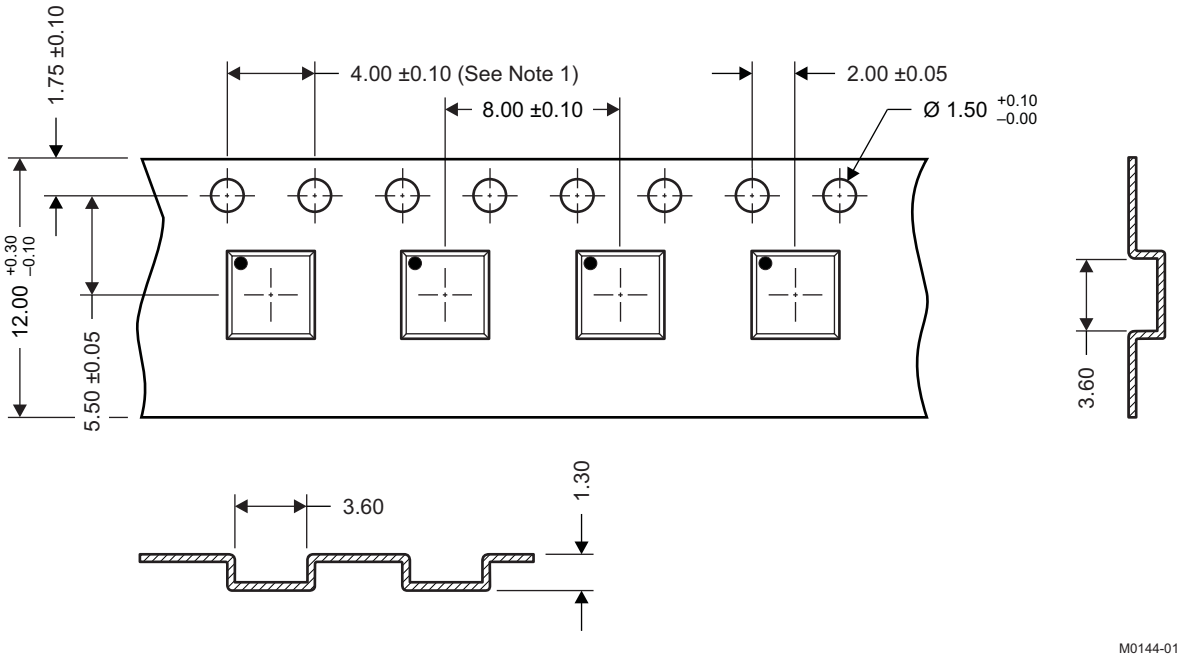

要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线，请参见《应用说明》SLPA005 - *通过 PCB 布局布线技巧来减少振铃*。

## 7.3 建议模板开口




全部尺寸单位为 mm，除非另外注明。

## 7.4 Q3 卷带信息




注释：

1. 10 链轮孔距累积容差为 ±0.2
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积
3. 材料：黑色抗静电聚苯乙烯
4. 全部尺寸单位为 mm（除非另外注明）。
5. 厚度：0.30 ± 0.05mm
6. MSL1 260°C（红外 (IR) 和传导）无铅回流焊兼容

10-Dec-2020

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD25404Q3 | ACTIVE | VSON-CLIP | DQG | 8 | 2500 | RoHS-Exempt & Green | SN | Level-1-260C-UNLIM | -55 to 150 | CSD25404 | Samples |
| CSD25404Q3T | ACTIVE | VSON-CLIP | DQG | 8 | 250 | RoHS-Exempt & Green | SN | Level-1-260C-UNLIM | -55 to 150 | CSD25404 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

10-Dec-2020