GENERAL DESCRIPTION

The SGM61233 is a current mode controlled synchronous Buck converter with 4.5V to 28V input range and 3A rated output current. The quiescent current is 320µA (TYP) and the shutdown supply current is 2µA (TYP). Two MOSFETs with low R_{DSON} are integrated to improve the efficiency. Efficiency is maximized through power-save mode (PSM) at light load. The SGM61233A has a wide selectable switching frequency (50kHz to 1500kHz) to allow desired tradeoff between efficiency and component sizes. The SGM61233B has adjustable soft-start time for flexible application. The SGM61233C has a fixed 340kHz switching frequency and a fixed internal 2ms soft-start time.

The UVLO level can be adjusted (increased) by an external resistor divider. Secure operation in overload conditions is ensured by cycle-by-cycle current limit, hiccup protection and thermal shutdown protection. The low-side MOSFET has sinking current limit to prevent excessive reverse current.

The SGM61233 is offered in the Green SOIC-8 (Exposed Pad) and TDFN-3×3-10L packages.

FEATURES

- **4.5V to 28V Input Voltage Range**
- **0.8V Internal Voltage Reference**
- **Typical 320µA Quiescent Current**
- **Typical 2µA Shutdown Current**
- **Integrated 118mΩ and 81mΩ MOSFETs Support up to 3A Continuous Output Current**
- **SGM61233A: Internal 2ms Soft-Start, 50kHz to 1500kHz Adjustable Frequency**
- **SGM61233B: Adjustable Soft-Start, Fixed 340kHz Frequency**
- **SGM61233C: Internal 2ms Soft-Start, Fixed 340kHz Frequency**
- **High Light-Load Efficiency**
- **Hiccup Mode Over-Current Protection**
- **Over-Voltage Protection**
- **Thermal Shutdown Protection**
- **Available in Green SOIC-8 (Exposed Pad) and TDFN-3×3-10L Packages**

APPLICATIONS

Industrial Power Supplies
Distributed Power Bus Supplies
LCD Display
CPE Equipment
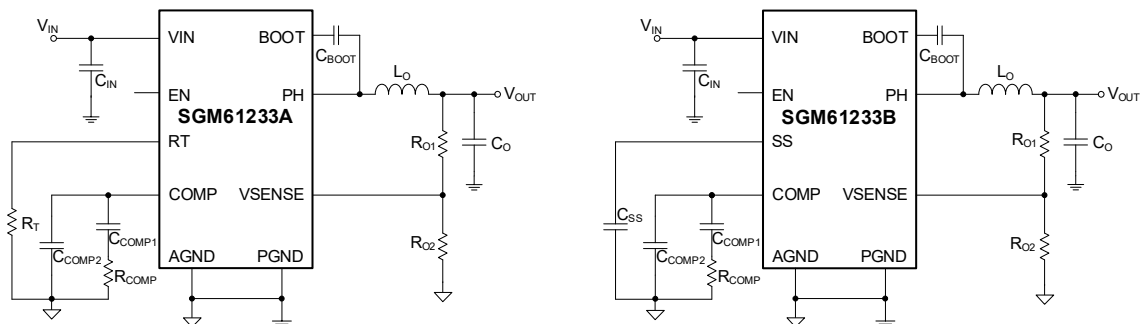Set-Top Displays
Battery Chargers

## TYPICAL APPLICATION

Figure 1. Typical Application Circuits

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61233A	SOIC-8 (Exposed Pad)	-40℃ to +150℃	SGM61233ATPS8G/TR	SGM MD3TPS8 XXXXX	Tape and Reel, 4000
	TDFN-3×3-10L	-40℃ to +150℃	SGM61233ATTD10G/TR	SGM MDGD XXXXX	Tape and Reel, 4000
SGM61233B	SOIC-8 (Exposed Pad)	-40℃ to +150℃	SGM61233BTPS8G/TR	SGM MDHTPS8 XXXXX	Tape and Reel, 4000
	TDFN-3×3-10L	-40℃ to +150℃	SGM61233BTTD10G/TR	SGM MDID XXXXX	Tape and Reel, 4000
SGM61233C	SOIC-8 (Exposed Pad)	-40℃ to +150℃	SGM61233CTPS8G/TR	SGM 066TPS8 XXXXX	Tape and Reel, 4000
	TDFN-3×3-10L	-40℃ to +150℃	SGM61233CTTD10G/TR	SGM 065D XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

X X X X X
— Vendor Code
— Trace Code
— Date Code - Year
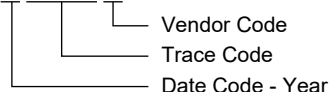
Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range .... -0.3V to 30V
EN Voltage.. -0.3V to 6V
BOOT Voltage .... -0.3V to (V_{PH} + 6.5)V
VSENSE, COMP, RT, SS Voltage .... -0.3V to 3V
BOOT-PH Voltage ....0V to 6.5V
PH Voltage.. -1V to 30V
PH Voltage (10ns Transient)............................ -3.5V to 30V
V_{DIFF}, (GND to Exposed Thermal Pad) ....-0.2V to 0.2V
Package Thermal Resistance
SOIC-8 (Exposed Pad), θ_{JA} .... 37℃/W
TDFN-3×3-10L, θ_{JA} .... 43℃/W
Junction Temperature..+150℃
Storage Temperature Range ....-65℃ to +150℃
Lead Temperature (Soldering, 10s) ....+260℃
ESD Susceptibility
HBM...3000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ....4.5V to 28V
Output Voltage Range ....0.8V to 24V
Output Current Range ....0A to 3A
Operating Junction Temperature Range......-40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.
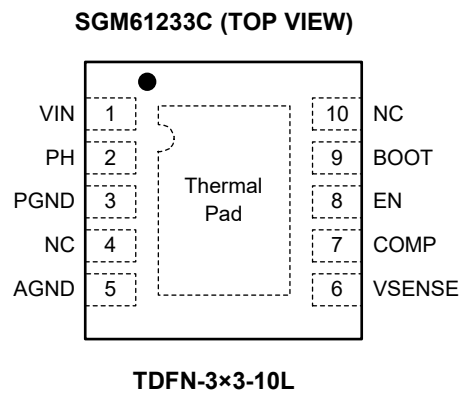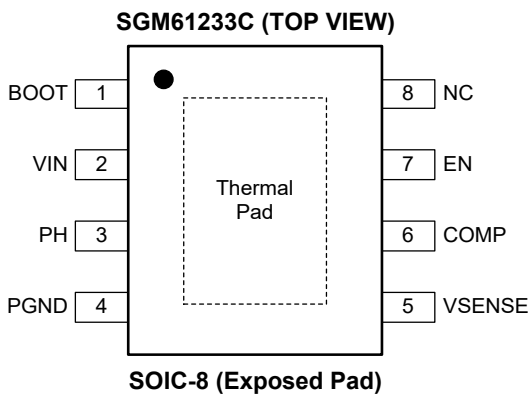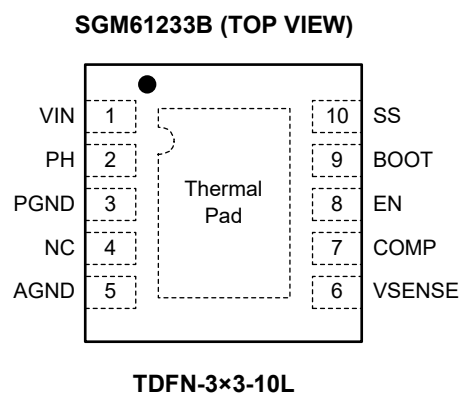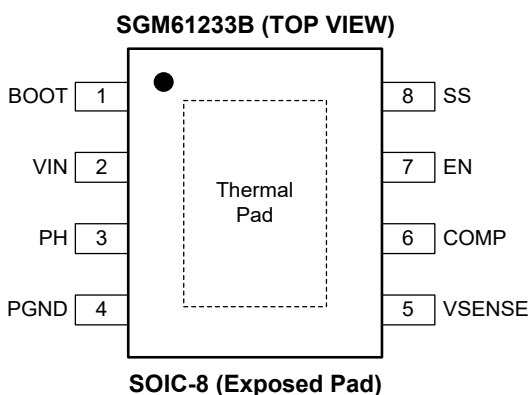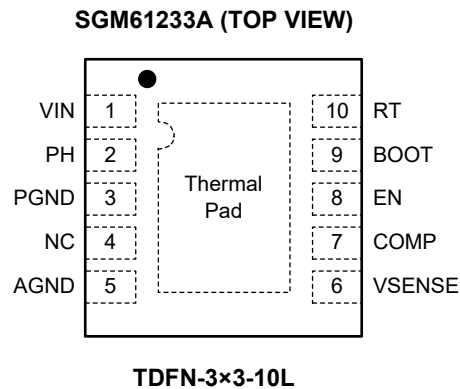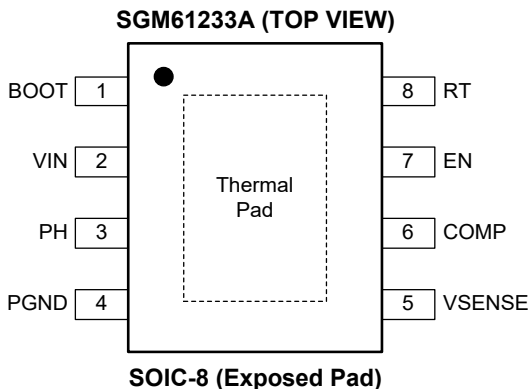
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

SGM61233A (TOP VIEW)

BOOT	1		8	RT
VIN	2	Thermal Pad	7	EN
PH	3		6	COMP
PGND	4		5	VSENSE

SOIC-8 (Exposed Pad)

SGM61233A (TOP VIEW)

VIN	1		10	RT
PH	2		9	BOOT
PGND	3	Thermal Pad	8	EN
NC	4		7	COMP
AGND	5		6	VSENSE

TDFN-3×3-10L

SGM61233B (TOP VIEW)

BOOT	1		8	SS
VIN	2	Thermal Pad	7	EN
PH	3		6	COMP
PGND	4		5	VSENSE

SOIC-8 (Exposed Pad)

SGM61233B (TOP VIEW)

VIN	1		10	SS
PH	2		9	BOOT
PGND	3	Thermal Pad	8	EN
NC	4		7	COMP
AGND	5		6	VSENSE

TDFN-3×3-10L

SGM61233C (TOP VIEW)

BOOT	1		8	NC
VIN	2	Thermal Pad	7	EN
PH	3		6	COMP
PGND	4		5	VSENSE

SOIC-8 (Exposed Pad)

SGM61233C (TOP VIEW)

VIN	1		10	NC
PH	2		9	BOOT
PGND	3	Thermal Pad	8	EN
NC	4		7	COMP
AGND	5		6	VSENSE

TDFN-3×3-10L

PIN DESCRIPTION

NAME	PIN		I/O	FUNCTION
	SOIC-8 (Exposed Pad)	TDFN-3×3-10L		
BOOT	1	9	O	Bootstrap Input. Connect it to PH pin with a 0.1µF ceramic capacitor. The MOSFET will turn off if the BOOT capacitor voltage drops below its BOOT-PH UVLO level to get the capacitor voltage refreshed.
VIN	2	1	I	Input Supply Voltage. Connect it to a 4.5V to 28V power source.
PH	3	2	O	Switching Node of the Converter. Connect it to the bootstrap capacitor and the inductor.
PGND	4	3	G	Power Ground.
VSENSE	5	6	I	Transconductance (gm) Error Amplifier (EA) Inverting Input. It is used as the feedback input to sense and regulate VOUT. Output voltage is set by a resistor divider from the output.
COMP	6	7	O	EA Output (internally connected to the PWM comparator input). Place the compensation network between COMP and AGND. The EA output current is injected into this network to create the control voltage (VC). It will be compared with the compensated sensed current signal to generate the switching pulses (set duty cycle).
EN	7	8	I	Active High Enable Input. Float or pull up to enable, or pull down below 1.13V (TYP) to disable the device. VIN UVLO level can be programmed using a resistor divider from VIN.
RT			O	Frequency is set by connecting an external resistor between the RT pin and AGND. (SGM61233A Only)
SS	8	10	O	Soft-Start Program. Connect an external capacitor to SS pin to program the output rise time during startup. (SGM61233B Only)
NC			—	No Connection (SGM61233C Only). This pin must be left floating.
NC	—	4	—	No Connection.
AGND	Thermal Pad	5	G	Analog Ground. It must be connected to PGND pin for proper operation.
Thermal Pad	—	Thermal Pad	—	It helps to cool the device junction and must be connected to PGND pin for proper operation.

NOTE: I = Input, O = Output, G = GND.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +150℃, V_{IN} = 4.5V to 28V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage and UVLO (VIN Pin)						
Operating Input Voltage	V_{IN}		4.5		28	V
Input UVLO Threshold	V_{UVLO}	Rising V_{IN}		4.2	4.5	V
Input UVLO Hysteresis	V_{UVLO_HYS}			270	350	mV
VIN-Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V		2	10	µA
VIN-Operating Non-Switching Supply Current	I_Q	V_{VSENSE} = 810mV		320	460	µA
Enable (EN Pin)						
Enable Threshold	V_{EN_TH}	Rising		1.2	1.31	V
		Falling	1.02	1.13		V
Input Current	I_{EN}	V_{EN} = 1.1V		1.15		µA
Hysteresis Current	I_{HYS}	V_{EN} = 1.3V		3.7		µA
Voltage Reference						
Voltage Reference	V_{REF}	T_J = +25℃	0.792	0.8	0.812	V
		T_J = -40℃ to +150℃	0.790	0.8	0.814	
MOSFET						
High-side Switch Resistance [1]	R_{DSON_HS}	$V_{BOOT-PH}$ = 3.5V		128	230	mΩ
		$V_{BOOT-PH}$ = 5V		118	220	
Low-side Switch Resistance [1]	R_{DSON_LS}	V_{IN} = 12V		81	150	mΩ
Error Amplifier						
Error-Amplifier Transconductance	gm_{EA}	-2µA < I_{COMP} < 2µA, V_{COMP} = 1V		1300		µmhos
Error-Amplifier Source and Sink Current	I_{EA}	V_{COMP} = 1V, 100mV overdrive		145		µA
Start Switching Peak Current Threshold [2]	I_{gm}			0.5		A
COMP to I_{SWITCH} gm	gm_{PS}			8		A/V
Current Limit						
High-side Switch Current Limit Threshold	I_{LIM_HS}	V_{IN} = 12V	4.7	5.7	6.7	A
Low-side Switch Sourcing Current Limit	I_{LIM_LS}	V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 340kHz	3.4	4.7	6	A
Low-side Switch Sinking Current Limit				0.1		A
Thermal Shutdown						
Thermal Shutdown [2]	T_{SHDN}			175		℃
Thermal Shutdown Hysteresis [2]	T_{HYS}			10		℃
BOOT Pin						
BOOT-PH UVLO	$V_{UVLO\_BOOT-PH}$			3.25	3.6	V
Soft-Start						
Soft-Start Charge Current, SGM61233B	I_{SS}			2.4		µA

NOTES:

1. Measured at pins.

2. Not production tested.

TIMING REQUIREMENTS

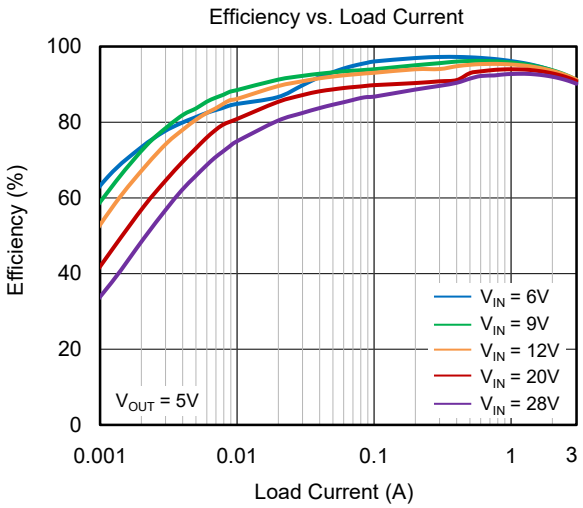| PARAMETER	MIN	TYP	MAX	UNITS
Current Limit				
Hiccup Wait Time		512		Cycles
Hiccup Time before Restart		16384		Cycles
Thermal Shutdown				
Thermal Shutdown Hiccup Time		32768		Cycles
Soft-Start				
Internal Soft-Start Time, SGM61233A and SGM61233C		2		ms

SWITCHING CHARACTERISTICS

(T_J = -40℃ to +150℃, and typical values are at T_J = +25℃, unless otherwise noted.)

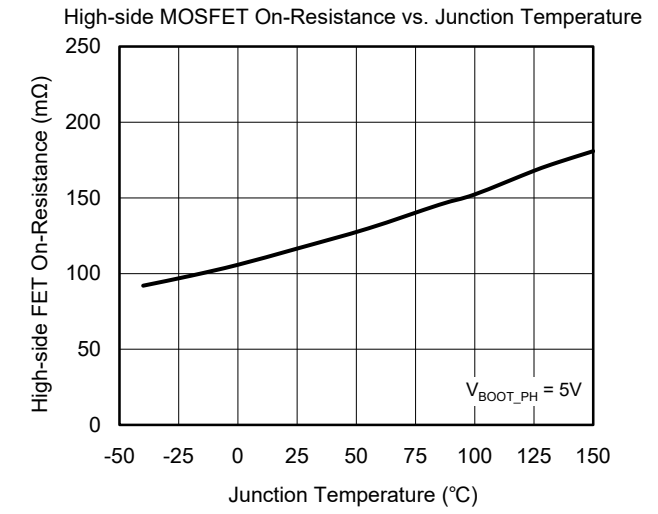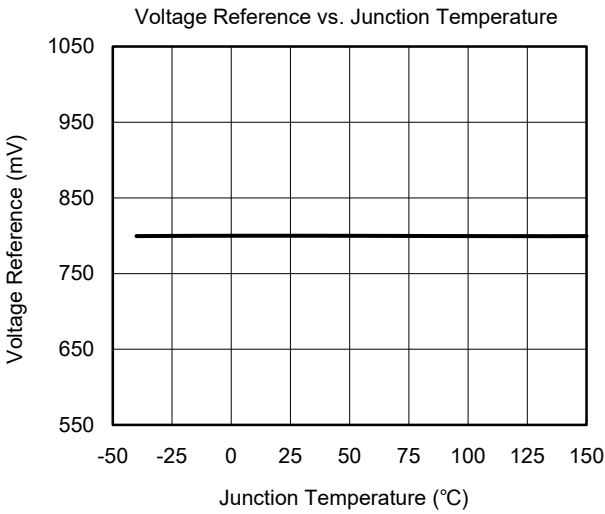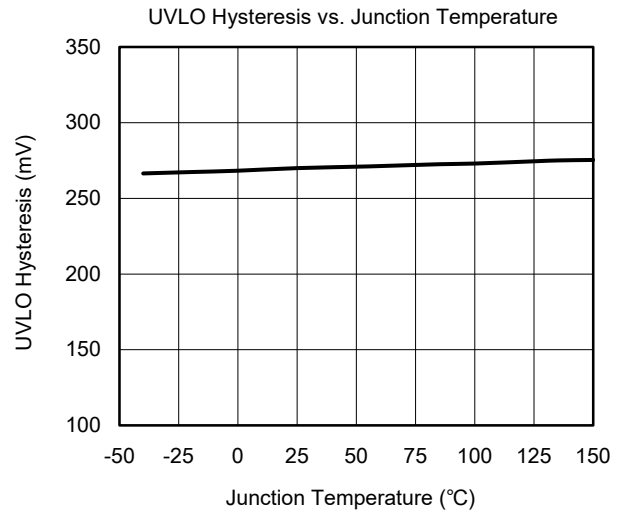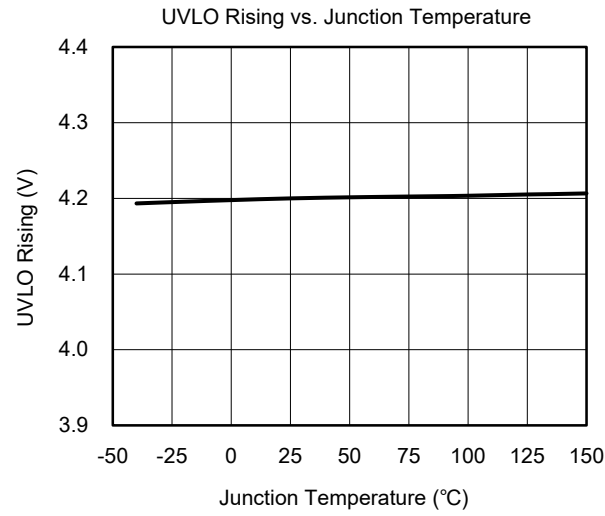| PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PH Pin					
Minimum On-Time	Measured at 90% to 90% of V_{IN}, I_{PH} = 2A		110		ns
Minimum Off-Time	$V_{(BOOT-PH)}$ ≥ 3.5V		90		ns
Switching Frequency					
Switching Frequency Range, SGM61233A		50		1500	kHz
	R_T = 100kΩ	450	480	510	kHz
	R_T = 1000kΩ	40	50	60	kHz
	R_T = 30kΩ	1330	1500	1620	kHz
Internal Switching Frequency, SGM61233B and SGM61233C		310	340	370	kHz

TYPICAL PERFORMANCE CHARACTERISTICS

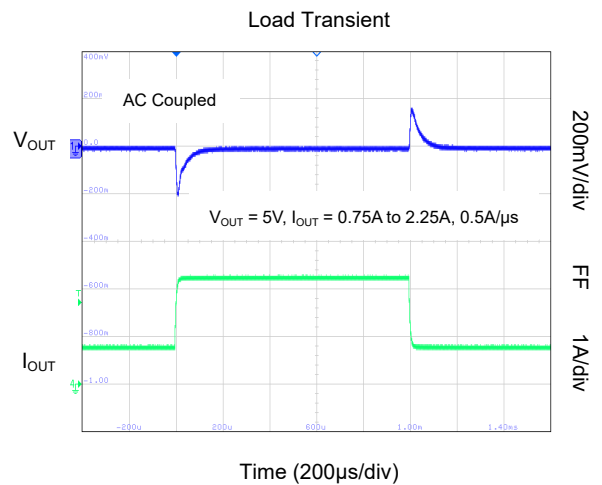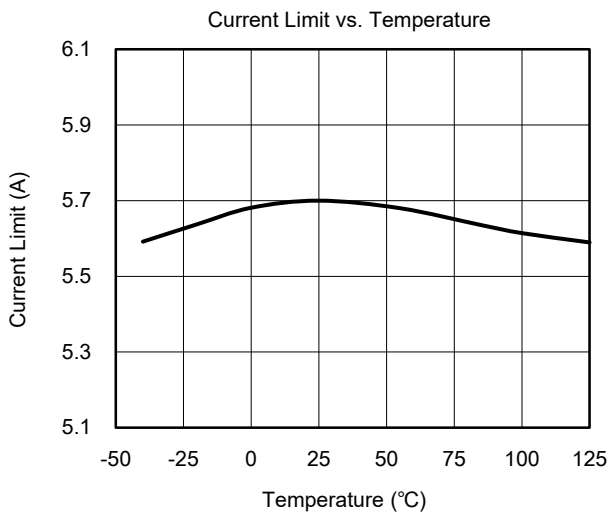T_A = +25℃, V_{IN} = 12V, f_{SW} = 340kHz, L = 15µH, and C_{OUT} = 94µF, unless otherwise noted.

Line Regulation vs. Input Voltage

V_{OUT} = 5V

I_{OUT} = 60mA
I_{OUT} = 1.5A
I_{OUT} = 3A

Load Regulation vs. Input Voltage

V_{OUT} = 5V

V_{IN} = 6V
V_{IN} = 12V
V_{IN} = 28V

Efficiency vs. Load Current

V_{OUT} = 5V

V_{IN} = 6V
V_{IN} = 9V
V_{IN} = 12V
V_{IN} = 20V
V_{IN} = 28V

Switching Frequency vs. RT/CLK Resistance

Quiescent Current vs. Junction Temperature

V_{IN} = 12V
V_{IN} = 28V

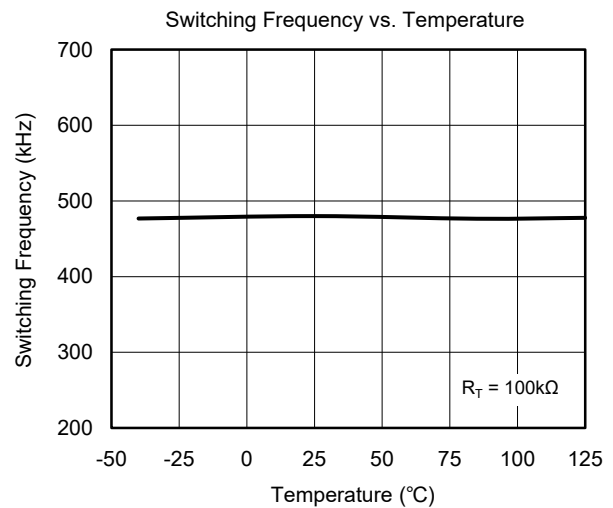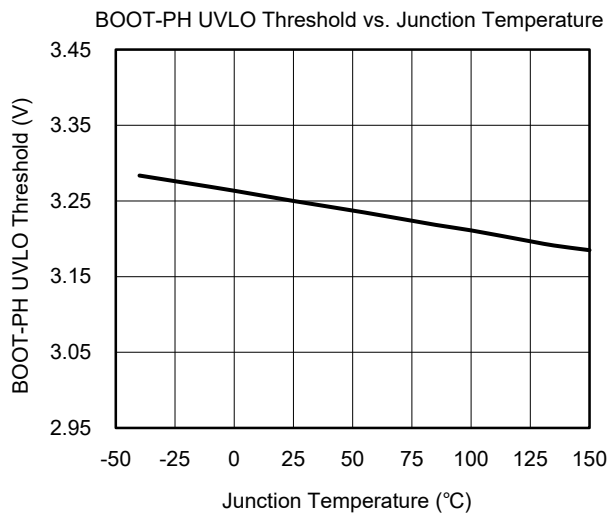Shutdown Current vs. Junction Temperature
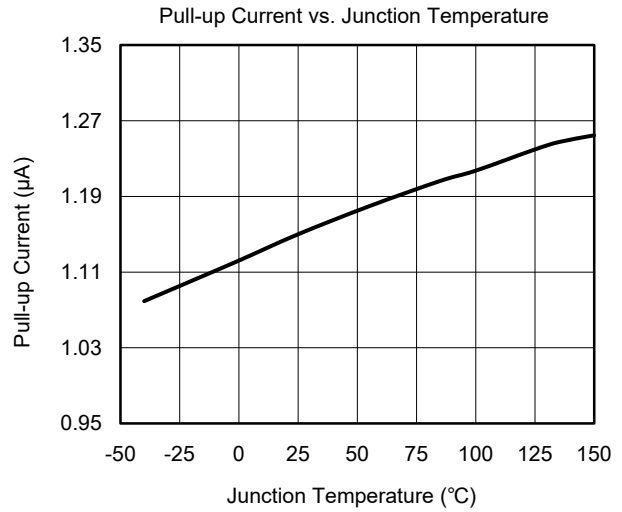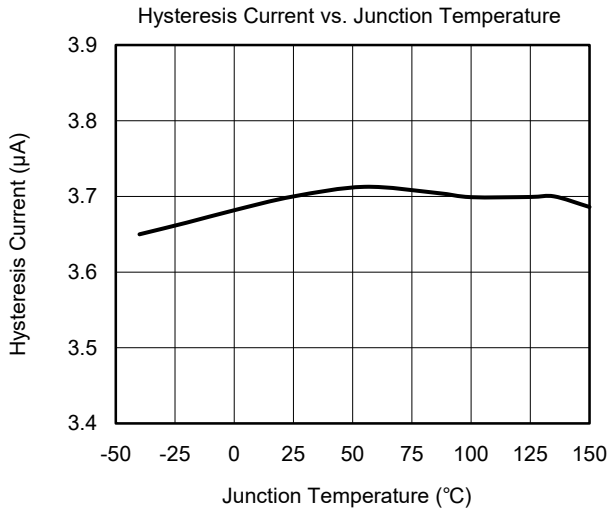
V_{IN} = 12V
V_{IN} = 28V

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, f_{SW} = 340kHz, L = 15µH, and C_{OUT} = 94µF, unless otherwise noted.

UVLO Rising vs. Junction Temperature

UVLO Hysteresis vs. Junction Temperature

Voltage Reference vs. Junction Temperature

High-side MOSFET On-Resistance vs. Junction Temperature

V_{BOOT_PH} = 5V

Low-side MOSFET On-Resistance vs. Junction Temperature

EN-UVLO Threshold vs. Junction Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

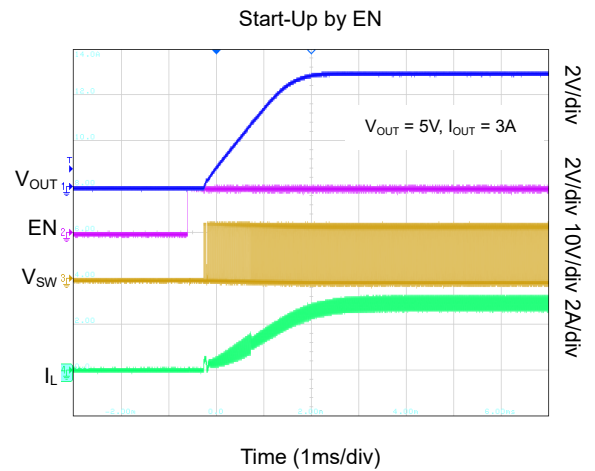T_A = +25℃, V_{IN} = 12V, f_{SW} = 340kHz, L = 15μH, and C_{OUT} = 94μF, unless otherwise noted.
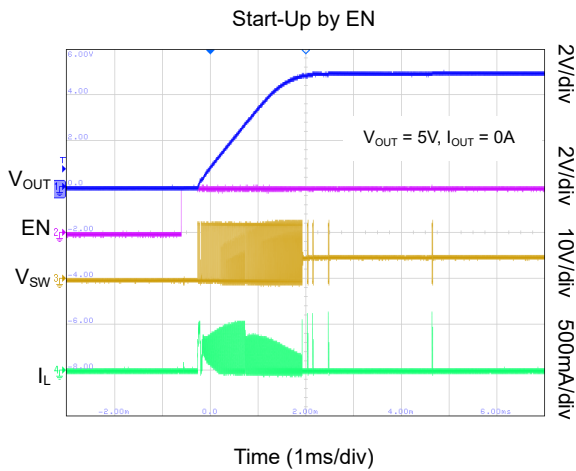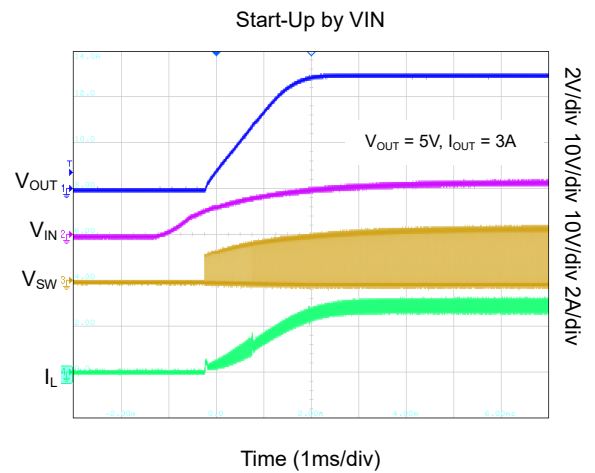
Hysteresis Current vs. Junction Temperature

Pull-up Current vs. Junction Temperature

BOOT-PH UVLO Threshold vs. Junction Temperature

Switching Frequency vs. Temperature

R_T = 100kΩ

Current Limit vs. Temperature

Load Transient

AC Coupled

V_{OUT}

200mV/div

V_{OUT} = 5V, I_{OUT} = 0.75A to 2.25A, 0.5A/μs

FF

I_{OUT}

1A/div

Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, f_{SW} = 340kHz, L = 15µH, and C_{OUT} = 94µF, unless otherwise noted.
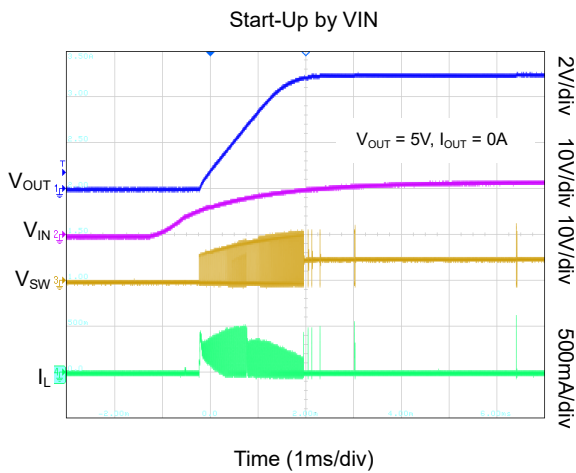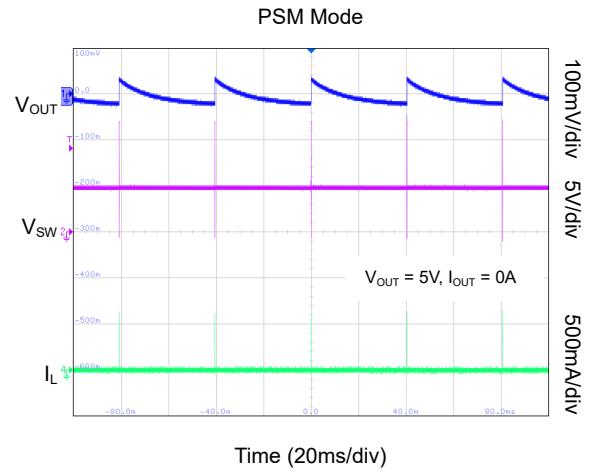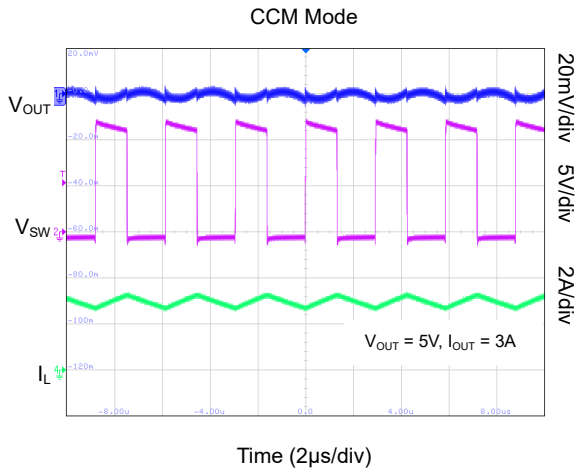
CCM Mode

V_{OUT} = 5V, I_{OUT} = 3A

Time (2µs/div)

PSM Mode

V_{OUT} = 5V, I_{OUT} = 0A

Time (20ms/div)

Start-Up by VIN

V_{OUT} = 5V, I_{OUT} = 0A

Time (1ms/div)

Start-Up by VIN

V_{OUT} = 5V, I_{OUT} = 3A

Time (1ms/div)

Start-Up by EN

V_{OUT} = 5V, I_{OUT} = 0A

Time (1ms/div)

Start-Up by EN

V_{OUT} = 5V, I_{OUT} = 3A

Time (1ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, f_{SW} = 340kHz, L = 15µH, and C_{OUT} = 94µF, unless otherwise noted.
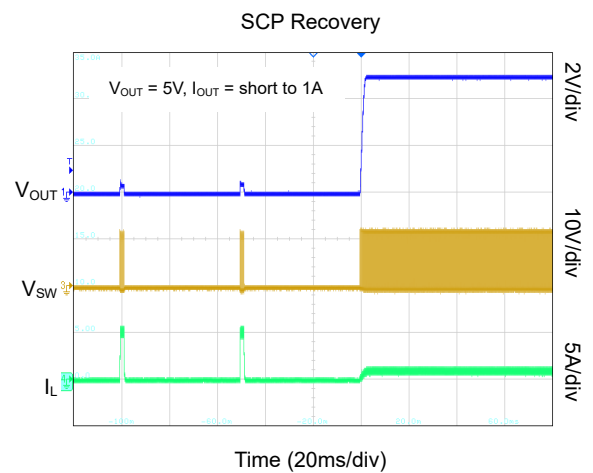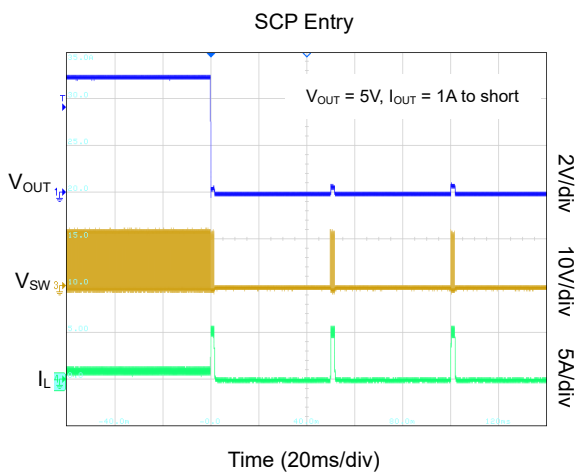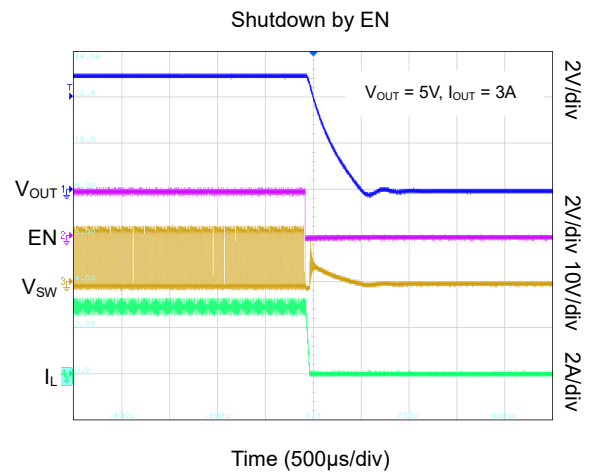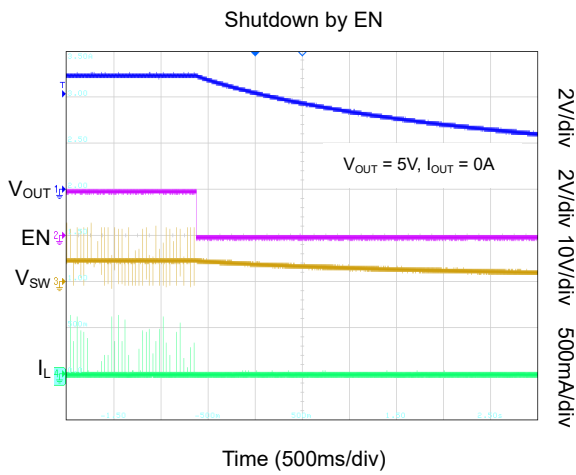
Shutdown by VIN

V_{OUT} = 5V, I_{OUT} = 0A

Time (50ms/div)

Shutdown by VIN

V_{OUT} = 5V, I_{OUT} = 3A

Time (500µs/div)

Shutdown by EN

V_{OUT} = 5V, I_{OUT} = 0A

Time (500ms/div)

Shutdown by EN

V_{OUT} = 5V, I_{OUT} = 3A

Time (500µs/div)

SCP Entry

V_{OUT} = 5V, I_{OUT} = 1A to short

Time (20ms/div)

SCP Recovery

V_{OUT} = 5V, I_{OUT} = short to 1A

Time (20ms/div)

FUNCTIONAL BLOCK DIAGRAM

Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61233 is a 28V synchronous Buck converter with two integrated N-MOSFETs and 3A continuous output current capabilit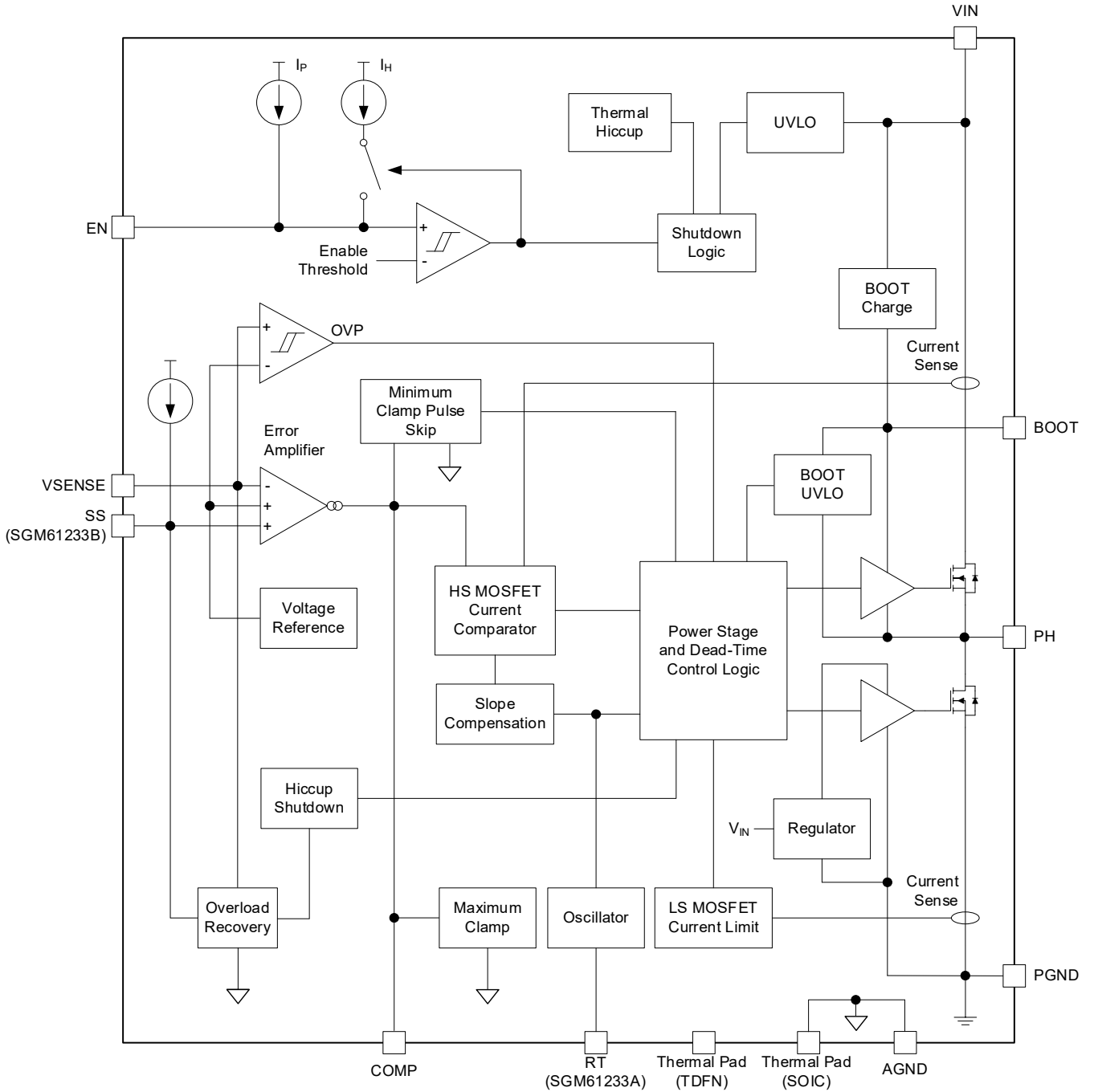y. Using peak current mode control provides the device good line and load transient responses with reduced output capacitance and simple compensation.

The minimum operating input voltage of the device is 4.5V. The output voltage can be set down to 0.8V (reference voltage). Typical no switching operating current is 320μA. The shutdown current is 2μA if the device is disabled. High efficiency is achieved through the integrated low R_{DSON} high-side switch (118mΩ) and low-side switch (81mΩ).

The EN pin is internally pulled up by a current source that can keep the device enable if EN pin is floating. It can also be used to increase the input UVLO threshold with a resistor divider.

The bootstrap diode is integrated and only a small capacitor (C_{BOOT}) between BOOT and PH pins is needed for the high-side MOSFET gate driving bias. A separate UVLO circuit monitors C_{BOOT} voltage and turns off the high-side switch if C_{BOOT} voltage falls below a preset threshold.

Additional features such as thermal shutdown, over-voltage protection, and short-circuit protection (hiccup mode) are also provided.

The SGM61233A has adjustable switching frequency from 50kHz to 1500kHz and a fixed internal 2ms soft-start time.

The SGM61233B has an internal current source on the SS pin that allows soft-start time to be adjusted with a small external capacitor. The device has a fixed 340kHz switching frequency.

The SGM61233C has a fixed 340kHz switching frequency and a fixed internal 2ms soft-start time.

Minimum Input Voltage (4.5V) and UVLO

The recommended minimum operating input voltage is 4.5V. It may operate with lower input voltages that are above the V_{IN} rising UVLO threshold (4.2V TYP). The V_{IN} UVLO threshold has a hysteresis of 270mV (TYP).

If V_{IN} falls below the falling UVLO voltage, the device will stop switching. If the EN pin is left floating or pulled high and V_{IN} exceeds the rising UVLO threshold, the device will start up with a soft-start.

Enable Input and UVLO Adjustment

The EN pin is able to control the device on or off. An internal pull-up current source keeps the EN pin voltage at high state by default. The EN pin can be pulled up to a voltage above its rising threshold or left floating to enable the device. The device will be disabled if the EN voltage is pulled externally below the falling threshold voltage.

If an application requires increasing the V_{IN} turn-on threshold and adding hysteresis to the V_{IN} UVLO, a voltage divider as shown in Figure 3 is required. When EN voltage exceeds V_{ENH} = 1.2V (TYP), an additional 3.7μA current is injected to the divider to provide hysteresis and it will be removed when EN pin voltage is below V_{ENL} = 1.13V (TYP). Use Equation 1 and 2 to calculate these resistors. V_{START} is the input start (turn-on) threshold voltage and V_{STOP} is the input stop (turn-off) threshold voltage.

$$R_{EN1} = \frac{V_{START}\left(\frac{V_{ENL}}{V_{ENH}}\right) - V_{STOP}}{1.15μA \times \left(1 - \frac{V_{ENL}}{V_{ENH}}\right) + 3.7μA} \tag{1}$$

$$R_{EN2} = \frac{R_{EN1} \times V_{ENL}}{V_{STOP} - V_{ENL} + R_{EN1}\left(1.15μA + 3.7μA\right)} \tag{2}$$
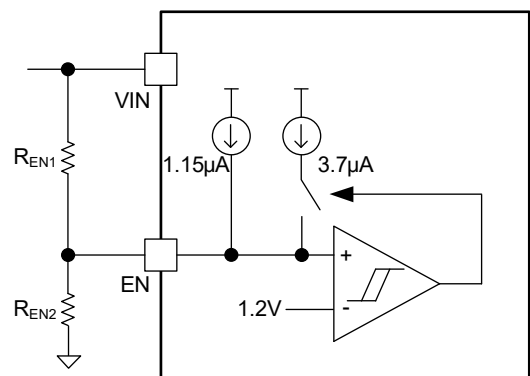

Figure 3. VIN UVLO Adjustment

DETAILED DESCRIPTION (continued)

Bootstrap Gate Driving (BOOT)

An internal regulator provides the bias voltage for gate driver using a 0.1µF ceramic capacitor. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor must have a 10V or higher voltage rating. When the voltage across the BOOT capacitor falls below the BOOT-PH UVLO (3.25V TYP), the high-side switch is turned off, and the low-side switch is turned on to recharge the BOOT capacitor.

RT Pin and Switching Frequency Adjustment (SGM61233A Only)

Several parameters such as losses, inductor and capacitors sizes and response time are considered in selection of the switching frequency. Higher frequency increases the switching and gate charge losses, and lower frequency requires larger inductance and capacitance, which can lead to larger overall physical size and higher costs. Therefore, a tradeoff is needed between losses and component size. If the application is noise-sensitive to a frequency range, the frequency should be selected out of that range.

The switching frequency of the SGM61233A can be set between 50kHz to 1500kHz using a resistor (R_T) placed between RT and AGND pins. Equation 3 can be used to determine R_T for a given switching frequency.

$$R_T \ (k\Omega) = 55300 \times f_{SW}^{-1.025} (kHz) \qquad (3)$$

SS Pin and Soft-Start Adjustment (SGM61233B Only)

The SGM61233B has an external soft-start (SS) pin for adjustable startup time. It is recommended to add a soft-start capacitor (C_{SS}) between SS pin and AGND to set the soft-start time. The lower of the SS pin voltage V_{SS} and V_{REF} is applied to the error amplifier to regulate the output. The internal I_{SS} = 2.4µA (TYP) current charges C_{SS} and provides a linear voltage ramp on the SS pin. Use Equation 4 to calculate the soft-start time.

$$t_{SS} \ (ms) = \frac{C_{SS} \ (nF) \times V_{REF} \ (V)}{I_{SS} \ (\mu A)} \qquad (4)$$

Error Amplifier (EA)

This device uses a transconductance amplifier as an error amplifier (EA) to compare the sensed output voltage (V_{SENSE}) with the internal reference. The gain of EA amplifier in normal operation is 1300µA/V (TYP). The output current is injected into the frequency compensation network (between COMP and GND pins) to produce the control signal (V_C) for the PWM comparator.

Slope Compensation

Without implementing some slope compensation, the PWM pulse widths will be unstable and oscillatory at duty cycles above 50%. To avoid sub-harmonic oscillations in this device, an internal compensation ramp is added to the measured switch current before comparing it with the control signal by the PWM comparator.

Power-Save Mode

To increase light load efficiency, power-save mode (PSM) feature is included in the SGM61233. When the COMP pin voltage (VC) is lower than 0.545V (TYP), the device will enter power-save mode. In this mode, the MOSFET switching is inhibited when VC falls below 0.545V. The device will exit PSM if VC rises above 0.545V.

Over-Current Protection

Over-current protection (OCP) is naturally provided by current mode control. In each cycle, the high-side (HS) current sensing starts a short time (blanking time) after the HS switch is turned on. The sensed HS switch current is continuously compared with the HS current limit threshold and when the HS current reaches to that threshold, the HS switch is turned off.

While the low-side (LS) switch is turned on, the conduction current is monitored by the internal circuitry. In each cycle, the sensed LS switch current is compared to the internally LS current limit threshold only when the HS current limit threshold is triggered. If the sensed LS switch current is higher than the LS current limit threshold during LS conduction, the HS does not turn on and the LS stays on when the clock signal comes. When the sensed LS switch current is below the LS current limit threshold, the HS switch turns on again at the next clock.

In addition, if an output overload condition occurs for more than 512 switching cycles, then the device shuts down and restarts after 16384 cycles.

DETAILED DESCRIPTION (continued)

Over-Voltage Protection

When an overload or an output fault condition is removed, large overshoot may occur on the output. The SGM61233 includes a protection circuit to reduce such over-voltage transients. If the voltage at the VSENSE pin exceeds 109% of the V_{REF} threshold, the high-side switch is turned off. When it returns below 106% of the V_{REF}, the high-side switch is allowed to turn on again.

Thermal Shutdown (TSD)

If the junction temperature (T_J) exceeds +175℃ (TYP), the TSD protection circuit will stop the switch from operating to protect the device from overheating. When the junction temperature drops below +165°C (TYP), the device will automatically restart after the built-in thermal shutdown hiccup time and executes the power-up procedure.

APPLICATION INFORMATION

The design method and component selection for the SGM61233 Buck converter are explained in this section. A typical application circuit for the SGM61233A is shown in Figure 4. It is used for converting a 7V to 28V supply voltage to a lower 5V output voltage with a maximum output current of 3A.

The external components are designed based on the application requirements and device stability. Some suitable parameters for different output voltages are provided in Table 1 to simplify the selection of components. The C_{OUT} values in Table 1 are actual derating values. Higher nominal values are used for ceramic capacitors.
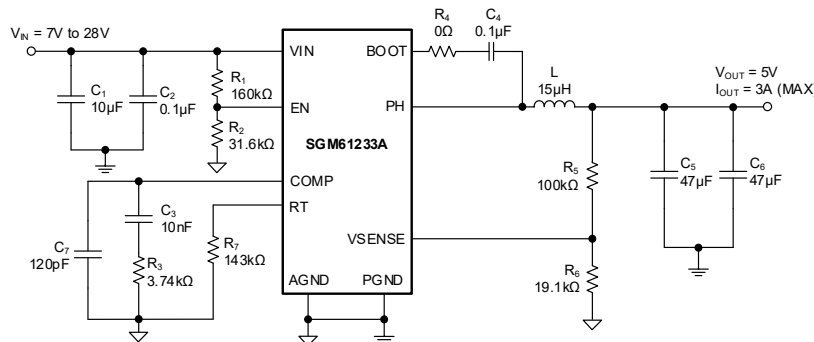
Typical Application

Figure 4. SGM61233A Typical Application Circuit

Table 1. Some Typical Parameters for Stable Operation

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R_5 (kΩ)	R_6 (kΩ)	R_3 (kΩ)	C_3 (nF)	C_7 (pF)
340	3.3	10	68	60.4	19.1	3.74	15	120
340	5	15	47	100	19.1	3.74	10	120
340	12	15	33	140	10	9.1	10	120
340	24	15	33	100	3.4	18	15	560

Requirements

The design parameters required for the design example are given in Table 2.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage	12V nominal
Start Input Voltage (Rising V_{IN})	7V
Stop Input Voltage (Falling V_{IN})	6V
Input Ripple Voltage	360mV, 3% of V_{IN_NOM}
Output Voltage	5V
Output Ripple Voltage	50mV, 1% of V_{OUT}
Output Current Rating	3A
Transient Response 1.5A to 3A Load Step	250mV, 5% of V_{OUT}
Operating Frequency	340kHz

Input Capacitors Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61233. At least 3µF of effective capacitance (after derating) is needed at the input. In some applications, additional bulk capacitance may also be required for the input, for example, when the SGM61233 is more than 5cm away from the input source. The input capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 5 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 3A, yields an RMS input ripple current of 1.5A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (5)$$

For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. Therefore, a 10µF/50V capacitor is selected for VIN to cover all DC bias, thermal and aging derating. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 6.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (6)$$

It is recommended to place an additional small size 0.1µF ceramic capacitor right beside VIN and PGND pins for high frequency filtering.

APPLICATION INFORMATION (continued)

Inductor Design

Equation 7 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor (K_{IND} = $\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions. For peak current mode converter, selecting an inductor with saturation current must be above the switch current limit. Typically, a 20% to 40% current ripple is selected (K_{IND} = 0.2 ~ 0.4).

$$L = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (7)$$

In this example, the calculated inductance will be 13.4µH with K_{IND} = 0.3, so the nearest larger inductance of 15µH is selected. The ripple, RMS and peak inductors current calculations are summarized in Equations 8, 9 and 10 respectively.

$$\Delta I_L = \frac{V_{IN\_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (8)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (9)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (10)$$

Output Capacitor Design

There are three main criteria that must be considered when designing the output capacitor (C_{OUT}): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect and respond to the output change.

Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 11 can be used to calculate the minimum output capacitance that is needed to supply a current step (ΔI_{OUT}) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT} (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (11)$$

where:

• ΔI_{OUT} is the change in output current.

• ΔV_{OUT} is the allowable change in the output voltage.

For example, if the acceptable transient from 1.5A to 3A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V and ΔI_{OUT} = 1.5A, the minimum required capacitance will be 35.3µF. Note that the impact of output capacitor ESR on the transient is not considered in Equation 11. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of ΔV_{OUT} transient.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 12 calculates the minimum capacitance required to keep the output-voltage overshoot to a desired value.

$$C_{OUT} > L \times \frac{I_{OUT\_H}^2 - I_{OUT\_L}^2}{(V_{OUT} + \Delta V_{OUT})^2 - V_{OUT}^2} \quad (12)$$

where:

• I_{OUT_H} is the output current under heavy loads.

• I_{OUT_L} is the output current under light loads.

APPLICATION INFORMATION (continued)

For example, if the acceptable transient from 3A to 1.5A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V, the minimum required capacitance will be 39.5µF.

Equation 13 can be used for the output ripple criteria and finding the minimum output capacitance needed. V_{OUT_RIPPLE} is the maximum acceptable ripple. In this example, the allowed ripple is 50mV that results in minimum capacitance of 6.6µF.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \qquad (13)$$

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 13. For a specific output capacitance value, use Equation 14 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement.

$$ESR_{COUT} < \frac{V_{OUT\_RIPPLE}}{\Delta I_L} - \frac{1}{8 \times f_{SW} \times C_{OUT}} \qquad (14)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, a 2 × 47µF/10V X5R ceramic capacitor with 3mΩ of ESR is used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 15 calculates the RMS current that the output capacitor must support.

$$I_{COUT\_RMS} = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{\sqrt{12} \times V_{IN\_MAX} \times L \times f_{SW}} \qquad (15)$$

Bootstrap Capacitor Selection

Use a 0.1µF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating for the bootstrap capacitor (C_4). It is recommended to add a resistor R_4 in series with C_4 to slow down switch-on speed of the HS switch and improve radiated EMI problems. For most applications, R_4 is used around 5~10Ω. Too high values for R_4 may cause insufficient C_4 charging in high duty-cycle applications. Slower switch switch-on speed will also increase switch losses and reduce efficiency.

UVLO Setting

The input UVLO can be programmed using an external voltage divider on the EN pin of the SGM61233. In this design, R_1 is connected between VIN and the EN pins

and R_2 is connected between EN and AGND pins (see Figure 4). The UVLO has two thresholds (hysteresis), one for power-up (turn-on) when the input voltage is rising and one for power-down or brownout (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above 7V (UVLO rising threshold). When the regulator is working, it will not stop switching until the input falls below 6V (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are R_1 = 160kΩ and R_2 = 31.6kΩ.

Switching Frequency

In order to make the parameter design match the internal setting frequency of SGM61233B and SGM61233C, the switching frequency of SGM61233A is set to 340kHz and R_7 = 140.6kΩ is calculated using Equation 3. For this example, the nearest lager standard resistor value is 143kΩ.

Feedback Resistors Setting

Use resistor dividers (R_5 and R_6) to set the output voltage through Equation 16 and 17.

$$R_6 = \frac{R_5 \times V_{REF}}{V_{OUT} - V_{REF}} \qquad (16)$$

$$V_{OUT} = V_{REF} \times \left(\frac{R_5}{R_6} + 1\right) \qquad (17)$$

It is recommended to choose R_5 around 100kΩ and calculate R_6 from Equation 16. Use accurate and stable resistors (1% or better) to enhance output accuracy. For this example, the selected values are R_5 = 100kΩ and R_6 = 19.1kΩ, resulting in a 4.988V output voltage.

Compensation Network Setting

Several techniques are used by engineers to compensate a DC/DC regulator. The method presented here uses simple calculations and generally results in high phase margins.
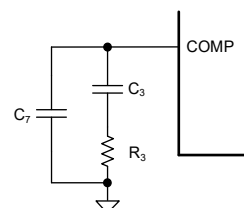

Figure 5. SGM61233 Typical Application Circuit

APPLICATION INFORMATION (continued)

One pole of the system is determined by the converter (C_{OUT} and R_{LOAD}), as given in Equation 18:

$$f_{P1} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} \qquad (18)$$

where R_{LOAD} is the load resistor and C_{OUT} is the output capacitor.

The system has two zeros. One is generated by the large ESR of C_{OUT} (ESR_{COUT}) and the other by the compensator (C_3 and R_3), as given in Equation 19 and Equation 20:

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR_{COUT}} \qquad (19)$$

$$f_{Z1} = \frac{1}{2\pi \times C_3 \times R_3} \qquad (20)$$

If the ESR of the output capacitor is large, the effect of this zero can be compensated by adding C_7 to the compensation network that places a third pole at:

$$f_{P3} = \frac{1}{2\pi \times C_7 \times R_3} \qquad (21)$$

The main goal of the compensation network is to adjust the shape of the converter transfer function to get a desired loop gain. The crossover frequency at which the loop gain is 1 (0dB) is an important factor that determines the bandwidth. Setting the crossover at a frequency that too high will lead to system instability.

At the beginning of the design, the crossover frequency is initially set to approximately 10% of the switching frequency ($0.1 \times f_{SW}$), and then the following steps are taken to design the compensation network with sufficient phase margin.

1. Select R_3 based on the desired crossover frequency (f_C):

$$R_3 = \frac{2\pi \times C_{OUT} \times f_C}{G_m \times G_{CS}} \times \frac{V_{OUT}}{V_{REF}} \qquad (22)$$

where G_m is the error-amplifier transconductance (G_m = 1300µA/V) and G_{CS} is the current-sense transconductance (G_{CS} = 8A/V).

2. Select C_3 to get sufficient phase margin. In the applications using typical inductor values, placing the compensation zero (f_{Z1}) at $f_{Z1} < 0.25 \times f_C$ would be sufficient and C_3 can be calculated as:

$$C_3 > \frac{4}{2\pi \times R_3 \times f_C} \qquad (23)$$

3. Use C_7 if the ESR zero is located below $f_{SW}/2$. This condition is valid if Equation 24 is true:

$$\frac{1}{2\pi \times C_{OUT} \times ESR_{COUT}} < \frac{f_{SW}}{2} \qquad (24)$$

In this case, choose C_7 from Equation 25 to set a pole (f_{P3}) over the ESR zero:

$$C_7 = \frac{C_{OUT} \times ESR_{COUT}}{R_3} \qquad (25)$$

Layout Information

Layout Considerations

Examples of PCB layouts for SGM61233A in SOIC and TDFN packages are provided in Figure 6 and Figure 7, respectively. These layouts have been shown to bring good results, although other layout designs may also obtain good performance.

• Bypass the VIN pin to PGND pin with low-ESR ceramic capacitors (10μF/X5R or better) and place them as close as possible to the device.

• Share the same PGND connection point with the input and output capacitors.

• Connect the device PGND to the PCB ground plane right at the PGND pin.

• Minimize the length and the area of the connection route from PH pin to the inductor to reduce the noise coupling from this area.

• Consider sufficient ground plane area on the top side for proper heat dissipation. Connect the large internal or back-side ground planes to the top-side ground near the device with thermal vias for better heat dissipation.
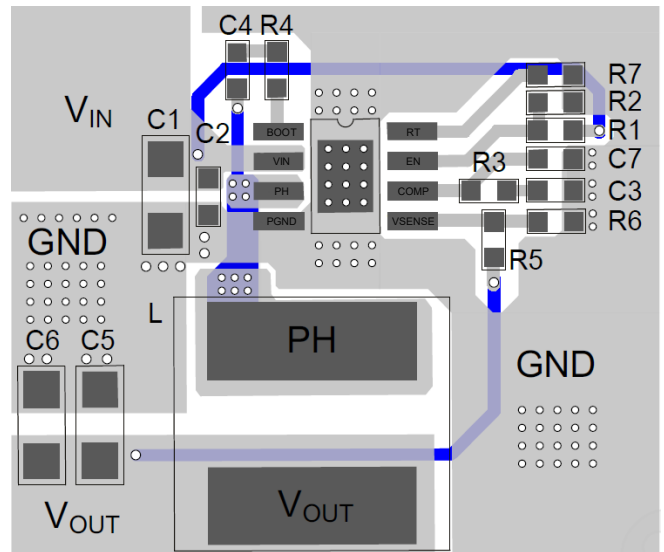
Layout Examples

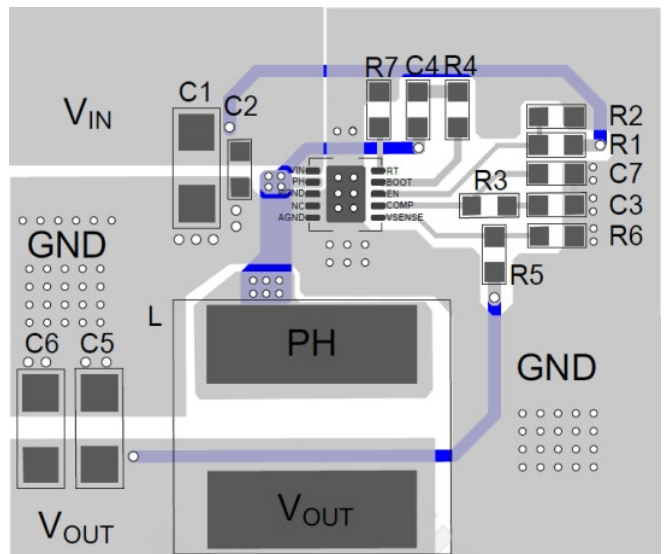**Figure 6. Example of PCB Layouts for SOIC-8 Package**

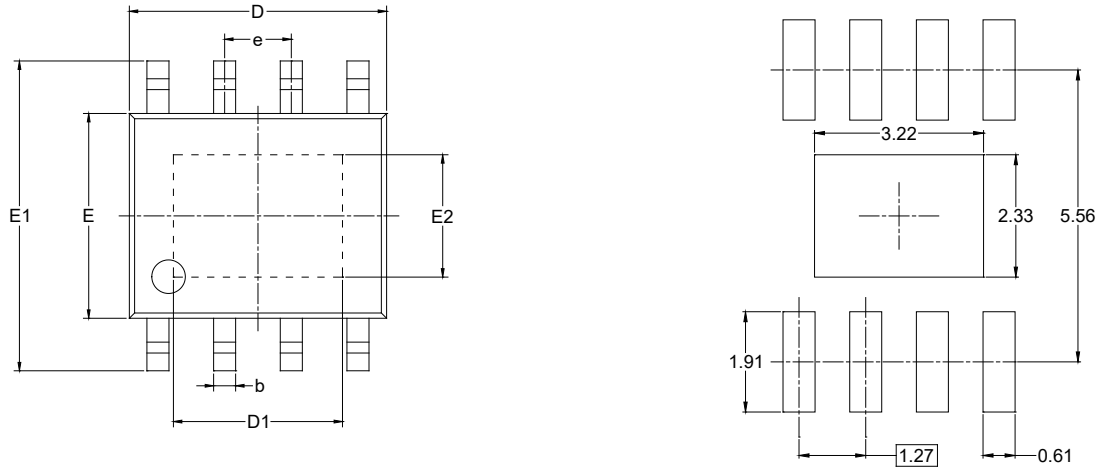**Figure 7. Example of PCB Layouts for TDFN Package**

REVISION HISTORY

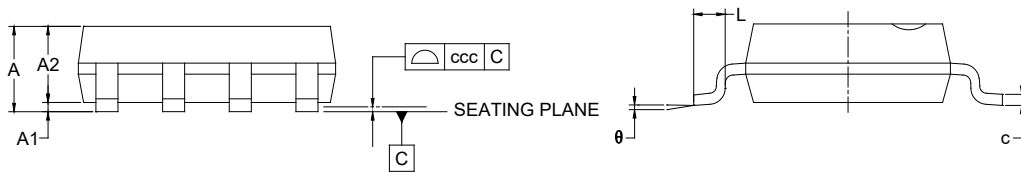NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (JULY 2023) to REV.A   **Page**

Changed from product preview to production data ....All

PACKAGE OUTLINE DIMENSIONS

SOIC-8 (Exposed Pad)

RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	**MOD**	**MAX**
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
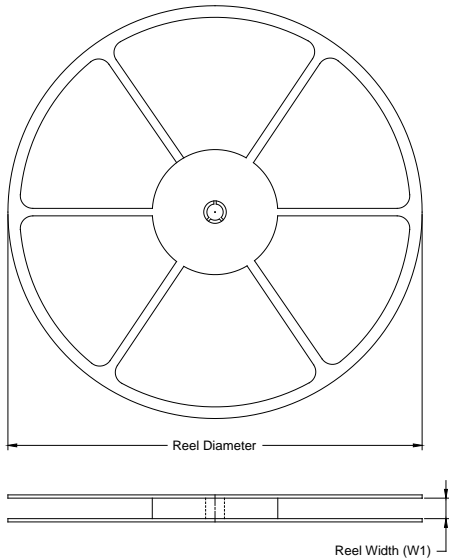3. Reference JEDEC MS-012.

PACKAGE OUTLINE DIMENSIONS

TDFN-3×3-10L

TOP VIEW

BOTTOM VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN (Unit: mm)
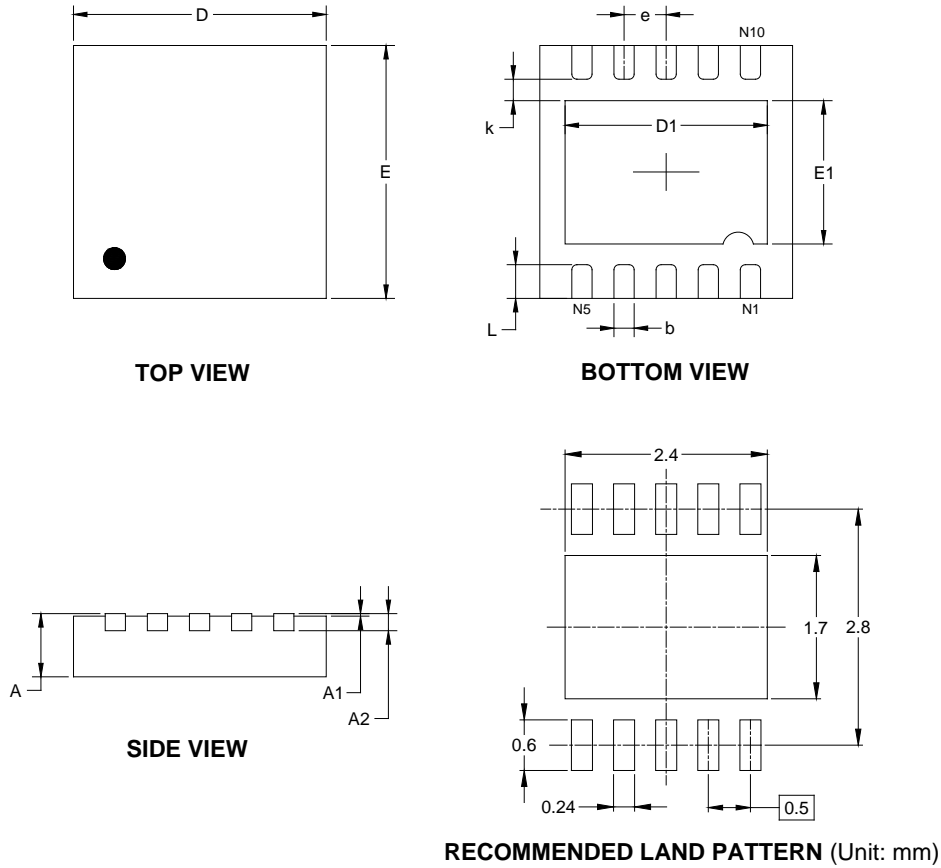
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

NOTE: This drawing is subject to change without notice.

TX00060.000

TAPE AND REEL INFORMATION

REEL DIMENSIONS
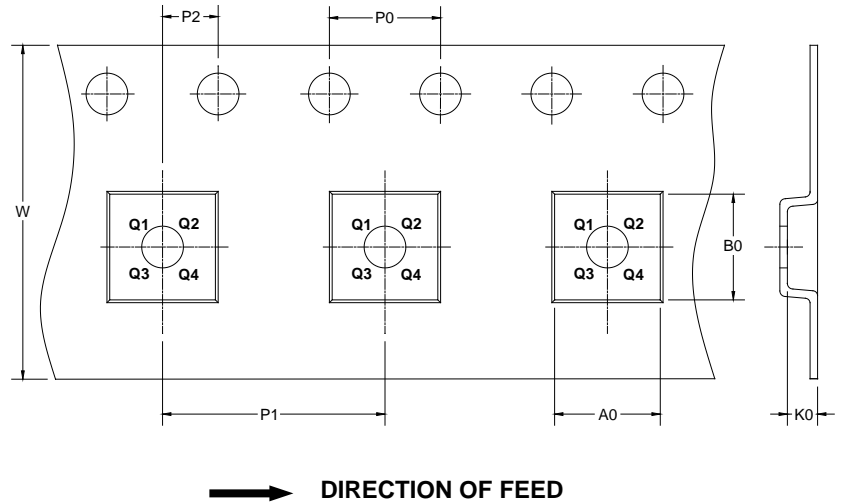
Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

DIRECTION OF FEED

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TDFN-3×3-10L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002