AOC2806

20V Common-Drain Dual N-Channel AlphaMOS

General Description

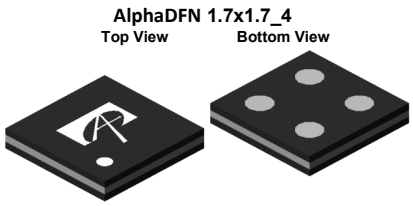
- Trench Power AlphaMOS (αMOS LV) technology
- Low $R_{SS(ON)}$
- With ESD protection to improve battery performance and safety
- Common drain configuration for design simplicity
- RoHS and Halogen-Free Compliant

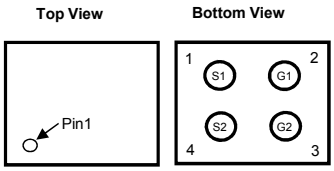
Applications

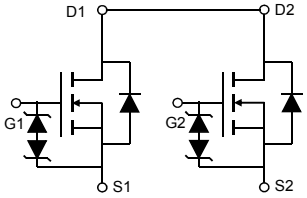
- Battery protection switch
- Mobile device battery charging and discharging

Product Summary

V_{SS}	20V
I_S (at V_{GS}=4.5V)	4.5A
$R_{SS(ON)}$ (at V_{GS}=4.5V)	< 18mΩ
$R_{SS(ON)}$ (at V_{GS}=4.0V)	< 20mΩ
$R_{SS(ON)}$ (at V_{GS}=3.7V)	< 21mΩ
$R_{SS(ON)}$ (at V_{GS}=3.1V)	< 23mΩ
$R_{SS(ON)}$ (at V_{GS}=2.5V)	< 29mΩ
Typical ESD protection	**HBM Class 3A**







Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOC2806	AlphaDFN 1.7x1.7_4	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Source-Source Voltage		V_{SS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Source Current(DC) Note1	T_A=25°C	I_S	4.5	A
Source Current(Pulse) Note2		I_{SM}	18	
Power Dissipation Note1	T_A=25°C	P_D	0.7	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient	t ≤ 10s	$R_{\theta JA}$	115	140	°C/W
Maximum Junction-to-Ambient	Steady-State		140	180	°C/W

Note 1. Mounted on 1in2 FR-4 board with 2oz. Copper.
Note 2. PW <300 µs pulses, duty cycle 0.5% max

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{SSS}	Source-Source Breakdown Voltage	I_S=250µA, V_{GS}=0V Test Circuit 6	20			V
I_{SSS}	Zero Gate Voltage Source Current	V_{SS}=20V, V_{GS}=0V Test Circuit 1			1	µA
		T_J=55°C			5	
I_{GSS}	Gate leakage current	V_{SS}=0V, V_{GS}=±10V Test Circuit 2			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{SS}=V_{GS}, I_S=250µA Test Circuit 3	0.5	0.85	1.3	V
$R_{SS(ON)}$	Static Source to Source On-Resistance	V_{GS}=4.5V, I_S=3A Test Circuit 4	10	15	18	mΩ
		T_J=125°C	14	20.5	25	
		V_{GS}=4.0V, I_S=3A Test Circuit 4	11	15.8	20	mΩ
		V_{GS}=3.7V, I_S=3A Test Circuit 4	11.5	16.3	21	mΩ
		V_{GS}=3.1V, I_S=3A Test Circuit 4	12.5	17.6	23	mΩ
		V_{GS}=2.5V, I_S=3A Test Circuit 4	14.5	21	29	mΩ
g_{FS}	Forward Transconductance	V_{SS}=5V, I_S=3A Test Circuit 3		16		S
V_{FSS}	Forward Source to Source Voltage	I_S=1A,V_{GS}=0V Test Circuit 5		0.68	1	V
DYNAMIC PARAMETERS						
R_g	Gate resistance	f=1MHz		2		KΩ
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{G1S1}=4.5V, V_{SS}=10V, I_S=3A		12.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{G1S1}=4.5V, V_{SS}=10V, R_L=3.3Ω, R_{GEN}=3Ω Test Circuit8		1.0		µs
t_r	Turn-On Rise Time			3.0		µs
$t_{D(off)}$	Turn-Off DelayTime			2.1		µs
t_f	Turn-Off Fall Time			8.8		µs

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

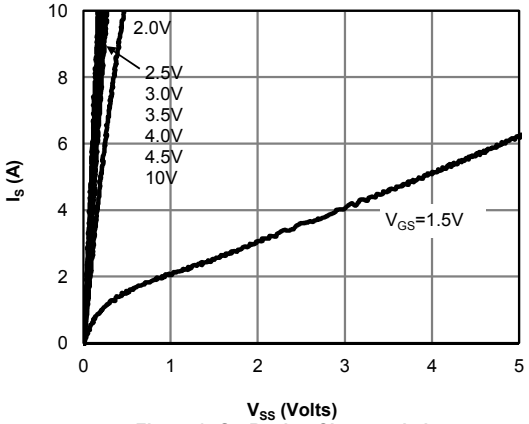


Figure 1: On-Region Characteristics

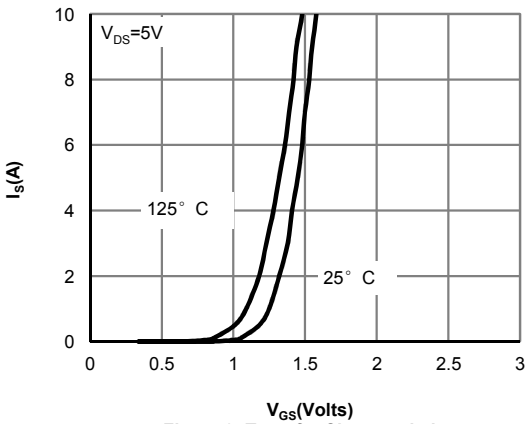


Figure 2: Transfer Characteristics

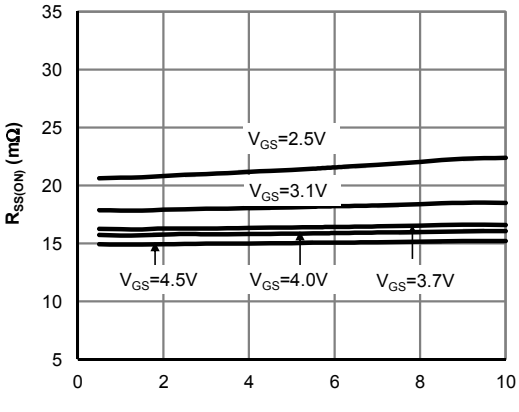


Figure 3: On-Resistance vs. Source Current and Gate Voltage

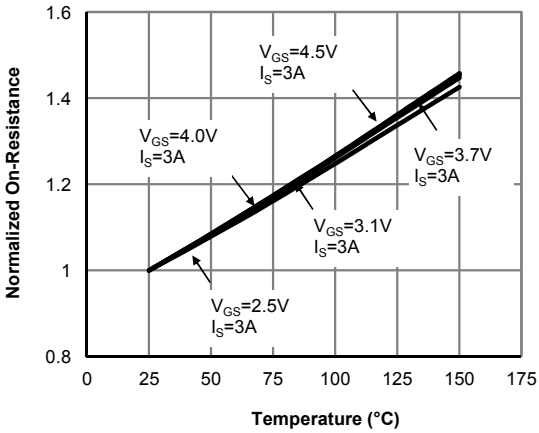


Figure 4: On-Resistance vs. Junction Temperature

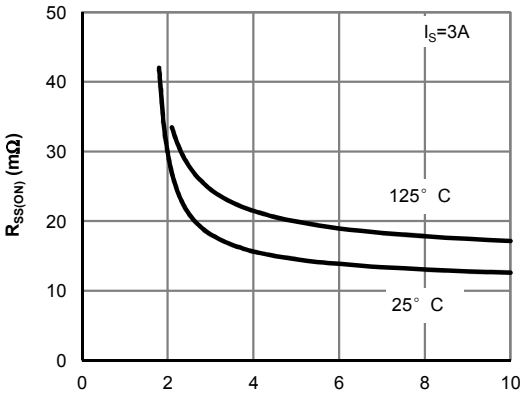


Figure 5: On-Resistance vs. Gate-Source Voltage

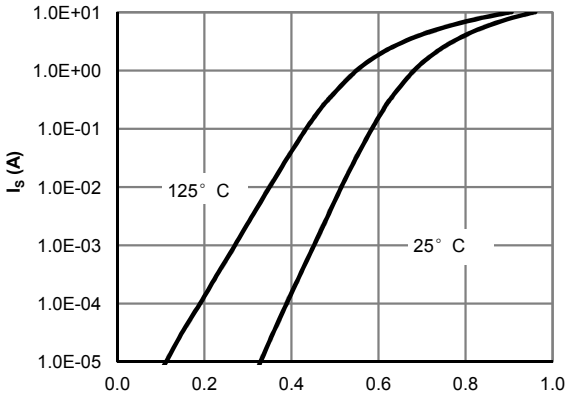


Figure 6: Forward Source to Source Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

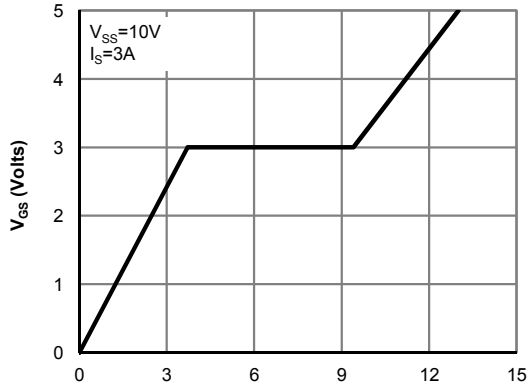


Figure 7: Gate-Charge Characteristics

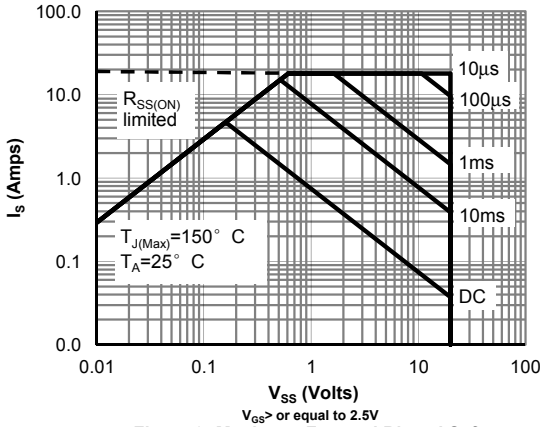


Figure 9: Maximum Forward Biased Safe Operating Area (Note1)

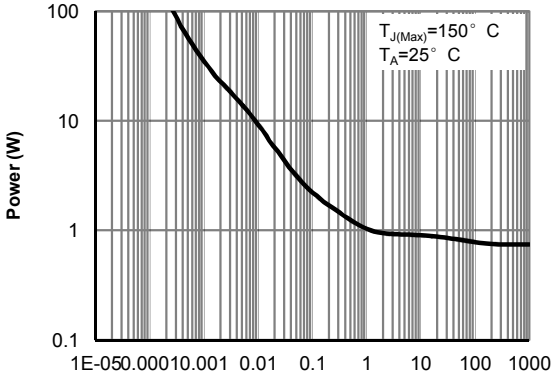


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note1)

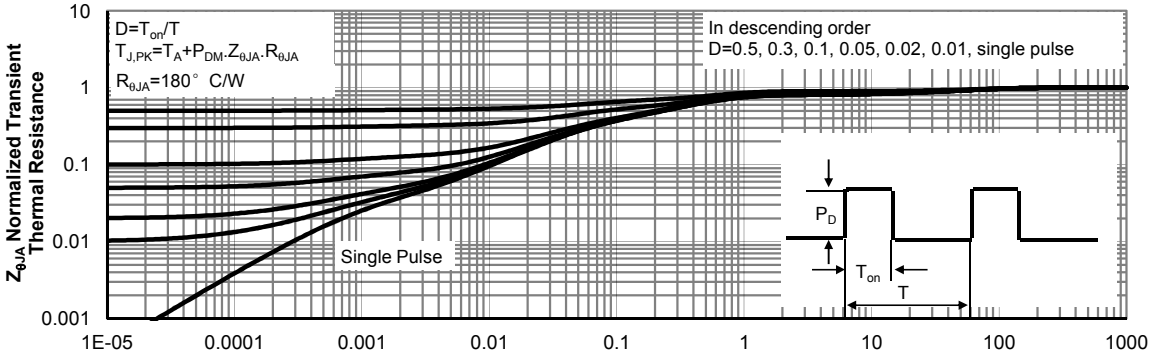
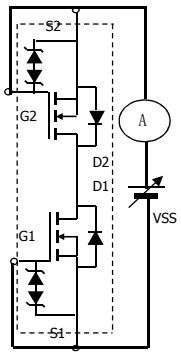


Figure 11: Normalized Maximum Transient Thermal Impedance (Note1)

TEST CIRCUIT 1 Isss

POSITIVE VSS FOR ISSS+

NEGATIVE VSS FOR ISSS-

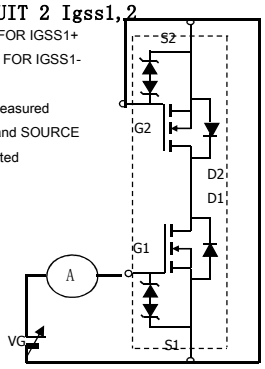


TEST CIRCUIT 2 Igss1,2

POSITIVE VGS FOR IGSS1+

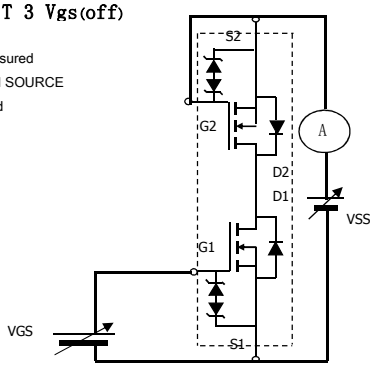
NEGATIVE VGS FOR IGSS1-

When FET1 is measured between GATE and SOURCE of FET2 are shorted



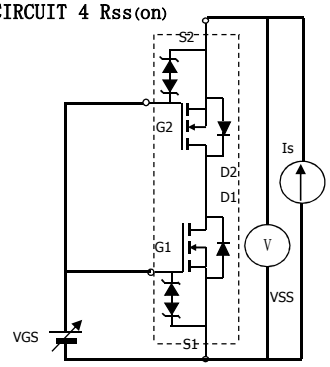
TEST CIRCUIT 3 Vgs(off)

When FET1 is measured between GATE and SOURCE of FET2 are shorted



TEST CIRCUIT 4 Rss(on)

Vss/Is

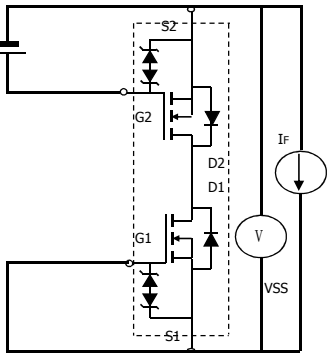


TEST CIRCUIT 5 $V_{F(GS)1,2}$

4.5V

When FET1 measured FET2 VGS=4.5V

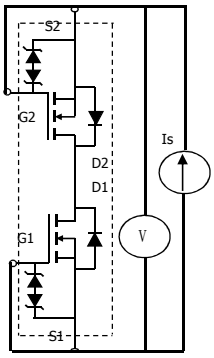
VGS=0



TEST CIRCUIT 6 BV_{DSS}

POSITIVE VSS FOR ISSS+

NEGATIVE VSS FOR ISSS-

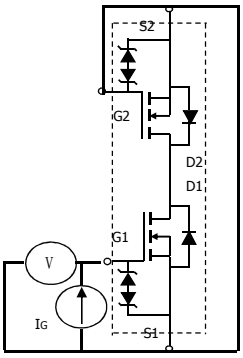


TEST CIRCUIT 7 $BV_{GSO1,2}$

POSITIVE VSS FOR ISSS+

NEGATIVE VSS FOR ISSS-

When FET1 is measured between GATE and SOURCE of FET2 are shorted



TEST CIRCUIT 8 Switching time