Product Summary

BV_{SSS}	$R_{SS(ON)\ MAX}$	I_S T_A = +25°C
30V	7.8mΩ @ V_{GS} =10V	14.6A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{SS(ON)}$) with a 3.37mm x 1.47mm x 0.2mm size and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Battery Management
- Load Switch
- Battery Protection

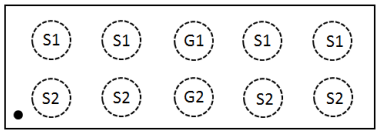
Features

- Built-in G-S Protection Diode Against ESD 2kV HBM.
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

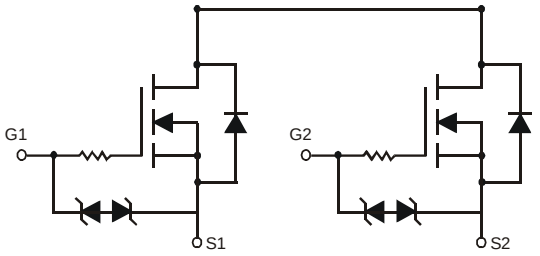
Mechanical Data

- Case: X4-DSN3415-10
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram

ESD PROTECTED TO 2kV



Top View



N-Channel N-Channel

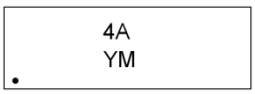
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMN3008SCP10-7	X4-DSN3415-10	3000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
3. For packaging details, go to our website at

Marking Information



4A = Product Type Marking Code
YM = Date Code Marking
Y or $\overline{Y}$ = Year (ex: E = 2017)
M or $\overline{M}$ = Month (ex: 9 = September)

Date Code Key

Year	2015	2016	2017	2018	2019	2020	2021
Code	C	D	E	F	G	H	I

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Source -Source Voltage			V_{SSS}	30	V
Gate-Source Voltage (Note 5)			V_{GSS}	±20	V
Continuous Source Current @ T_A = +25°C (Note 6)	Steady State	T_A = +25°C T_A = +70°C	I_S	14.6 11.6	A
Pulsed Source Current @ T_A = +25°C (Notes 6 & 7)			I_{SM}	80	A

Thermal Characteristics

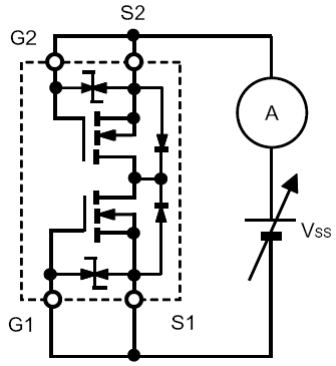
Characteristic	Symbol	Value	Unit
Power Dissipation, @ T_A = +25°C (Note 6)	P_D	2.7	W
Thermal Resistance, Junction to Ambient @T_A = +25°C (Note 6)	$R_{\theta JA}$	46.9	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

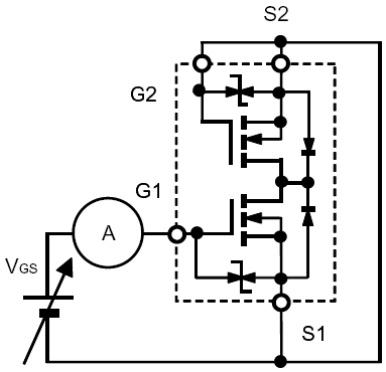
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Source to Source Breakdown Voltage T_J = +25°C	BV_{SSS}	30	—	—	V	I_S = 250μA, V_{GS} = 0V TEST CIRCUIT 1
Zero Gate Voltage Source Current T_J = +25°C	I_{SSS}	—	—	1.0	μA	V_{SS} = 24V, V_{GS} = 0V TEST CIRCUIT 1
Gate-Body Leakage	I_{GSS}	—	—	10	μA	V_{GS} = ±20V, V_{DS} = 0V TEST CIRCUIT 2
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	1.3	1.6	2.3	V	V_{SS} = 10V, I_S = 250μA TEST CIRCUIT 3
Static Source -Source On-Resistance	$R_{SS(ON)}$	—	6.1 8.1	7.8 11	mΩ	V_{GS} = 10 V, I_S = 7.0A TEST CIRCUIT 5 V_{GS} = 4.5V, I_S = 7.0A TEST CIRCUIT 5
Body Diode Forward Voltage	$V_{F(S-S)}$	—	0.8	—	V	I_F = 7.0A, V_{GS} = 0V, TEST CIRCUIT 6
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1476	—	pF	V_{SS} = 15V, V_{GS} = 0V, f = 1.0MHz TEST CIRCUIT 7
Output Capacitance	C_{oss}	—	204	—		
Reverse Transfer Capacitance	C_{rss}	—	97	—		
Gate Resistance	R_g	—	436.8	—	Ω	V_{SS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (10V)	Q_g	—	31.3	—	nC	V_{SS} = 15V, I_S = 7A TEST CIRCUIT 9
Total Gate Charge (4.5V)	Q_g	—	15.8	—	nC	
Gate-Source Charge	Q_{gs}	—	4.7	—	nC	
Gate-Drain Charge	Q_{gd}	—	6.3	—	nC	
Gate Charge at V_{TH}	$Q_{g(TH)}$	—	3.1	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	186	—	ns	V_{SS} = 15V, R_L = 2.1Ω, I_S = 7A TEST CIRCUIT 8
Turn-On Rise Time	t_R	—	314	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	928	—	ns	
Turn-Off Fall Time	t_F	—	858	—	ns	

Notes:
5. AEC-Q101 V_{GS} maximum is 16V.
6. Device mounted on FR-4 material with 1inch^2 (6.45cm^2), 2oz (0.071mm thick) Cu.
7. Repetitive rating, pulse width limited by junction temperature.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to production testing.

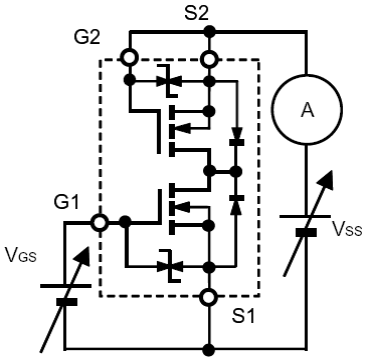
Test Circuits



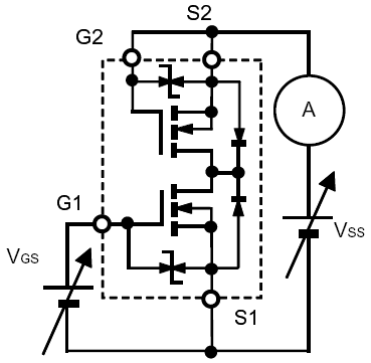
TEST CIRCUIT 1 I_{SSS}



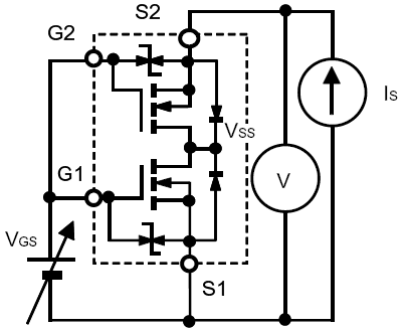
TEST CIRCUIT 2 I_{GSS}
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



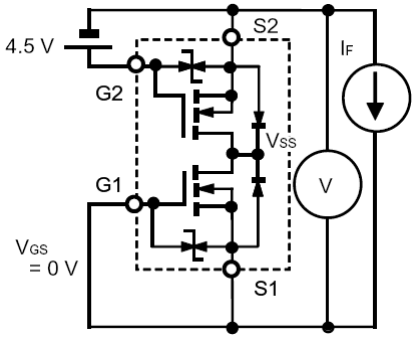
TEST CIRCUIT 3 $V_{GS(OFF)}$
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



TEST CIRCUIT 4 $|y_{fs}|$
$\Delta I_S/\Delta V_{GS}$

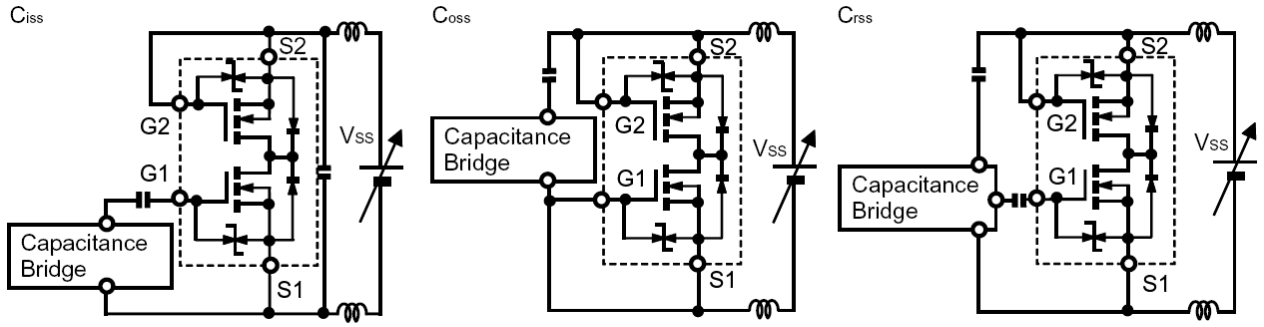


TEST CIRCUIT 5 $R_{SS(ON)}$
V_{SS}/I_S

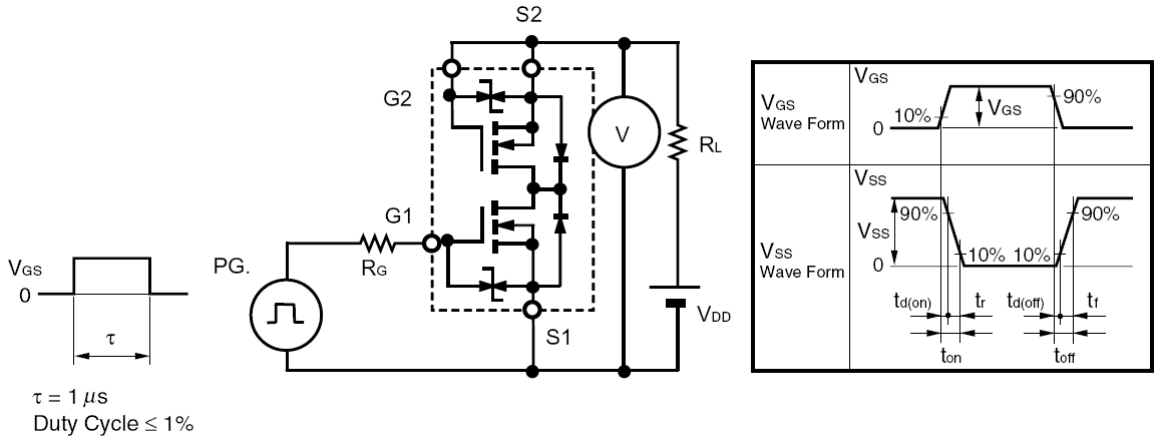


TEST CIRCUIT 6 $V_{F(S-S)}$
When FET1 is measured, FET2 is added V_{GS} +4.5V.

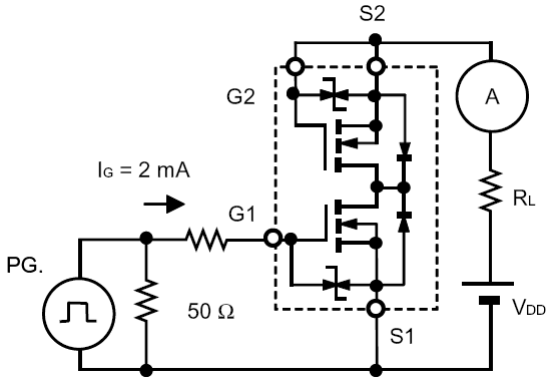
Test Circuits (Cont.)



TEST CIRCUIT 7



TEST CIRCUIT 8 $t_{d(on)}$, t_r, $t_{d(off)}$, t_f



TEST CIRCUIT 9 Q_G

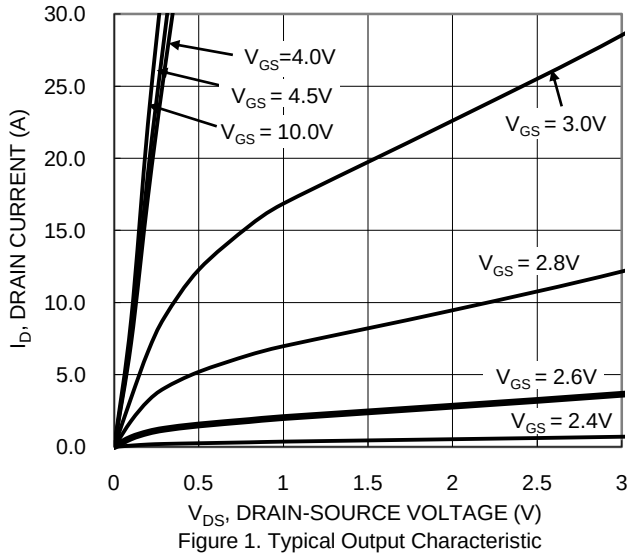


Figure 1. Typical Output Characteristic

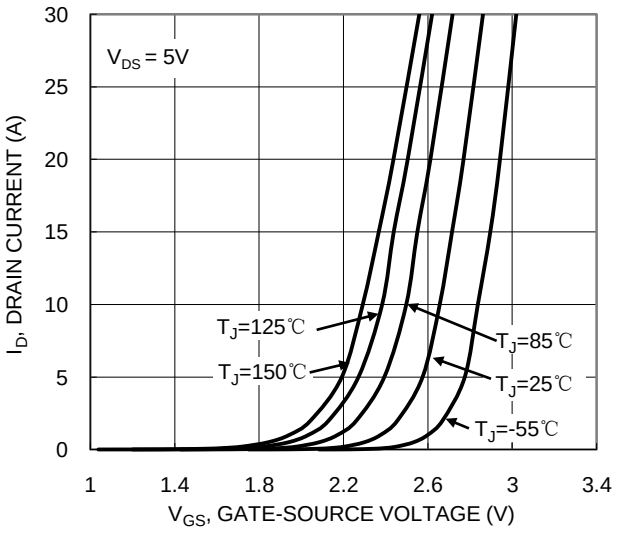


Figure 2. Typical Transfer Characteristic

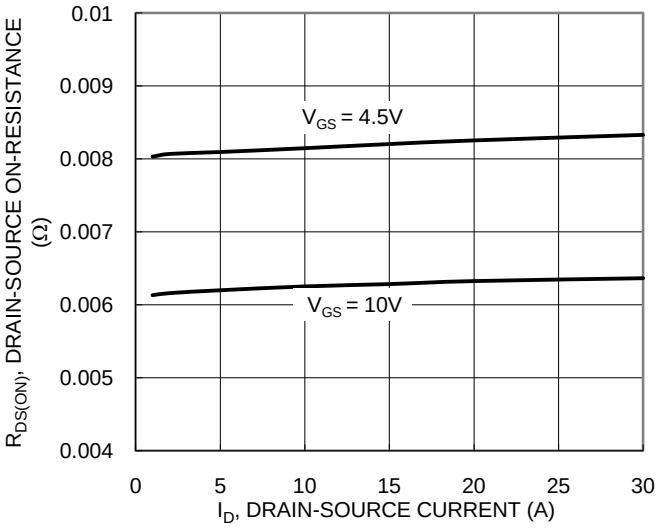


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

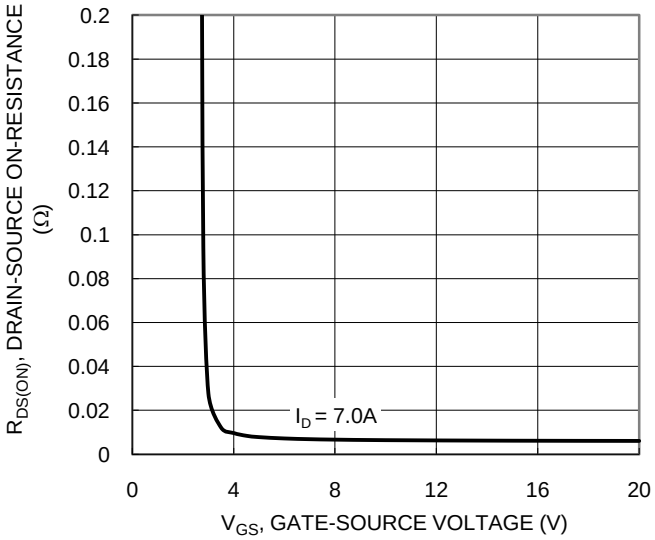


Figure 4. Typical Transfer Characteristic

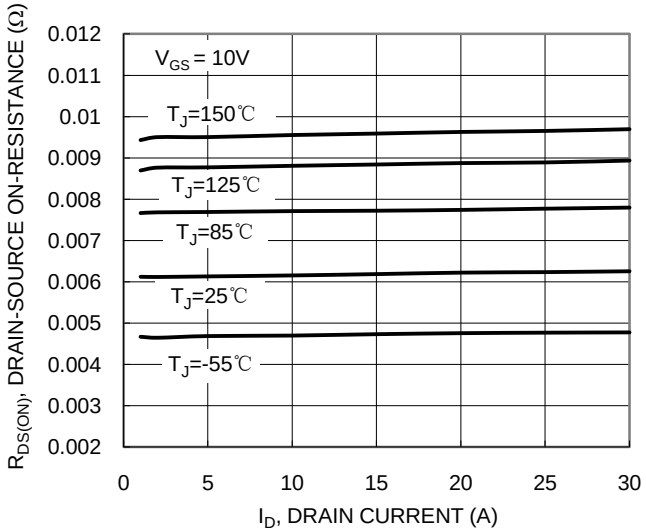


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

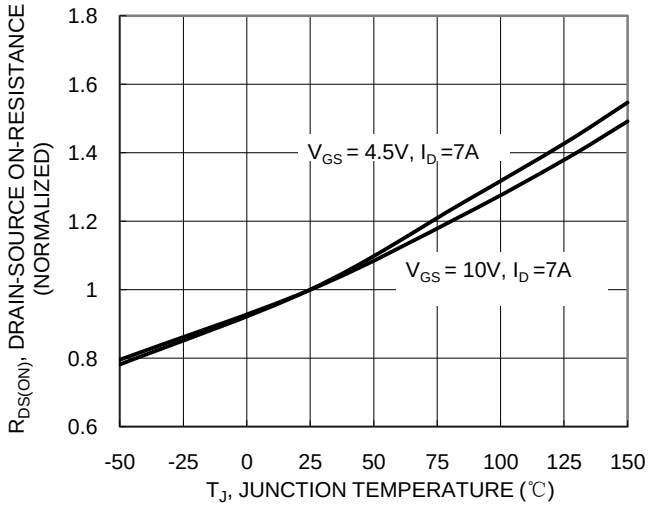


Figure 6. On-Resistance Variation with Junction Temperature

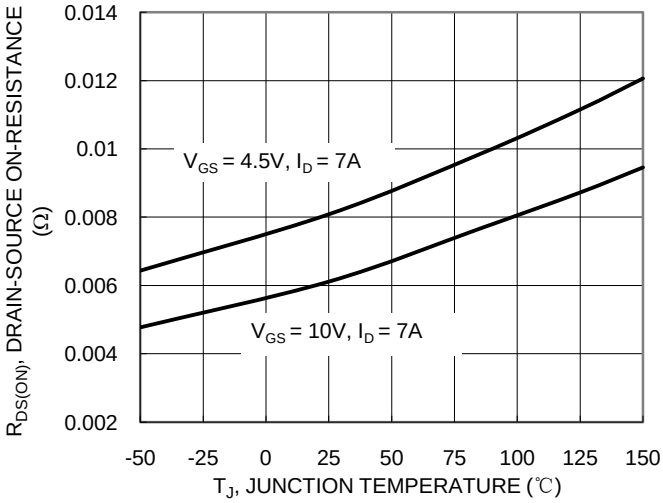


Figure 7. On-Resistance Variation with Junction Temperature

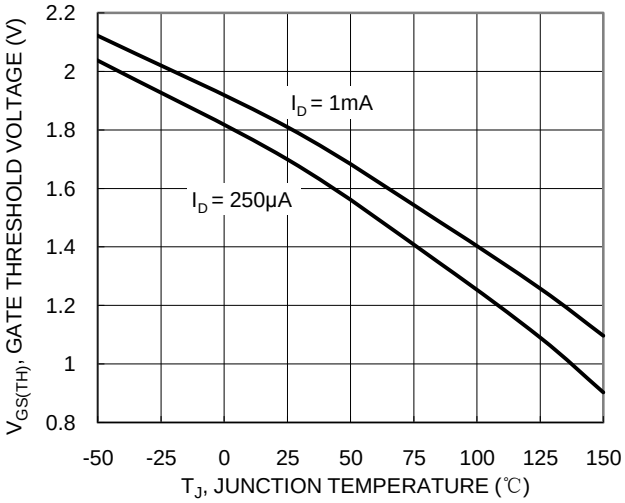


Figure 8. Gate Threshold Variation vs. Junction Temperature

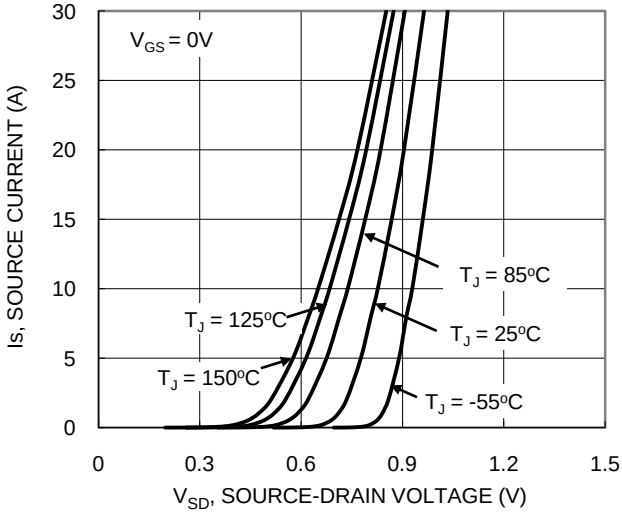


Figure 9. Diode Forward Voltage vs. Current

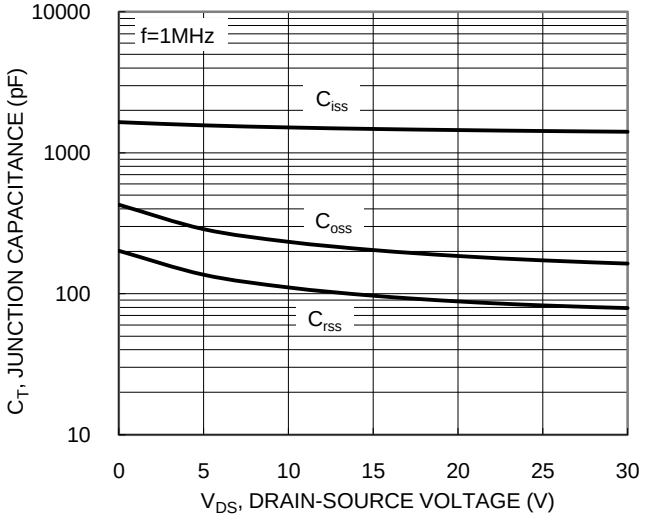


Figure 10. Typical Junction Capacitance

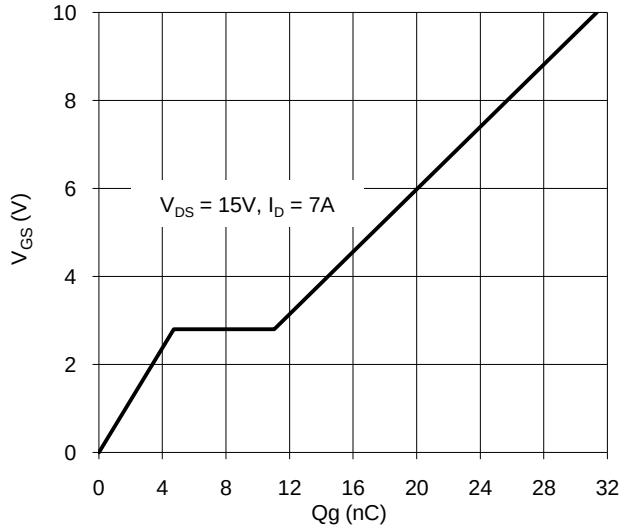


Figure 11. Gate Charge

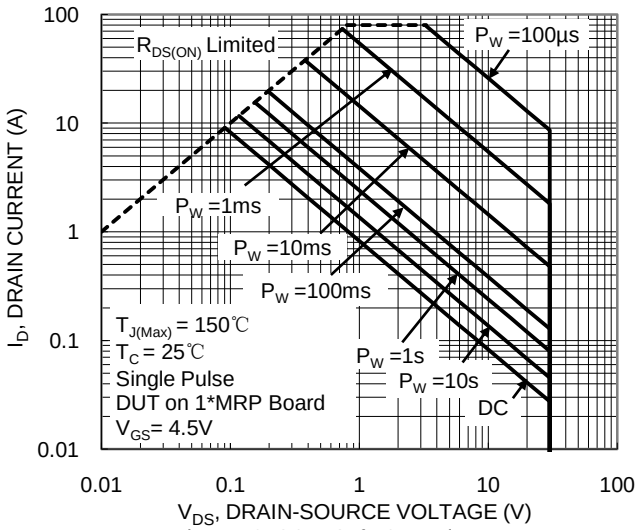


Figure 12. SOA, Safe Operation Area

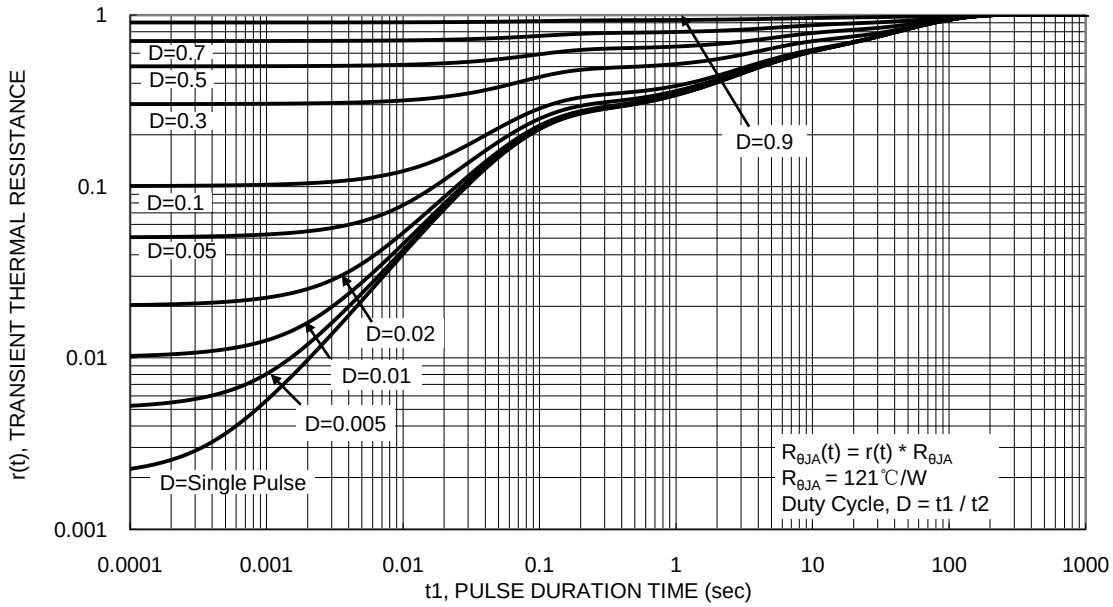
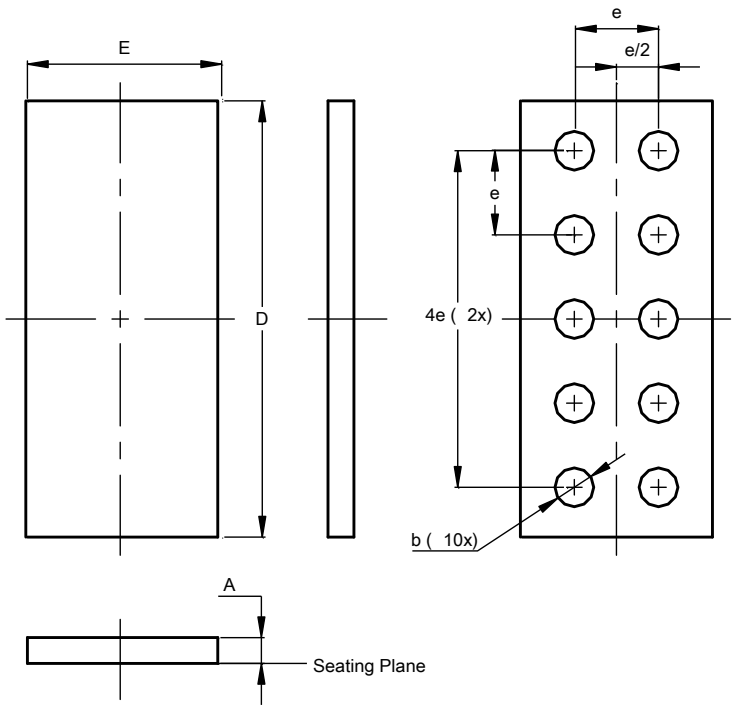


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X4-DSN3415-10

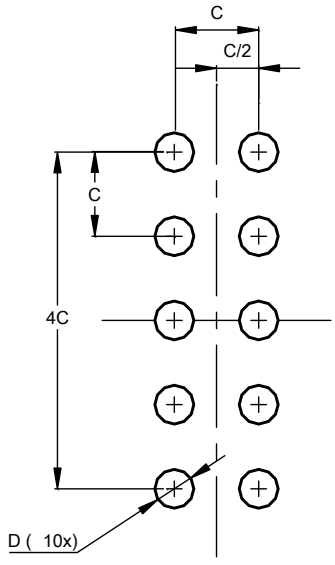


X4-DSN3415-10			
Dim	**Min**	**Max**	**Typ**
A	0.18	0.22	0.20
b	0.27	0.33	0.30
D	3.32	3.42	3.37
E	1.42	1.52	1.47
e	--	--	0.65
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X4-DSN3415-10



Dimensions	Value (in mm)
C	0.65
D	0.30