Description

The NDA345FA integrates a MOSFET driver, high-side MOSFET and low-side MOSFET into a single package.
The driver and MOSFETs have been optimized for high-current DC−DC buck power conversion applications. The NDA345FA integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 45 A.
- Capable of Switching at Frequencies up to 2 MHz.
- Capable of Peak Currents up to 75 A.
- Compatible with 3.3 V or 5 V PWM Input.
- Responds Properly to 3-level PWM Inputs.
- Option for Zero Cross Detection with 3-level PWM.
- Internal Bootstrap Diode.
- Undervoltage Lockout.
- Supports Intel® Power State 4.
- Thermal Warning output.
- Thermal Shutdown.

Applications

- Desktop & Notebook Microprocessors V−Core and Non−V−Core DC−DC Converters.

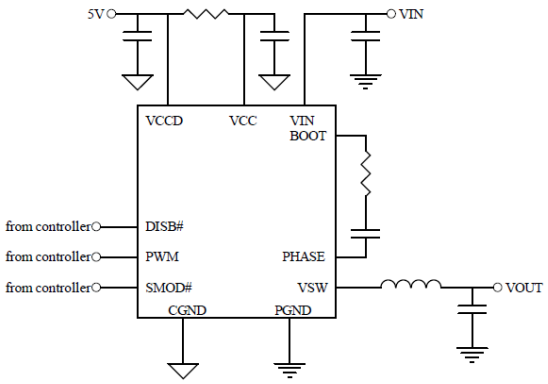
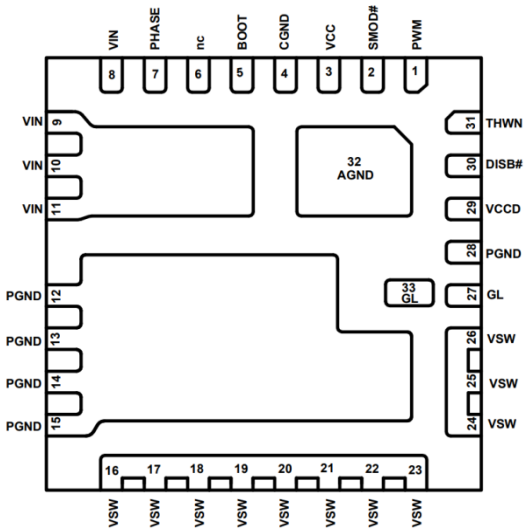


Figure 1. Application Schematic



PINOUT DIAGRAM

Table 1. PIN LIST AND DESCRIPTIONS

Pin No.	Symbol	Description
1	PWM	PWM Control Input and Zero Current Detection Enable
2	SMOD#	Skip Mode pin. 3-state input (see Table 1 LOGIC TABLE): SMOD# = High → State of PWM determine whether the NDA345FA performs ZCD or not. SMOD# = Mid → Connects PWM to internal resistor divider placing a bias voltage on PWM pin. Otherwise, logic is equivalent to SMOD# in the high state. SMOD# = Low → Placing PWM into mid-state pulls GH and GL low without delay. There is an internal pull-up resistor to VCC on this pin.
3	VCC	Control Power Supply Input
4,32	CGND, AGND	Signal Ground (pin 4 and pad 32 are internally connected)
5	BOOT	Bootstrap Voltage
6	nc	Open pin (not used)
7	PHASE	Bootstrap Capacitor Return
8-11	VIN	Conversion Supply Power Input
12-15,28	PGND	Power Ground
16-26	VSW	Switch Node Output
27,33	GL	Low Side FET Gate Access (pin 27 and pad 33 are internally connected)
29	VCCD	Driver Power Supply Input
30	DISB#	Output disable pin. When this pin is pulled to a logic high level, the driver is enabled. There is an internal pull-down resistor on this pin.
31	THWN	Thermal warning indicator. This is an open-drain output. When the temperature at the driver die reaches TTHWN, this pin is pulled low.

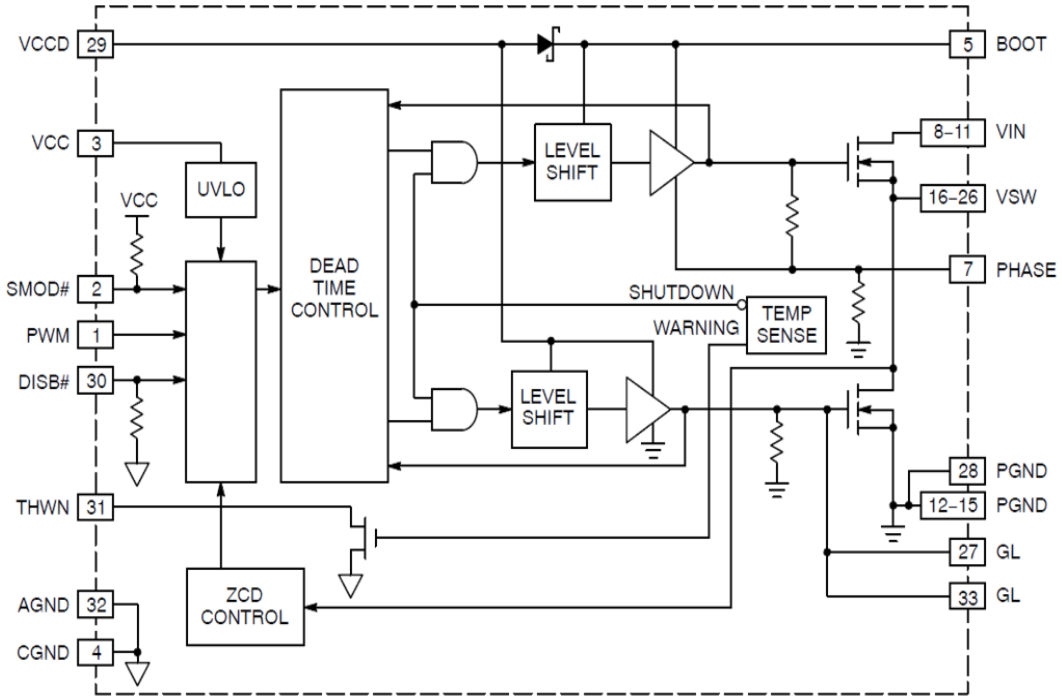


Figure 2. Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS (Electrical Information-all signals referenced to PGND unless noted otherwise)

Pin Name/Parameter	Min	Max	Unit
VCC, VCCD	-0.3	6.5	V
VIN	-0.3	30	V
BOOT (DC)	-0.3	35	V
BOOT (< 20 ns)	-0.3	40	V
BOOT to PHASE (DC)	-0.3	6.5	V
VSW, PHASE (DC)	-0.3	30	V
VSW, PHASE (< 5 ns)	-5	37	V
All Other Pins	-0.3	V_{VCC} + 0.3	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance	θ_{JA}	12.4	℃/W
	θ_{J-PCB}	1.8	℃/W
Operating Junction Temperature Range (Note 1)	T_J	-40 to +150	℃
Operating Ambient Temperature Range	T_A	-40 to +125	℃
Maximum Storage Temperature Range	T_{STG}	-55 to +150	℃
Maximum Power Dissipation		10.5	W
Moisture Sensitivity Level	MSL	1	

1. The maximum package power dissipation must be observed.
2. JESD 51−5 (1S2P Direct-Attach Method) with 0 LFM.
3. JESD 51−7 (1S2P Direct-Attach Method) with 0 LFM.

Table 4. RECOMMENDED OPERATING CONDITIONS

Parameters	Pin Name	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage Range	VCC, VCCD		4.5	5.0	5.5	V
Conversion Voltage	VIN		4.5	12	20	V
Continuous Output Current		F_{SW} = 1 MHz, V_{IN} = 12 V, V_{OUT} = 1.0 V, T_A = 25°C			40	A
		F_{SW} = 300 kHz, V_{IN} = 12 V, V_{OUT} = 1.0 V, T_A = 25°C			45	A
Peak Output Current		F_{SW} = 500 kHz, V_{IN} = 12 V, V_{OUT} = 1.0 V, Duration = 10 ms, Period = 1 s, T_A = 25°C			75	A
Junction Temperature			-40		125	℃

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS

(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 µF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
VCC SUPPLY CURRENT						
Operating		DISB# = 5 V, PWM = 400 kHz		1	2	mA
No switching		DISB# = 5 V, PWM = 0 V			2	mA
Disabled		DISB# = 0 V, SMOD# = VCC		0.4	1	uA
		DISB# = 0 V, SMOD# = GND		6	13	uA
UVLO Start Threshold	V_{UVLO}	VCC Rising	2.9		3.3	V
UVLO Hysteresis			150			mV
VCCD SUPPLY CURRENT						
Enabled, No Switching		DISB# = 5 V, PWM = 0 V, V_{PHASED} = 0 V		175	300	uA
Disabled		DISB# = 0 V		0.4	1	uA
Operating		DISB# = 5 V, PWM = 400 kHz			20	mA
DISB# INPUT						
Input Resistance		To Ground		467		kΩ
Upper Threshold	V_{UPPER}				2.0	V
Lower Threshold	V_{LOWER}		0.8			V
Hysteresis		V_{UPPER} – V_{LOWER}	200			mV
Enable Delay Time		Time from DISB# transitioning HI to when VSW responds to PWM.			40	us
Disable Delay Time		Time from DISB# transitioning LOW to when both output FETs are off.		21	50	ns
SMOD# INPUT						
SMOD# Input Voltage High	V_{SMOD_HI}		2.65			V
SMOD# Input Voltage Mid-state	$V_{SMOD\#\_MID}$		1.4		2.0	V
SMOD# Input Voltage Low	V_{SMOD_LO}				0.7	V
SMOD# Input Resistance	$R_{SMOD\#\_UP}$	Pull-up resistance to VCC		455		kΩ
SMOD# Propagation Delay, Falling	$T_{SMOD\#\_PD\_F}$	PWM = High-to-Low, SMOD# = Low to GL = 90%		34	40	ns
SMOD# Propagation Delay, Rising	$T_{SMOD\#\_PD\_R}$	PWM = High-to-Low, SMOD# = High to GL = 10%		22	30	ns

PWM INPUT						
Input High Voltage	V_{PWM_HI}		2.65			V
Input Mid-state Voltage	V_{PWM_MID}		1.4		2.1	V
Input Low Voltage	V_{PWM_LO}				0.7	V
Input Resistance	R_{PWM_HIZ}	SMOD# = $V_{SMOD\#\_HI}$ or $V_{SMOD\#\_LO}$	10			MΩ
Input Resistance	R_{PWM_BIAS}	SMOD# = $V_{SMOD\#\_MID}$		68		kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product per- formance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. ELECTRICAL CHARACTERISTICS (continued)

(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
PWM INPUT						
PWM Input Bias Voltage	V_{PWM_BIAS}	SMOD# = $V_{SMOD\#\_MID}$		1.7		V
Non-overlap Delay, Leading Edge	T_{NOL_L}	GL Falling = 1 V to GH−VSW Rising = 1 V		13		ns
Non-overlap Delay, Trailing Edge	T_{NOL_T}	GH−VSW Falling = 1 V to GL Rising = 1 V		12		ns
PWM Propagation Delay, Rising	T_{PWM,PD_R}	PWM = High to GL = 90%		13	35	ns
PWM Propagation Delay, Falling	T_{PWM,PD_F}	PWM = Low to VSW = 90%		52	78	ns
Exiting PWM Mid-state Propagation Delay, Mid-to-Low	$T_{PWM\_EXIT\_L}$	PWM = Mid-to-Low to GL = 10%		14	25	ns
Exiting PWM Mid-state Propagation Delay, Mid-to-High	$T_{PWM\_EXIT\_H}$	PWM = Mid-to-High to VSW = 10%		13	25	ns
ZCD FUNCTION						
Zero Cross Detect Threshold	V_{ZCD}			-6		mV
ZCD Blanking + Debounce Time	t_{BLNK}			330		ns

THERMAL WARNING & SHUTDOWN						
Thermal Warning Temperature	T_{THWN}	Temperature at Driver Die		150		℃
Thermal Warning Hysteresis	T_{THWN_HYS}			15		℃
Thermal Shutdown Temperature	T_{THDN}	Temperature at Driver Die		180		℃
Thermal Shutdown Hysteresis	T_{THDN_HYS}			25		℃
THWN Open Drain Current	I_{THWN}				5	mA
BOOSTSTRAP DIODE						
Forward Voltage		Forward Bias Current = 2.0 mA		380		mV
HIGH-SIDE DRIVER						
Output Impedance, Sourcing	R_{SOURCE_GH}	Source Current = 100 mA		0.9		Ω
Output Sourcing Peak Current	I_{SOURCE_GH}			2		A
Output Impedance, Sinking	R_{SINK_GH}	Source Current = 100 mA		0.7		Ω
Output Sinking Peak Current	I_{SINK_GH}			2.5		A
LOW-SIDE DRIVER						
Output Impedance, Sourcing	R_{SOURCE_GL}	Source Current = 100 mA		0.9		Ω
Output Sourcing Peak Current	I_{SOURCE_GL}	GL = 2.5 V		2		A
Output Impedance, Sinking	R_{SINK_GH}	Sink Current = 100 mA		0.4		Ω
Output Sinking Peak Current	I_{SINK_GL}	GL = 2.5 V		4.5		A
GL Rise Time		GL = 10% to 90%, C_{LOAD} = 3.0 nF		12		ns
GL Fall Time		GL = 90% to 10%, C_{LOAD} = 3.0 nF		6		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product per- formance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. LOGIC TABLE

INPUT TRUTH TABLE				
DISB#	PWM	SMOD# (Note 4)	GH (Not a Pin)	GL
L	X	X	L	L
H	H	X	H	L
H	L	X	L	H
H	MID	H or MID	L	ZCD (Note 5)
H	MID	L	L	L (Note 6)

4. PWM input is driven to mid-state with internal divider resistors when SMOD# is driven to mid-state and PWM input is undriven externally.
5. GL goes low following 80 ns de-bounce time, 250 ns blanking time and then SW exceeding ZCD threshold.
6. There is no delay before GL goes low.

Typical Performance Characteristics

(Test Conditions: VIN = 12 V, VCC = PVCC =5 V, VOUT =1 V & 1.8V, TA = 25°C, unless otherwise noted.)

Figure 3. Efficiency

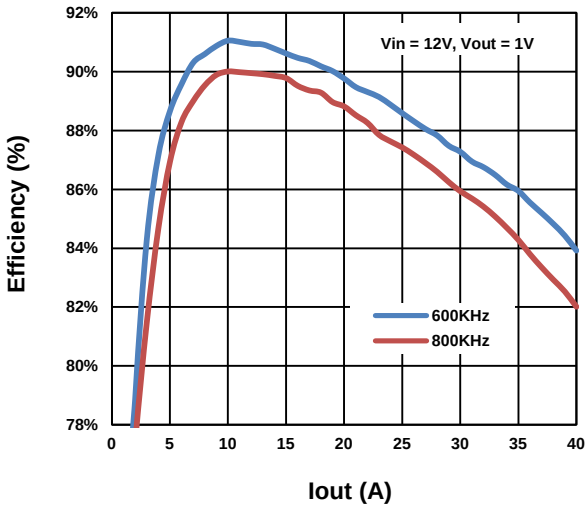


Figure 4. Power Loss vs. Output Current

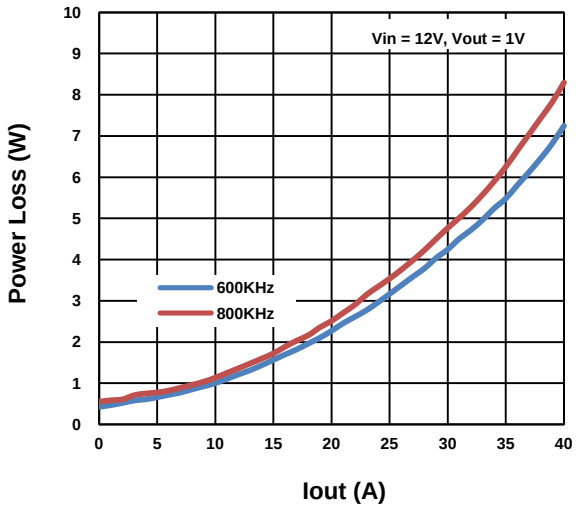


Figure 5. Efficiency

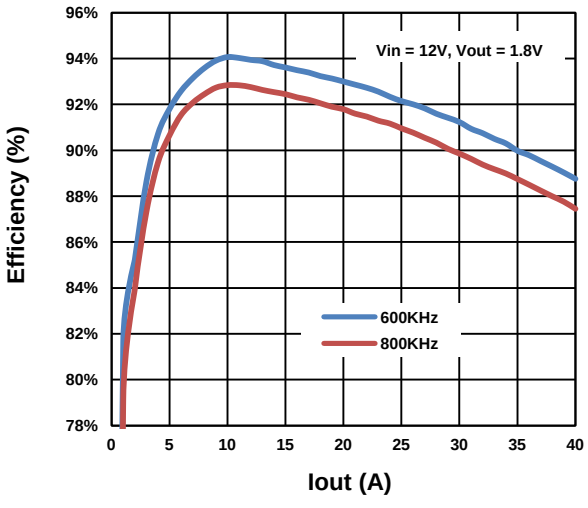
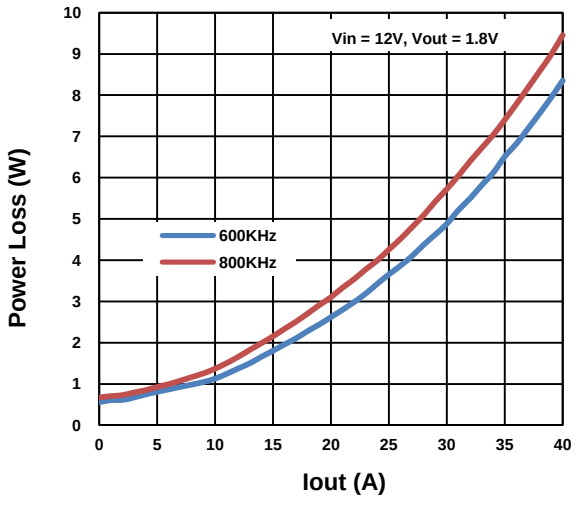


Figure 6. Power Loss vs. Output Current



Typical Performance Characteristics

(Test Conditions: VIN = 19 V, VCC = PVCC =5 V, VOUT =1 V & 1.8V, TA = 25°C, unless otherwise noted.)

Figure 7. Efficiency

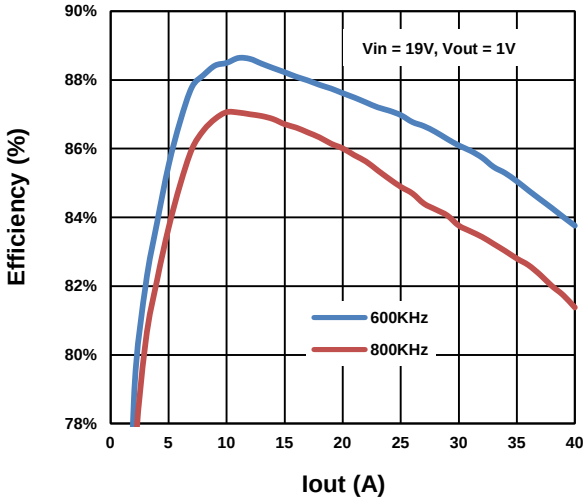


Figure 8. Power Loss vs. Output Current

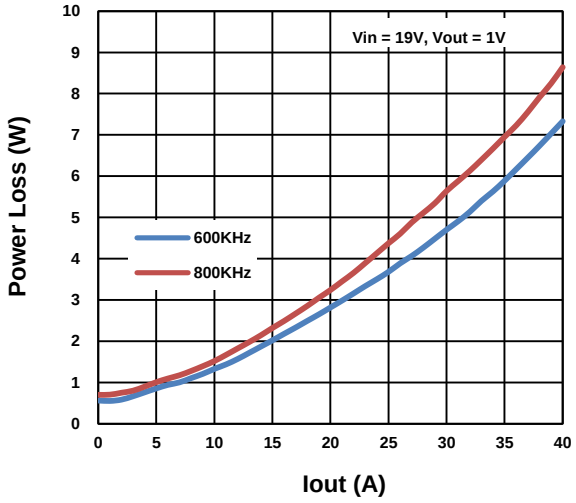


Figure 9. Efficiency

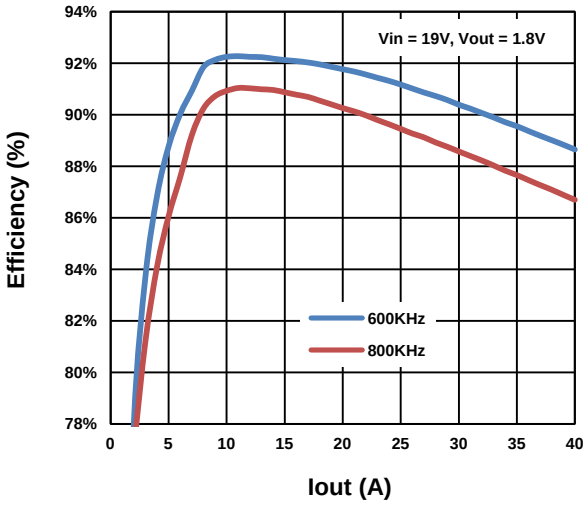
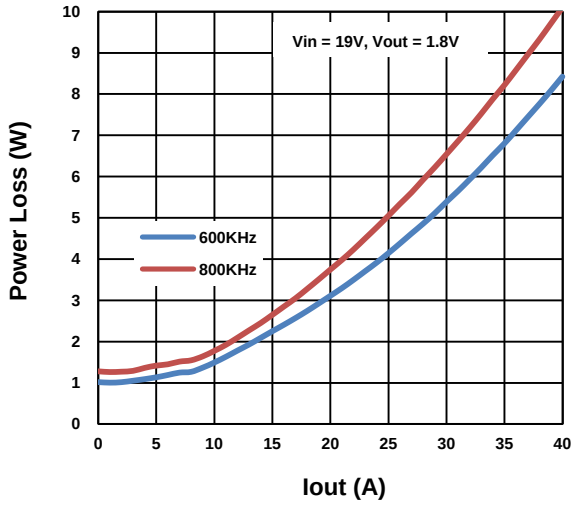


Figure 10. Power Loss vs. Output Current



Application Information

Theory of Operation

The NDA345FA is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The NDA345FA supports numerous application control definitions including ZCD (Zero Current Detect) and alternately PWM Tristate control. A PWM input signal is required to control the drive signals to the high-side and low-side integrated MOSFETs.

Low-Side Driver

The low-side driver drives an internal, ground-referenced low-$R_{DS(on)}$ N-Channel MOSFET. The voltage supply for the low-side driver is internally connected to the VCCD and PGND pins.

High-Side Driver

The high-side driver drives an internal,floating low-$R_{DS(on)}$ N-channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSW and PHASE) pins.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor and resistor. When the NDA345FA is starting up, the VSW pin is at ground, allowing the bootstrap capacitor to charge up to VCCD through the bootstrap diode (see Figure 1). When the PWM input is driven high, the high-side driver turns on the high-side MOSFET using the stored charge of the bootstrap capacitor. As the high-side MOSFET turns on, the voltage at the VSW and PHASE pins rises. When the high-side MOSFET is fully turned on, the switch node settles to VIN and the BST pin settles to VIN + VCCD (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the HS Driver. A multi-layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used as the

bootstrap capacitor. An optional 1 to 4Ω resistor in series with the bootstrap capacitor decreases the VSW overshoot.

Power Supply Decoupling

The NDA345FA sources relatively large currents into the MOSFET gates. In order to maintain a constant and stable supply voltage (VCCD) a low-ESR capacitor should be placed near the power and ground pins. A multi-layer ceramic capacitor (MLCC) between 1 µF and 4.7 µF is typically used.

A separate supply pin (VCC) is used to power the analog and digital circuits within the driver. A 1 µF ceramic capacitor should be placed on this pin in close proximity to the NDA345FA. It is good practice to separate the VCC and VCCD decoupling capacitors with a resistor (10Ω typical) to avoid coupling driver noise to the analog and digital circuits that control the driver function (see Figure 1).

Safety Timer and Overlap Protection Circuit

It is important to avoid cross-conduction of the two MOSFETS which could result in a decrease in the power conversion efficiency or damage to the device.

The NDA345FA prevents cross-conduction by monitoring the status of the MOSFETs and applying the appropriate amount of non-overlap (NOL) time (the time between the turn-off of one MOSFET and the turn-on of the other MOSFET). When the PWM input pin is driven high, the gate of the low-side MOSFET (LSGATE) goes low after a propagation delay (tpdlGL). The time it takes for the low-side MOSFET to turn off is dependent on the total charge on the low-side MOSFET gate.

The NDA345FA monitors the gate voltage of both MOSFETs and the switch node voltage to determine the conduction status of the MOSFETs. Once the low-side MOSFET is turned off an internal timer delays (tpdhGH) the turn-on of the high-side MOSFET. When the PWM input pin goes low, the gate of the high-side MOSFET (HSGATE) goes low after the propagation delay (tpdlGH). The time to turn off the high-side MOSFET (tfGH) is dependent on the total gate charge of the high-side MOSFET. A timer is triggered once the high-side MOSFET stops conducting, to delay (tpdhGL) the turn-on of the low-side MOSFET.

Zero Current Detect

The Zero Current Detect PWM (ZCD_PWM) mode is enabled when SMOD# is high (see Tables 6 and 8).

With PWM set to > VPWM_HI, GL goes low and GH goes high after the non-overlap delay. When PWM is driven to < VPWM_HI and to > VPWM_LO, GL goes high after the non-overlap delay, and stays high for the duration of the ZCD blanking timer (T_{ZCD_BLANK}) and an 80 ns de-bounce timer. Once this timer expires, VSW is monitored for zero current detection, and GL is pulled low once zero current is detected. The threshold on VSW to determine zero current undergoes an auto-calibration cycle every time DISB# is brought from low to high. This

auto-calibration cycle typicallytakes 25 µs to complete.

PWM Input

The PWM Input pin is a tri-state input used to control the HS MOSFET ON/OFF state. It also determines the state of the LS MOSFET. See Table 6 for logic operation. The PWM in some cases must operate with frequency programming resistances to ground. These resistances can range from 10 kΩ to 300K Ω depending on the application. When SMOD# is set to > VSMOD#_HI or to < VSMOD#_LO, the input impedance to the PWM input is very high in order to avoid interferences with controllers that must use programming resistances on the PWM pin.

If SMOD# is set to < VSMOD#_HI and > VSMOD#_LO(Mid-State), the PWM pin undriven default voltage is set to Mid-State with internal divider resistances.

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High-Side FET to prevent power transfer. The pin has a pull-down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull-up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NDA345FA.

Table 7. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State
L	X	Disabled (GH = GL = 0)
H	L	Disabled (GH = GL = 0)
H	H	Enabled (See Table 6)
H	Open	Disabled (GH = GL = 0)

Thermal Warning/Thermal Shutdown Output

The THWN pin is an open drain output. When the temperature of the driver exceeds TTHWN, the THWN pin is pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops T_{THWN_HYS} below T_{THWN}, the THWN pin goes high. If the driver temperature exceeds T_{THDN}, the part enters thermal shutdown and turns off both MOSFETs. Once the temperature falls T_{THDN_HYS} below T_{THDN}, the part resumes normal operation.

Skip Mode Input (SMOD#)

The SMOD# tri-state input pin has an internal pull-up resistance to VCC. When driven low, the SMOD# pin enables the low side synchronous MOSFET to operate independently of the internal ZCD function. When the SMOD# pin is set low while PWM is in the mid-state, the low side MOSFET is disabled to allow discontinuous mode operation.

The NDA345FA has the capability of internally connecting a resistor divider to the PWM pin. To engage this mode, SMOD# needs to be placed into mid-state. While in SMOD# mid-state, the IC logic is equivalent to SMOD# being in the high state.

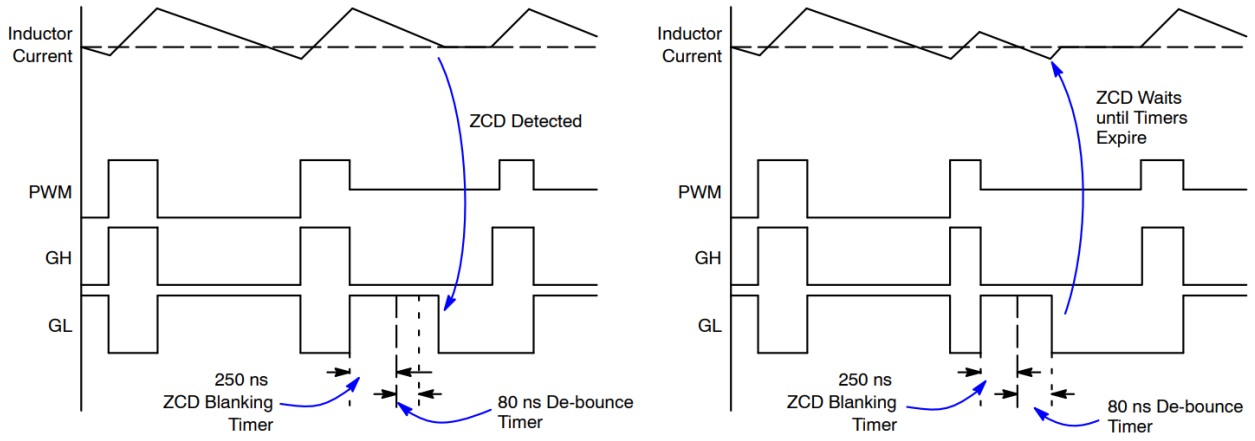


Figure 11. PWM Timing Diagram

NOTES: If the Zero Current Detect circuit detects zero current after the ZCD Wait timer period, the GL is driven low by the Zero Current Detect signal.
If the Zero Current Detect circuit detects zero current before the ZCD Wait timer period expires, the Zero Current detect signal is ignored and the GL is driven low at the end of the ZCD Wait timer period.

For Use with Controllers with 3-State PWM and No Zero Current Detection Capability:

Table 8. LOGIC TABLE − 3-STATE PWM CONTROLLERS WITH NO ZCD

PWM	SMOD#	GH (Not a Pin)	GL
H	H	ON	OFF
M	H	OFF	ZCD
L	H	OFF	ON

This section describes operation with controllers that are capable of 3 states in their PWM output and relies on the NDA345FA to conduct zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to either be set to 5 V or left disconnected. The NDA345FA has an internal pull-up resistor that connects to VCC that sets SMOD# to the logic high state if this pin is disconnected.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. To enter into DCM, PWM needs to be switched to the mid-state.

Whenever PWM transitions to mid-state, GH turns off and GL turns on. GL stays on for the duration of the de-bounce timer and ZCD blanking timers. Once these timers expire, the NDA345FA monitors the VSW voltage and turns GL off when VSW exceeds the ZCD threshold voltage. By turning off the LS FET, the body diode of the LS FET allows any positive current to go to zero but prevents negative current from conducting.

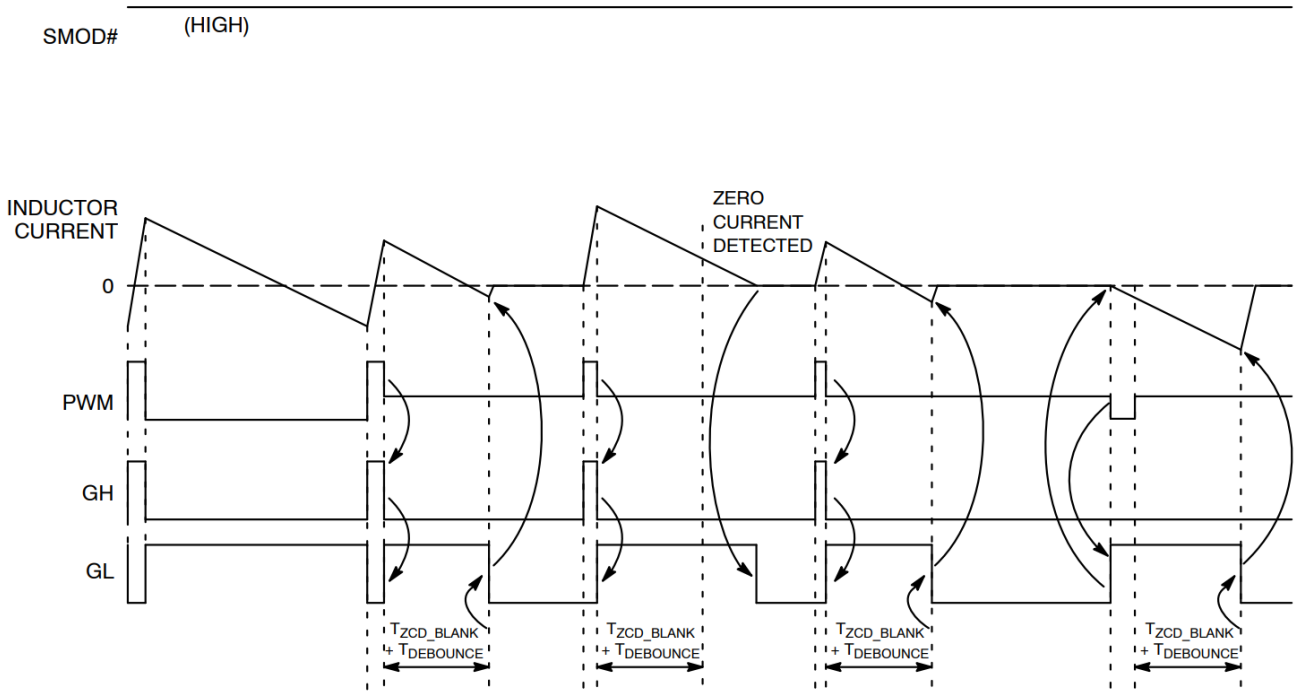


Figure 12. Timing Diagram − 3-State PWM Controller, No ZCD

For Use with Controllers with 3-state PWM and Zero Current Detection Capability:

Table 9. LOGIC TABLE − 3-STATE PWM CONTROLLERS WITH ZCD

PWM	SMOD#	GH (Not a Pin)	GL
H	L	ON	OFF
M	L	OFF	OFF
L	L	OFF	ON

This section describes operation with controllers that are capable of 3 PWM output levels and have zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to be pulled low (below VSMOD#_LO).

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. During DCM, the controller is responsible for detecting when zero current has occurred, and then notifying the NDA345FA to turn off the LS FET. When the controller detects zero current, it needs to set PWM to mid-state, which causes the NDA345FA to pull both GH and GL to their off states without delay.

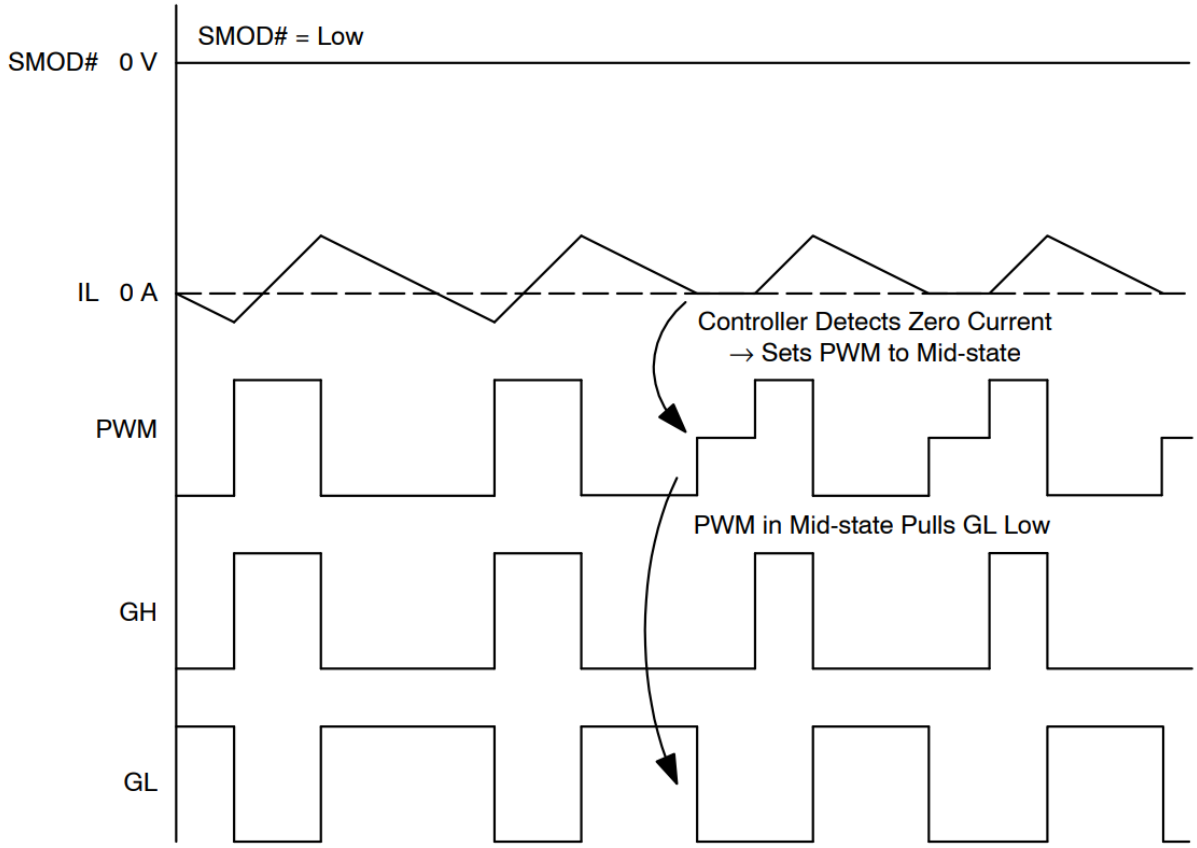
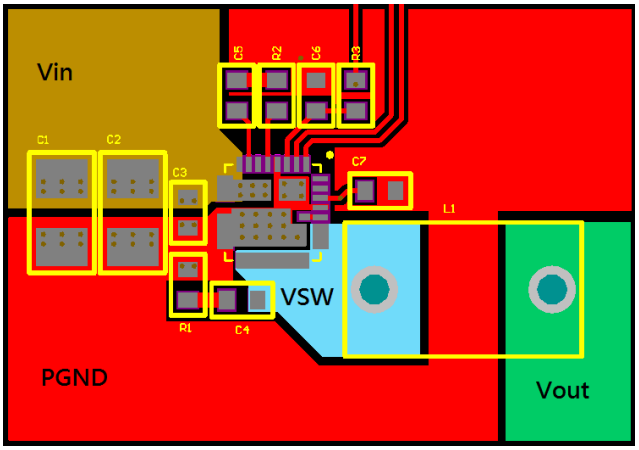


Figure 13. Timing Diagram − 3-State PWM Controller, with ZCD

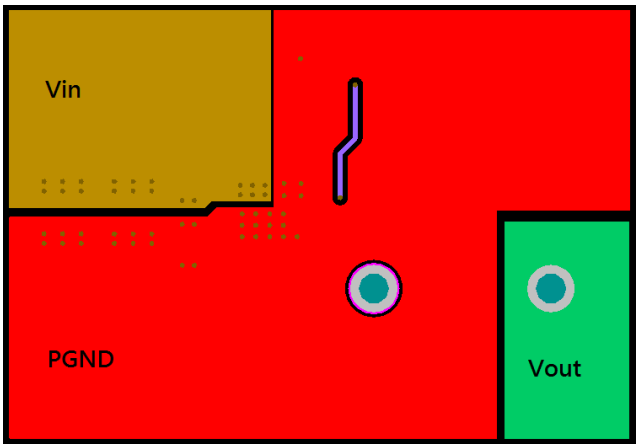
NDA345FA PCB layout guide

NDA345FA is a high-current-rated device capable of operating up to 2 MHz. Achieving such high frequency requires extremely fast switching speeds to keep switching losses and device temperatures within limits. Integrating a robust gate driver with MOSFETs in one package eliminates the parasitic components or PCB associated with the driver-to-MOSFET and between high side and low side MOSFETs, thus resulting in excellent switching speeds. However, correspondingly high levels of dv/dt and di/dt will be present throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients.

The PCB design is somewhat simplified because of the package integration and optimized pin assignment. The VIN and PGND pins are located adjacent to each other, and the input bypass capacitors (C1, C2, C3) should be placed as close as possible to these pins. The PHASE switching loop, formed by PHASE (VSW), output inductor (L1), and output capacitor COUT is the next critical current loop. This requires a second layer with an uninterrupted PGND plane with sufficient GND vias placed as close as possible to the bypass capacitor PGND pads.

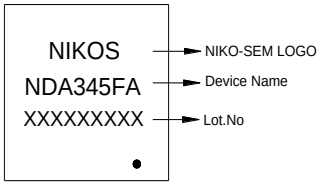


To simplify thermal management, both VIN and GND pads should be attached to larger VIN and PGND planes directly using a number of vias. These vias provide a thermal connection to the copper layers under the NDA345FA, which then conduct heat away from the heat source, whereby the “electrical vias” also function as “thermal vias”, It is essential to ensure that the cooper plane is not interrupted by tracks that run perpendicular to the thermal path away from the power component. The VCCD bypass capacitor CVCCD (C7) should connect directly to the PGND plane, and a via should be used to connect CVCCD directly to the PGND plane. Finally, CBOOT (C5) and RBOOT(R2) should be connected directly to pins 5, and 7.



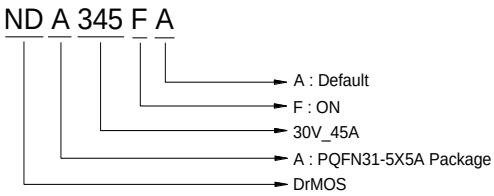
Marking Information:(Please see the corresponding data sheet)

1.零件Marking 文字面說明

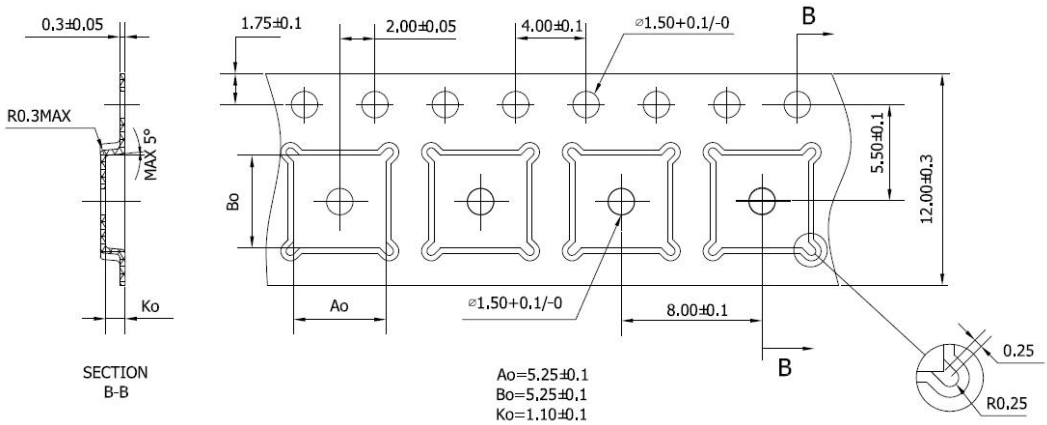


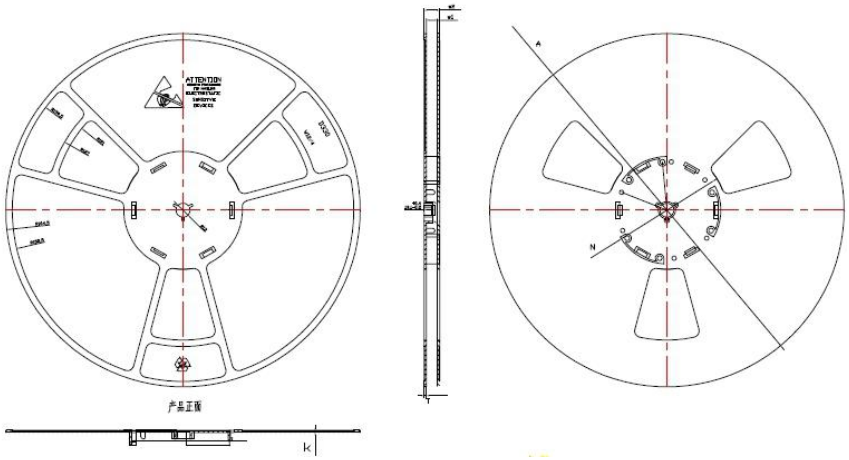
#1

2.零件 Part number 說明



Tape&Reel Information:5000pcs/Reel

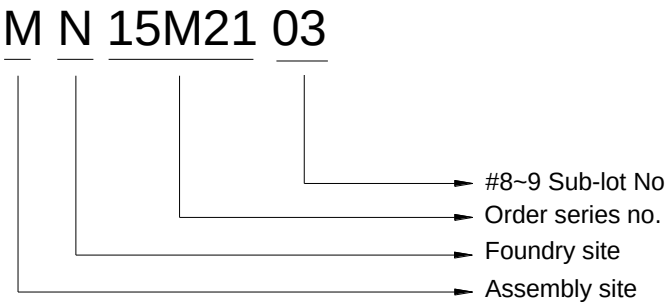




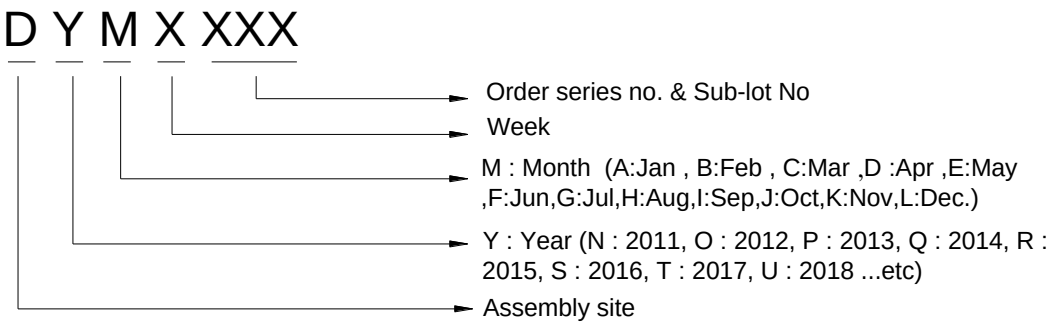
附註:All Dimension in millimeter

Lot.No. & Date Code rule

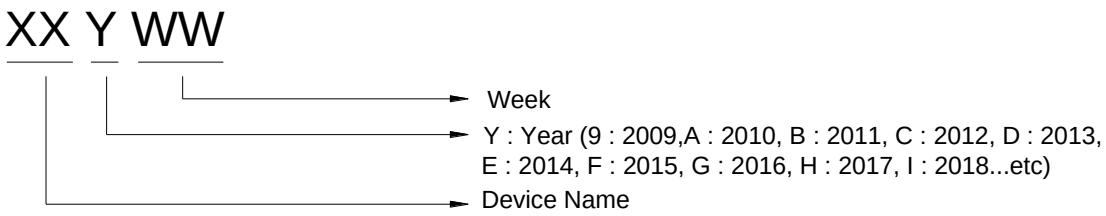
1.LOT.NO.



2.Date Code



3.Date Code (for Small package)



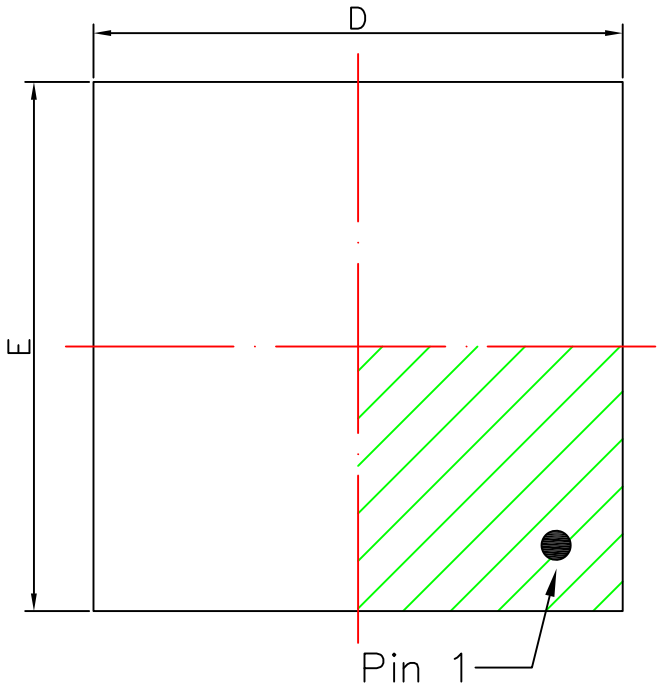
Label rule

標籤內容 (Label content)

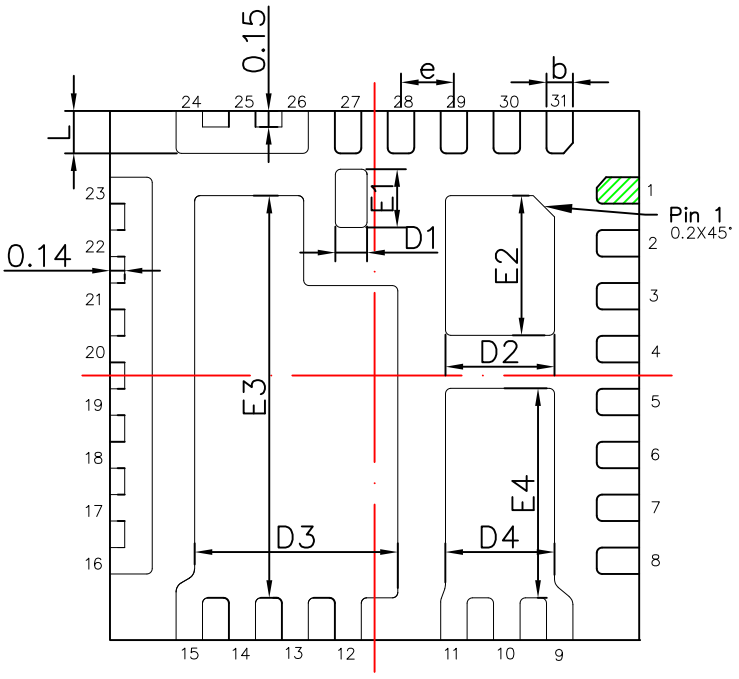
1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可區分英文"O"和數字"0"，"G 和"Q"的字型即可) (Or any font capable of being distinguished for Letter O and digital 0, and for G and Q))
3	NIKO-SEM	Height: 4 mm
4	NIKO SEMICONDUCTOR CO., LTD.	Height: 1 mm
5	Package	Height: 2 mm
6	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
7	Device	Height: 3 mm (Max: 16 Digit) Device Name not including Rev.
8	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
9	D/C	Height: 3 mm (Max: 7 Digit)
10	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
11	Pb Free label	Pb Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Halogen Free label	G Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
13	Scan info	Device / Lot / D/C / QTY , Insert " / " between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least

NIKO-SEM

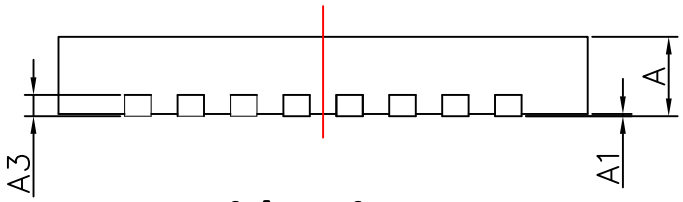
PQFN31-5X5



Top View



Bottom View

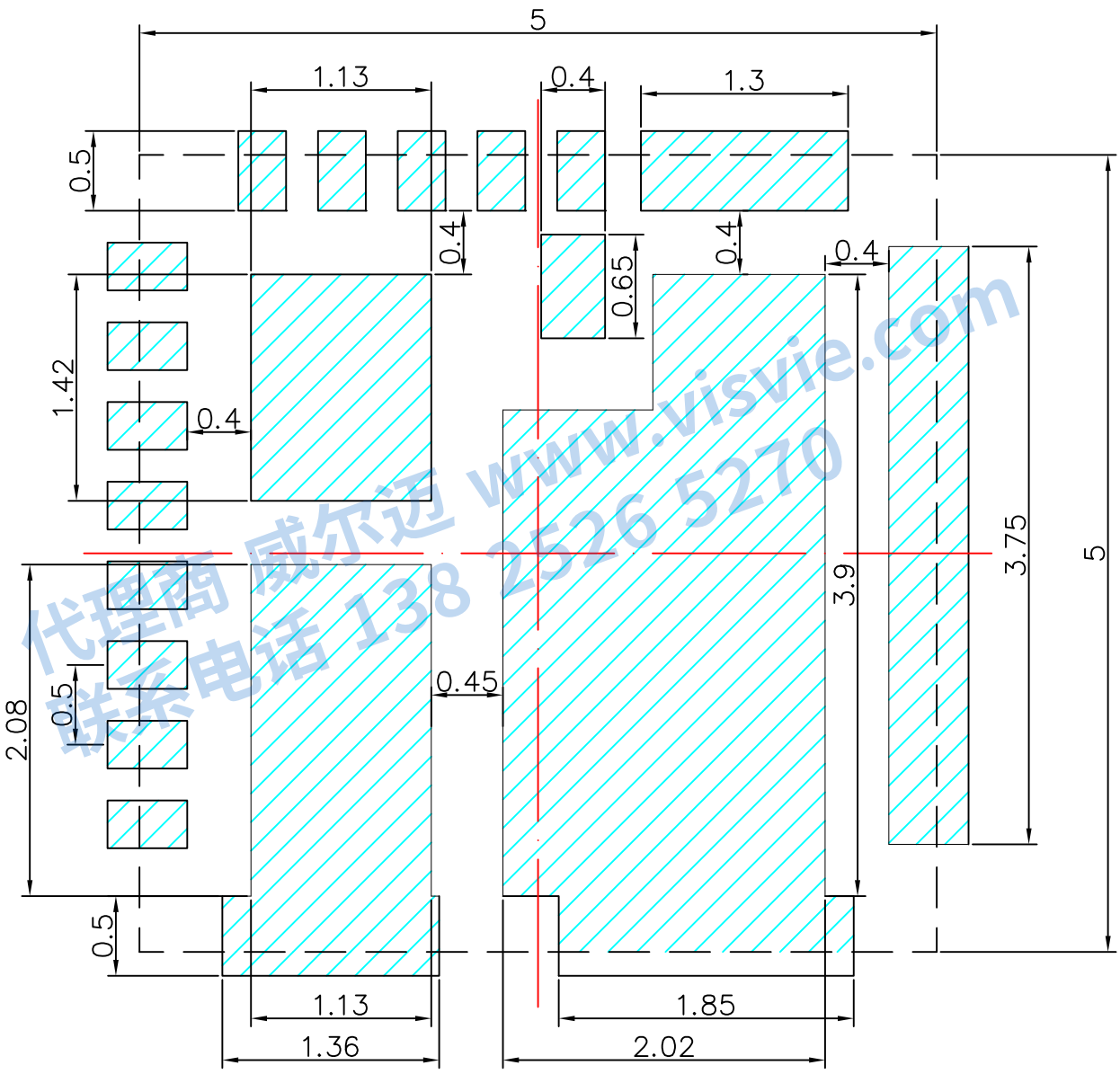


Side View

SYMBOL	DIMENSIONS IN MM			SYMBOL	DIMENSIONS IN MM		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	0.70	0.75	0.80	D4	0.93	1.03	1.13
A1	0	0.02	0.05	E	5.00 BSC		
A3	0.20 REF.			E1	0.45	0.55	0.65
b	0.20	0.25	0.30	E2	1.22	1.32	1.42
D	5.00 BSC			E3	3.70	3.80	3.90
D1	0.20	0.30	0.40	E4	1.88	1.98	2.08
D2	0.93	1.03	1.13	e	0.50 BSC		
D3	1.82	1.92	2.02	L	0.30	0.40	0.50

*** Dimensions Are Exclusive Of Burrs , Mold Flash And Tie Bar Protrusions**

Package Dimension	PQFN31-5x5			REV.	1.1	Q'TY	1 OF 2
UNIT	MM	SCALE	15 : 1	DATE	Aug.10.2023		



Land Pattern
(Only for reference)