SGM52421R8/SGM52421R8A
8-Channel, Low Noise, Low Power, 24-Bit, Sigma-Delta ADC with PGA and Reference

FEATURES

- Power Supply Range: 2.7V to 3.6V and ±1.8V
- 3 Power Modes Available
- Up to 23 Noise Free Bits in Full Power Mode with Gain = 1
- Rail-to-Rail Analog Inputs Applicable for Gains > 1
- Simultaneous 50Hz/60Hz Rejection at 25SPS (Single Cycle Settling)
- Crosspoint Multiplexed Analog Inputs
  - Provide 8 Differential/15 Pseudo Differential Inputs
- Programmable Gain Allows Settings from 1 to 128
- Matched Programmable Excitation Currents Integrated
- Internal Clock Oscillator Included
- On-Chip Bias Voltage Generator Available
- Low-side Power Switch Incorporated
- General-Purpose Outputs Provided
- Multiple Filter Options Offered
- Internal Temperature Sensor for Enhanced Functionality
- Self and System Calibration Capabilities
- Sensor Burnout Detection Enabled
- Automatic Channel Sequencer Simplifying Operations
- Per Channel Configuration Customizable
- Support Independent Interface Power Supply
- 3-Wire or 4-Wire Serial Interface
  - Compatible with SPI, QSPI, Microwire, and DSP
  - Equipped with Schmitt Trigger on SCLK
- Operating Temperature Range: -40℃ to +125℃
- Available in a Green TQFN-5×5-32IL Package

APPLICATIONS

Industrial Process Control
Instrumentation
Temperature Measurement
Smart Transmitters
Pressure Measurement

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GENERAL DESCRIPTION

The SGM52421R8/SGM52421R8A deliver precise low-power, low-noise analog front-end integration for high-precision measurements. It includes a 24-bit Σ-Δ ADC, supporting 8 differential or 15 single-ended/pseudo-differential inputs, with an on-board low-gain stage for direct small-signal ADC interfacing.

A key feature is its tri-mode power flexibility, optimizing current consumption, output data rate (ODR) and RMS noise. It also offers diverse filter options for enhanced versatility.

At 25SPS (single-cycle settling), it achieves simultaneous 50Hz/60Hz rejection (> 80dB at lower ODRs).

Core strengths include high signal chain integration: precision band gap reference (plus external differential reference support), programmable excitation/burnout currents, and a bias voltage generator. A low-side power switch cuts bridge sensor power between conversions to minimize total power use.

With an integrated channel sequencer, it enables multi-channel communication (up to 16 channels, including supply/reference diagnostics), allowing interleaved diagnostics and conversions. Per-channel configuration lets users customize gain, filter, ODR, buffering and reference individually.

Comprehensive diagnostics (CRC, signal chain validation, serial interface checks) boost system robustness, reducing external components to save board space, shorten design cycles and cut costs. FMEDA assessments show > 90% safe failure fraction (SFF) per IEC 61508, ensuring reliability.

It operates on a single 2.7V to 3.6V analog supply (or dual 1.8V supplies), with 2V to 3.6V digital power. Offered in a Green TQFN-5×5-32IL package, it works from -40℃ to +125℃.

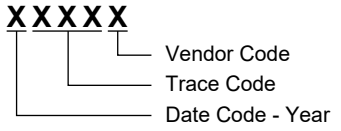
Note: in this datasheet, multi-function pins (e.g., DOUT/nRDY) are labeled with full names or a single relevant function (e.g., nRDY).

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM52421R8	TQFN-5×5-32IL	-40℃ to +125℃	SGM52421R8XTVN32G/TR	SGM1XX XTVN32 XXXXX	Tape and Reel, 3000
SGM52421R8A	TQFN-5×5-32IL	-40℃ to +125℃	SGM52421R8AXTVN32G/TR	SGM2FE XTVN32 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AV_{SS} ..... -0.3V to 3.96V
IOV_{DD} to DGND ..... -0.3V to 3.96V
IOV_{DD} to AV_{SS} ..... -0.3V to 5.94V
AV_{SS} to DGND ..... -1.98V to 0.3V
Analog Input Voltage to AV_{SS} ..... -0.3V to AV_{DD} + 0.3V
Reference Input Voltage to AV_{SS} ..... -0.3V to AV_{DD} + 0.3V
Digital Input Voltage to DGND ..... -0.3V to IOV_{DD} + 0.3V
Digital Output Voltage to AGND ..... -0.3V to IOV_{DD} + 0.3V
AINx/Digital Input Current 10mA
Package Thermal Resistance
TQFN-5×5-32IL, θ_{JA} ..... 27.5℃/W
TQFN-5×5-32IL, θ_{JB} ..... 7.7℃/W
TQFN-5×5-32IL, $\theta_{JC\ (TOP)}$ ..... 22.3℃/W
TQFN-5×5-32IL, $\theta_{JC\ (BOT)}$ ..... 1.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

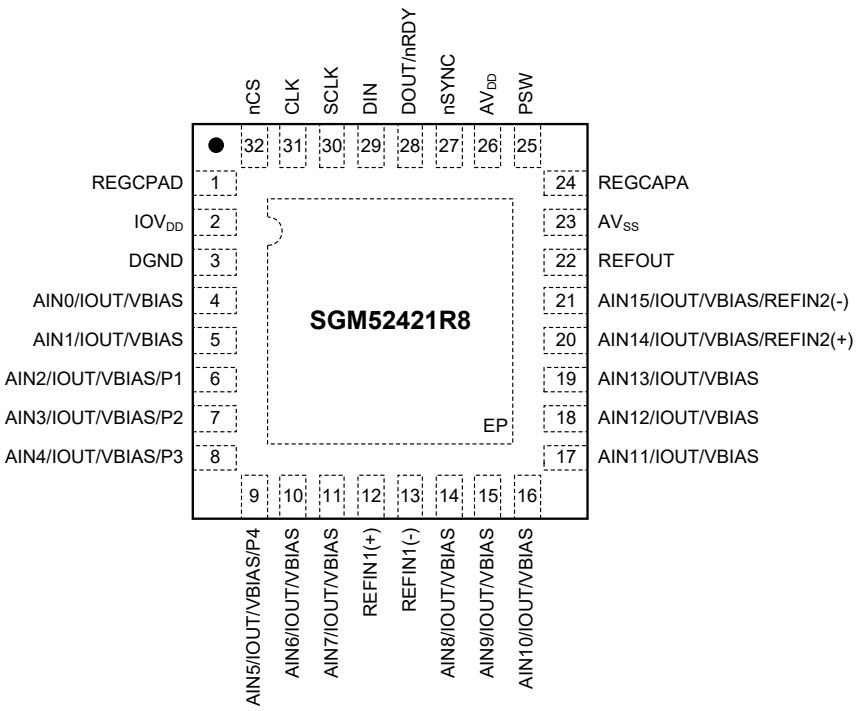
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

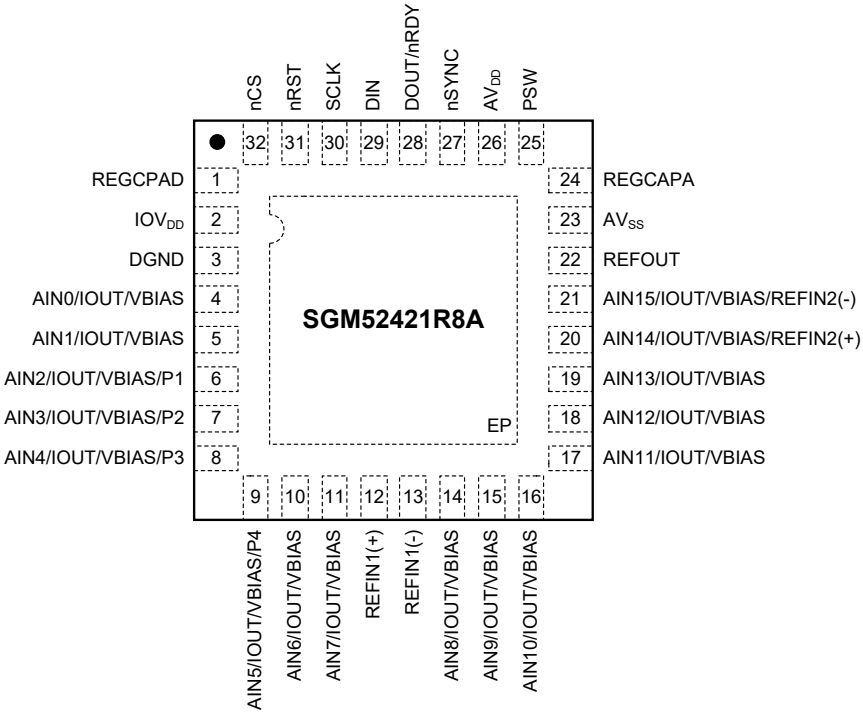
PIN CONFIGURATIONS

SGM52421R8 (TOP VIEW)



TQFN-5×5-32IL

SGM52421R8A (TOP VIEW)



TQFN-5×5-32IL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	REGCAPD	Digital LDO Regulator Output: It is recommended to connect this pin to DGND with a 0.1μF capacitor for decoupling.
2	IOV_{DD}	Digital Supply Voltage (IOV_{DD}): 2V to 3.6V. IOV_{DD} operates independently of AV_{DD}, so the serial interface can run at 2V while AV_{DD} stays at 3.6V.
3	DGND	Digital Ground.
4	AIN0/IOUT/VBIAS	Analog Input 0/Internal Excitation Current Source Output/Bias Voltage Pin. The pin is multifunctional. Programmable via registers as positive/negative terminal for differential/ pseudo-differential input, access to internal programmable excitation current source, or routed IOUT1/IOUT0. It also generates a bias voltage midway between analog supply rails.
5	AIN1/IOUT/VBIAS	Analog Input 1/Internal Excitation Current Source Output/Bias Voltage Pin. The pin is multifunctional. Programmable via registers as positive/negative terminal for differential/ pseudo-differential input, access to internal programmable excitation current source, or routed IOUT1/IOUT0. It also generates a bias voltage midway between analog supply rails.
6	AIN2/IOUT/VBIAS/P1	Multifunctional Pin (Analog Input 2/Internal Excitation I/O/Bias Voltage/GPO 1). Configurable via registers, it acts as ± terminal for differential/pseudo-differential input, accesses the programmable internal excitation current source, and routes IOUT0/IOUT1. It also generates mid-rail bias voltage and works as a GPO (referenced to AV_{SS}/AV_{DD}).
7	AIN3/IOUT/VBIAS/P2	Versatile Pin (Analog Input 3/Internal Excitation I/O/Bias Voltage/GPO 2). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, generates mid-rail bias voltage, and acts as a GPO (referenced to AV_{SS}/AV_{DD}).
8	AIN4/IOUT/VBIAS/P3	Versatile Pin (Analog Input 4/Internal Excitation I/O/Bias Voltage/GPO 3). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, generates mid-rail bias voltage, and serves as a GPO (referenced to AV_{SS}/AV_{DD}).
9	AIN5/IOUT/VBIAS/P4	Versatile Pin (Analog Input 5/Internal Excitation I/O/Bias Voltage/GPO 4). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, generates mid-rail bias voltage, and acts as a GPO (referenced to AV_{SS}/AV_{DD}).
10	AIN6/IOUT/VBIAS	Multifunctional Pin (Analog Input 6/Internal Excitation I/O/Bias Voltage). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, and generates mid-rail bias voltage.
11	AIN7/IOUT/VBIAS	Multifunctional Pin (Analog Input 7/Internal Excitation I/O/Bias Voltage). Register-configurable as ± terminal for differential/pseudo-differential input. It accesses the programmable internal excitation current source, routes IOUT0/IOUT1, and generates mid-rail bias voltage.
12	REFIN1(+)	Positive Reference Input. Connect an external reference between REFIN1(+) and REFIN1(-). REFIN1(+) ranges from AV_{DD} to AV_{SS} + 0.5V. Nominal reference voltage (REFIN1(+) - REFIN1(-)) is 2.5V, but the device supports 0.5V to AV_{DD}.
13	REFIN1(-)	Negative Reference Input Accommodates a Reference Input Ranging from AV_{SS} to AV_{DD} - 0.5V.
14	AIN8/IOUT/VBIAS	Analog Input 8/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
15	AIN9/IOUT/VBIAS	Analog Input 9/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.

PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
16	AIN10/IOUT/VBIAS	Analog Input 10/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
17	AIN11/IOUT/VBIAS	Analog Input 11/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
18	AIN12/IOUT/VBIAS	Analog Input 12/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
19	AIN13/IOUT/VBIAS	Analog Input 13/Internal Excitation Current Source Output/Bias Voltage: Versatile pin with multiple functions. Configurable via registers as ± terminal for differential/pseudo-differential input. Accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here) and generates bias voltage midway between analog power rails.
20	AIN14/IOUT/VBIAS/ REFIN2(+)	Analog Input 14/Internal Excitation Current Source Output/Bias Voltage/Positive Reference Input: Multifunctional pin. Register-configurable as ± terminal for differential/pseudo-differential input, accesses internal programmable excitation current source (IOUT0/IOUT1 routable here), and generates bias voltage midway between analog power rails. Also acts as REFIN2(+) input: ranges from AV_{DD} to AV_{SS} + 0.5V. Nominal REFIN2(±) voltage is 2.5V; device supports 0.5V to AV_{DD}.
21	AIN15/IOUT/VBIAS/ REFIN2(-)	Analog Input 15/Internal Excitation Current Source Output/Bias Voltage/Negative Reference Input: Versatile, multifunctional pin. Register-configurable as ± terminal for differential/pseudo-differential input, accesses internal programmable excitation current source (IOUT0/IOUT1 steerable here), and generates bias voltage midway between analog power rails. Also serves as REFIN2(-) (range: AV_{SS} to AV_{DD} - 0.5V) and internal 2.5V reference buffered output.
22	REFOUT	Internal Reference Output Provides the Buffered Output of the Internal 2.5V Voltage Reference on This Pin.
23	AV_{SS}	Analog Supply Voltage (AV_{DD}, referenced to AV_{SS}): Regulates AV_{DD} voltage. AV_{DD} - AV_{SS} differential: 2.7V to 3.6V (mid/low power mode). 2.7V to 3.6V (full power mode). AV_{SS} can be < 0V for dual supplies (e.g., AV_{SS} = -1.8V, AV_{DD} = 1.8V provides ±1.8V to ADC).
24	REGCAPA	Analog LDO Regulator Output Requires Decoupling to AV_{SS} Using a 0.1μF Capacitor.
25	PSW	Low-side Power Switch Connects to AV_{SS}.
26	AV_{DD}	Analog Supply Voltage.
27	nSYNC	Synchronization Input (nSYNC): Logic input for syncing digital filters and analog modulators in multi-SGM52421R8/SGM52421R8A setups. Low nSYNC resets digital filter nodes, filter/calibration control logic, holds analog modulator in reset, and sets nRDY high (if low). Doesn't affect digital interface.
28	DOUT/nRDY	Serial Data Output/Data Ready Output (DOUT/nRDY): Dual-function pin. Acts as serial data output for ADC's output shift register (accesses on-chip data/control registers). Serves as data ready indicator: goes low when conversion completes, returns high if unread before next update. Falling edge can trigger processor interrupt for valid data. With external serial clock, outputs data/control words on the falling SCLK (valid on the rising SCLK) when nCS is low.
29	DIN	Serial Data Input: Feeds ADC's input shift register, transferring data to internal control registers. Register selection bits in the communications register specify the target register.
30	SCLK	Serial Clock Input (SCLK): Interface for ADC data transfers. Schmitt-triggered input enables opto-isolated compatibility. Operates as continuous clock (continuous pulse train) or non-continuous clock (smaller data batches).

PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
31	CLK	Clock Input/Output Pin. Supports internal or external clock for ADC operation. Enables internal clock output when active; accepts external clock when internal is disabled. Allows multi-ADC synchronization to a common clock for simultaneous conversions. (SGM52421R8 Only)
	nRST	Reset Pin. (SGM52421R8A Only)
32	nCS	Chip Select Input (nCS): Active-low logic input for ADC selection. Used to select the ADC in multi-device serial bus systems or for frame synchronization. If SPI diagnostics are unused, hardwire low to enable 3-wire mode (interfaced via SCLK, DIN, DOUT).
Exposed Pad	EP	Exposed Pad. Connect to AV_{SS}.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 2V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC							
Output Data Rate	f_{ADC}	Low power mode		1.17		2400	SPS
		Mid power mode		2.34		4800	
		Full power mode		9.38		19200	
No Missing Codes (1)		FS (2) > 2, $Sinc^4$ filter		24			Bits
		FS (2) > 8, $Sinc^3$ filter		24			
Resolution				See the RMS Noise and Resolution section			
RMS Noise and Update Rates				See the RMS Noise and Resolution section			
Integral Nonlinearity	INL	Gain = 1 (1)			±4		ppm of FSR
		Gain > 1 (3)			±4		
Offset Error (4)	E_O	Before calibration	Gain = 1 to 8		1.5		μV
			Gain = 16 to 128		1.5		
		After internal calibration/system calibration			In order of noise		
Offset Error Drift vs. Temperature (5) (13)		Low power mode	Gain = 1 or Gain > 32		32		nV/℃
			Gain = 2 to 8		22		
			Gain = 16		36		
			Gain = 32		17		
		Mid power mode	Gain = 1 or Gain > 32		23		
			Gain = 2 to 8		16		
			Gain = 16		21		
			Gain = 32		10		
		Full power mode	Gain = 1 or Gain > 32		21		
			Gain = 2 to 8		12		
			Gain = 16		39		
			Gain = 32		18		
Gain Error (4) (6)	E_G	Before internal calibration	Gain = 1, T_A = +25℃		0.001		%
			Gain > 1		0.001		
		After internal calibration	Gain = 2 to 8, T_A = +25℃		0.004		
			Gain = 16 to 128		0.01		
		After system calibration			TBD		
Gain Error Drift vs. Temperature					1		ppm/℃

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 2V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Rejection (A_{INP} = A_{INN} = 0.9V, External Reference)		Low power mode	Gain = 2 to 16		110		dB
			Gain = 1 or Gain > 16		105		
		Mid power mode (1)	Gain = 2 to 16		110		
			Gain = 1 or Gain > 16		105		
		Full power mode	AVDD at DC		105		
			AVDD at 50Hz or 60Hz		TBD		
			DVDD at DC		120		
Common Mode Rejection (7)		At DC (1)	A_{IN} = AVDD/2, Gain = 1		120		dB
		At DC	A_{IN} = AVDD/2, Gain 2 or 4		120		
			A_{IN} = AVDD/2, Gain 2 or 4	TBD (8)			
			A_{IN} = AVDD/2, Gain ≥ 8		120		
			A_{IN} = AVDD/2, Gain ≥ 8	TBD (8)			
		$Sinc^3$, $Sinc^4$ filter (1)	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		142		
			50SPS, 50Hz ± 1Hz		134		
			60SPS, 60Hz ± 1Hz		135		
		Fast settling filters (1)	First notch at 50Hz, 50Hz ± 1Hz		124		
			First notch at 60Hz, 60Hz ± 1Hz		124		
		Post filters (1)	20SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		135		
			25SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		136		
Normal Mode Rejection (1)		$Sinc^4$ filter, external clock	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		TBD		dB
			50SPS, REJ60 (9) = 1, 50Hz ± 1Hz, 60Hz ± 1Hz		TBD		
			50SPS, 50Hz ± 1Hz		TBD		
			60SPS, 60Hz ± 1Hz		TBD		
		$Sinc^4$ filter, internal clock	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		109		
			50SPS, REJ60 (9) = 1, 50Hz ± 1Hz, 60Hz ± 1Hz		85		
			50SPS, 50Hz ± 1Hz		103		
			60SPS, 60Hz ± 1Hz		102		
		$Sinc^3$ filter, external clock	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		TBD		
			50SPS, REJ60 (9) = 1, 50Hz ± 1Hz, 60Hz ± 1Hz		TBD		
			50SPS, 50Hz ± 1Hz		TBD		
			60SPS, 60Hz ± 1Hz		TBD		
		$Sinc^3$ filter, internal clock	10SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		104		
			50SPS, REJ60 (9) = 1, 50Hz ± 1Hz, 60Hz ± 1Hz		68		
			50SPS, 50Hz ± 1Hz		97		
			60SPS, 60Hz ± 1Hz		97		

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 2V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Normal Mode Rejection (1)		Fast settling filters, external clock	First notch at 50Hz, 50Hz ± 0.5Hz		TBD		
			First notch at 60Hz, 60Hz ± 0.5Hz		TBD		
		Fast settling filters, internal clock	First notch at 50Hz, 50Hz ± 0.5Hz		33		
			First notch at 60Hz, 60Hz ± 0.5Hz		35		
		Post filters, external clock	20SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		TBD		
			25SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		TBD		
		Post filters, internal clock	20SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		86		
			25SPS, 50Hz ± 1Hz, 60Hz ± 1Hz		62		
Analog Inputs (10)							
Differential Input Voltage Ranges (11)		V_{REF} = REFINx(+) - REFINx(-), or internal reference			±V_{REF}/gain		V
Absolute A_{IN} Voltage Limits (1)		Gain = 1 (unbuffered)		AV_{SS} - 0.05		AV_{DD} + 0.05	V
		Gain = 1 (buffered)		AV_{SS} + 0.1		AV_{DD} - 0.1	
		Gain > 1		AV_{SS} - 0.05		AV_{DD} + 0.05	
Absolute Input Current		Buffered	Low power mode		±0.64		nA
			Mid power mode		±1.32		
			Full power mode		±4.28		
		Gain = 1 (unbuffered), current varies with input voltage			±4		μA/V
Analog Inputs (10)							
Differential Input Current		Buffered	Low power mode		±0.18		nA
			Mid power mode		±0.36		
			Full power mode		±1.35		
Analog Input Current Drift		Buffered	Low power mode		TBD		pA/℃
			Mid power mode		TBD		
			Full power mode		TBD		
		Gain = 1 (unbuffered), current varies with input voltage			TBD		nA/V/℃

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 2V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input								
Internal Reference	Initial Accuracy		T_A = +25℃			2.5		V
	Drift		T_A = +25℃ to +125℃			4		ppm/℃
	Output Current					TBD		mA
	Load Regulation					TBD		μV/mA
	Power Supply Rejection					85		dB
External Reference	External REFIN Voltage (1)		REFIN = REFINx(+) - REFINx(-)			2.5		V
	Absolute REFIN Voltage Limits (1)		Unbuffered			TBD		V
			Buffered			TBD		
	Absolute Input Current		Buffered	Low power mode		±0.16		nA
				Mid power mode		±0.29		
				Full power mode		±1.22		
			Unbuffered			±10		μA
	Reference Input Current Drift		Buffered	Low power mode		TBD		pA/℃
				Mid power mode		TBD		
				Full power mode		TBD		
			Unbuffered			TBD		nA/℃
	Normal Mode Rejection					Same as for analog inputs		dB
	Common Mode Rejection					107		
Excitation Current Sources (IOUT0/IOUT1) Available on Any Analog Input Pin								
Output Current						50/100/ 250/500/ 750/1000		μA
Initial Tolerance			T_A = +25℃, 50μA to 1.5mA			±0.9		%
Drift						22.5		ppm/℃
Current Matching			Matching between IOUT0 and IOUT1, V_{OUT} = 0V, 50μA to 1.5mA			±0.18		%
Drift Matching (1)			250μA to 1mA			1.8		ppm/℃
Line Regulation (AV_{DD})			AV_{DD} = 3V ± 5%			±0.03		%/V
Load Regulation						±0.02		%/V

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 2V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Excitation Current Sources (IOUT0/IOUT1) Available on Any Analog Input Pin						
Output Compliance (1)		50μA/100μA/250μA/500μA current sources, 2% accuracy	AV_{SS} - 0.05		AV_{DD} - 0.37	V
		750μA and 1000μA current sources, 2% accuracy	AV_{SS} - 0.05		AV_{DD} - 0.48	
Bias Voltage (V_{BIAS}) Generator Available on Any Analog Input Pin						
Bias Voltage	V_{BIAS}			AV_{SS} + (AV_{DD} - AV_{SS})/2		V
V_{BIAS} Generator Start-Up Time		Dependent on the capacitance connected to AINx		TBD		μs/nF
Temperature Sensor						
Accuracy				TBD		℃
Sensitivity				TBD		Codes/℃
Low-Side Power Switch						
On-Resistance	R_{ON}			4.5		Ω
Allowable Current (1)		Continuous current		TBD		mA
Burnout Currents						
A_{IN} Current		Analog inputs must be buffered		0.5/2/4		μA
Digital Outputs (P1 to P4)						
High-Level Output Voltage	V_{OH}	I_{SOURCE} = 100μA		AV_{DD} - 0.01		V
Low-Level Output Voltage	V_{OL}	I_{SINK} = 100μA		TBD		V
Diagnostics						
Power Supply Monitor Detect Level		Analog low dropout regulator (ALDO), AV_{DD} - AV_{SS} ≥ 2.7V			1.6	V
		Digital LDO (DLDO), IOV_{DD} ≥ 1.75V			1.55	
Reference Detect Level		REF_DET_ERR bit active if V_{REF} < 0.7V		0.7		V
AINM/AINP Over-Voltage Detect Level			AV_{DD} + 0.04			V
AINM/AINP Under-Voltage Detect Level					AV_{SS} - 0.04	V
Internal/External Clock						
Internal Clock Frequency				614.4		kHz
Internal Clock Duty Cycle				50:50		%
External Clock Frequency		Internal divide by 4		2.4576		MHz
External Clock Duty Cycle Range				45:55 to 55:45		%
Logic Inputs (1)						
Low-Level Input Voltage	V_{INL}	2V ≤ IOV_{DD} < 2.3V			0.3 × IOV_{DD}	V
		2.3V ≤ IOV_{DD} ≤ 3.6V			0.7	
High-Level Input Voltage	V_{INH}	2V ≤ IOV_{DD} < 2.3V	0.7 × IOV_{DD}			V
		2.3V ≤ IOV_{DD} < 2.7V	1.7			
		2.7V ≤ IOV_{DD} ≤ 3.6V	2			
Hysteresis		2V ≤ IOV_{DD} ≤ 3.6V	0.2		0.6	V
Input Currents		V_{IN} = IOV_{DD} or GND	-1		1	μA
Input Capacitance		All digital inputs		TBD		pF

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 2V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Outputs (Including CLK)							
High-Level Output Voltage (1)	V_{OH}	I_{SOURCE} = 100μA		IOV_{DD} - 0.35			V
Low-Level Output Voltage (1)	V_{OL}	I_{SINK} = 100μA				0.4	V
Floating State Output Capacitance					TBD		pF
Data Output Coding					Offset Binary		
System Calibration (1)							
Calibration Limit		Full-scale				1.05 × FS	V
		Zero-scale		-1.05 × FS			V
Input Span				0.8 × FS		2.1 × FS	V
Power Supply Voltages for All Power Modes							
AV_{DD} to AV_{SS}		Low power mode		2.7		3.6	V
		Mid power mode		2.7		3.6	
		Full power mode		2.7		3.6	
IOV_{DD} to GND				2		3.6	
AV_{SS} to GND				-1.8		0	
IOV_{DD} to AV_{SS}						TBD	
Power Supply Currents (10) (12)							
Power Supply Current (External Reference)	I_{AVDD}	Low power mode	Gain = 1 (1), all buffers off		235		μA
			Gain = 1 I_{AVDD} increase per AINx buffer (1)		40		
			Gain = 2 to 8		380		
			Gain = 16 to 128		425		
			I_{AVDD} increase per reference buffer (1), all gains		20		
		Mid power mode	Gain = 1 (1), all buffers off		280		μA
			Gain = 1 I_{AVDD} increase per AINx buffer (1)		65		
			Gain = 2 to 8		508		
			Gain = 16 to 128		595		
			I_{AVDD} increase per reference buffer (1), all gains		45		
		Full power mode	Gain = 1 (1), all buffers off		600		μA
			Gain = 1 I_{AVDD} increase per AINx buffer (1)		200		
			Gain = 2 to 8		1225		
			Gain = 16 to 128		1575		
			I_{AVDD} increase per reference buffer (1), all gains		120		
		I_{AVDD} increase	Due to internal reference (1), independent of power mode, the reference buffers are not required when using this reference		75		μA
			Due to V_{BIAS} (1), independent of power mode		85		
			Due to diagnostics (1)		60		

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 2V to 3.6V, AV_{SS} = DGND = 0V, REFINx(+) = 2.5V, REFINx(-) = AV_{SS}, master clock = 614.4kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current (External Reference)	I_{IOVDD}	Low power mode		35		μA
		Mid power mode		50		
		Full power mode		151		
Power-Down Currents (12) (Independent of Power Mode)						
Standby Current	I_{AVDD}	LDOs on only		25		μA
	I_{IOVDD}			12		
Power-Down Current	I_{AVDD}			0.5		μA
	I_{IOVDD}			0.5		

NOTES:

1. Although not production tested, these specifications are backed by characterization data during the initial product release.

2. FS represents the decimal equivalent of the FS[10:0] bits in the filter registers.

3. Nonlinearity is production tested solely in full power mode. For other power modes, this specification is supported by characterization data during the initial product release.

4. Post-system or internal zero-scale calibration, offset error aligns with the noise level for the programmed gain and selected output data rate. A system full-scale calibration diminishes gain error to the noise level for the programmed gain and output data rate.

5. Recalibration at any temperature eliminates these errors.

6. Gain error pertains to both positive and negative full-scale. Factory calibration occurs at gain = 1, T_A = +25℃.

7. For gain > 1, the common mode voltage ranges between (AV_{SS} + 0.1 + 0.5/gain) and (AV_{DD} - 0.1 - 0.5/gain).

8. Specification extends to a broader common mode voltage range between (AV_{SS} - 0.05 + 0.5/gain) and (AV_{DD} - 0.1 - 0.5/gain).

9. REJ60 is a bit within the filter registers. Setting REJ60 to 1 places a notch at 60Hz when the first notch of the Sinc filter is at 50Hz, thereby enabling simultaneous rejection of both 50Hz and 60Hz frequencies.

10. When gain exceeds 1, the analog input buffers activate automatically. Disabling the buffers is only feasible when gain equals 1.

11. With V_{REF} = (AV_{DD} - AV_{SS}), the typical differential input is 0.92 × V_{REF}/gain for low and mid power modes, and 0.86 × V_{REF}/gain for full power mode when gain > 1.

12. Digital inputs equate to either IOV_{DD} or DGND with excitation currents and bias voltage generator disabled.

13. These parameters are measured at T_A = -40℃ to +85℃.

TIMING SPECIFICATIONS

(Full power mode AV_{DD} = 2.7V to 3.6V, mid and low power mode AV_{DD} = 2.7V to 3.6V, IOV_{DD} = 2V to 3.6V, AV_{SS} = DGND = 0V, input logic 0 = 0V, input logic 1 = IOV_{DD}, unless otherwise noted.)

PARAMETER [1] [2]	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK High Pulse Width	t_3		100			ns
SCLK Low Pulse Width	t_4		100			ns
Delay between Consecutive Read/Write Operations	t_{12}	Low power mode	3/MCLK [3]			ns
		Mid power mode	12/MCLK			
		Full power mode	24/MCLK			
DOUT/nRDY High Time if DOUT/nRDY is Low and the Next Conversion is Available	t_{13}	Low power mode		6		μs
		Mid power mode		25		
		Full power mode		50		
nSYNC Low Pulse Width	t_{14}	Low power mode	3/MCLK			ns
		Mid power mode	12/MCLK			
		Full power mode	24/MCLK			
Read Operation						
nCS Falling Edge to DOUT/nRDY Active Time	t_1		0		80	ns
SCLK Active Edge to Data Valid Delay [5]	t_2 [4]		0		80	ns
Bus Relinquish Time after nCS Inactive Edge	t_5 [6] [7]		10		80	ns
SCLK Inactive Edge to nCS Inactive Edge	t_6		0			ns
SCLK Inactive Edge to DOUT/nRDY High	t_7 [8]	The DOUT_nRDY_DEL bit is cleared, the nCS_EN bit is cleared	10			ns
		The DOUT_nRDY_DEL bit is set, the nCS_EN bit is cleared	110			
Data Valid after nCS Inactive Edge	t_{7A} [7]	The nCS_EN Bit is Set	t_5			ns
Write Operation						
nCS Falling Edge to SCLK Active Edge Setup Time [5]	t_8		0			ns
Data Valid to SCLK Edge Setup Time	t_9		30			ns
Data Valid to SCLK Edge Hold Time	t_{10}		25			ns
nCS Rising Edge to SCLK Edge Hold Time	t_{11}		0			ns

NOTES:

1. These specifications underwent sample testing during the initial release to ensure compliance. All input signals are defined with t_R = t_F = 5ns (10% to 90% of IOV_{DD} and timed from a voltage level of IOV_{DD}/2).

2. Refer to timing diagrams.

3. MCLK denotes the master clock frequency.

4. These specifications are determined with the load circuit and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

5. The SCLK active edge corresponds to the falling edge of SCLK.

6. These specifications are derived from the measured time taken by the data output to change by 0.5V when loaded with the circuit. The measured value is then extrapolated back to remove the effects of charging or discharging the 25pF capacitor. The times provided in the timing characteristics represent the true bus relinquish times of the device and are therefore independent of external bus loading capacitances.

7. nRDY returns high after reading the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if necessary, while nRDY is high, although subsequent reads must not occur close to the next output update. In continuous read mode, the digital word can be read only once.

8. When the nCS_EN bit is cleared, the DOUT/nRDY pin transitions from its DOUT function to its nRDY function following the last inactive edge of the SCLK. When nCS_EN is set, the DOUT pin continues to output the LSB of the data until the nCS inactive edge.

FUNCTIONAL BLOCK DIAGRAM

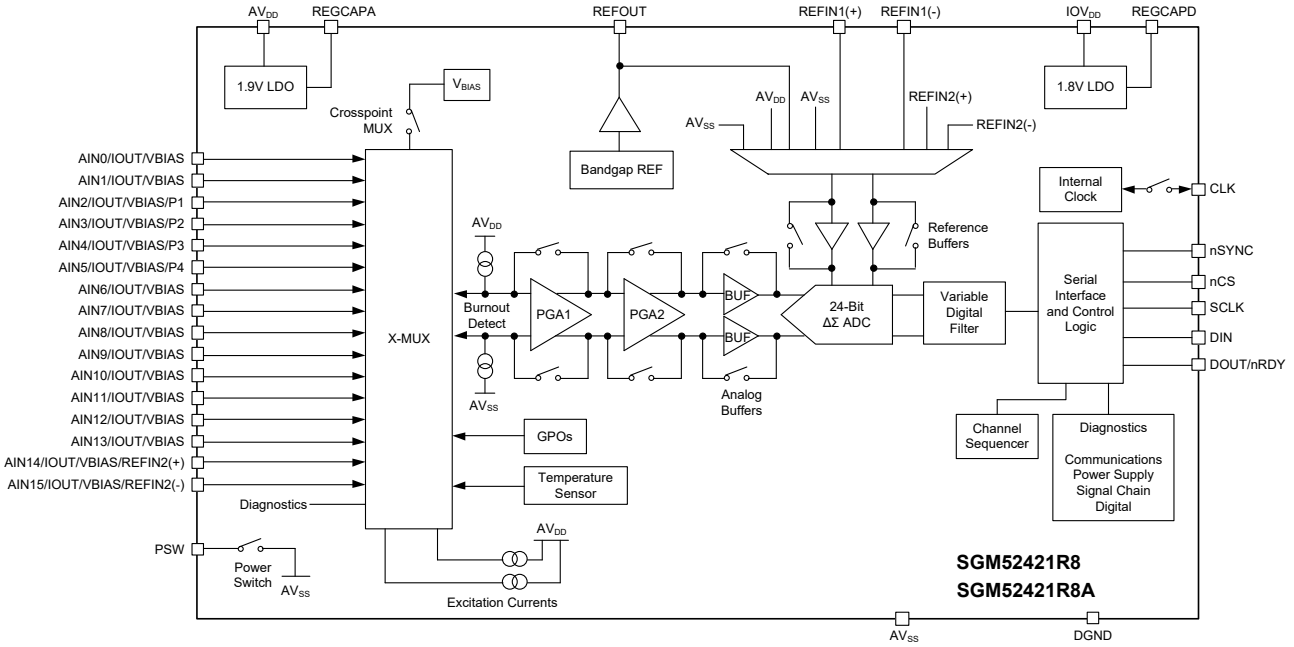


Figure 1. Block Diagram

RMS NOISE AND RESOLUTION

The RMS noise, effective resolution, peak-to-peak noise and noise-free (peak-to-peak) resolution for various output data rates, gain settings, and filters are shown in the below tables. Effective Resolution = Log_2 (Input Range/RMS Noise), and Peak-to-Peak Resolution = Log_2 (Input Range/Peak-to-Peak Noise).

Full Power Mode

Sinc[4]

Table 1. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.38	2.34	0.22(0.60)	0.13(0.74)	0.075(0.37)	0.060(0.30)	0.045(0.24)	0.035(0.17)	0.028(0.17)	0.026(0.11)
1920	10	2.5	0.30(0.60)	0.12(0.45)	0.088(0.37)	0.048(0.26)	0.054(0.26)	0.033(0.17)	0.029(0.14)	0.024(0.12)
960	20	5	0.32(1.19)	0.19(0.89)	0.11(0.37)	0.096(0.56)	0.071(0.35)	0.046(0.20)	0.046(0.20)	0.043(0.23)
480	40	10	0.35(1.19)	0.25(1.19)	0.17(0.82)	0.13(0.67)	0.10(0.52)	0.072(0.32)	0.053(0.26)	0.050(0.24)
384	50	12.5	0.42(1.79)	0.26(1.19)	0.16(0.67)	0.11(0.56)	0.11(0.54)	0.070(0.35)	0.053(0.25)	0.053(0.27)
320	60	15	0.72(1.49)	0.33(1.94)	0.19(0.67)	0.18(0.78)	0.13(0.65)	0.088(0.45)	0.071(0.37)	0.066(0.30)
240	80	20	0.46(2.38)	0.36(1.94)	0.26(1.12)	0.19(0.86)	0.13(0.60)	0.10(0.54)	0.077(0.36)	0.075(0.37)
120	160	40	0.67(2.98)	0.47(2.38)	0.27(1.42)	0.23(1.01)	0.15(0.84)	0.11(0.57)	0.11(0.49)	0.10(0.53)
60	320	80	0.80(4.17)	0.67(3.13)	0.43(2.46)	0.36(1.86)	0.26(1.28)	0.18(0.95)	0.16(1.04)	0.13(0.65)
30	640	160	1.59(8.64)	1.04(4.92)	0.60(2.83)	0.46(2.42)	0.42(1.99)	0.27(1.28)	0.23(1.43)	0.18(0.88)
15	1280	320	2.00(8.34)	1.54(7.30)	0.82(4.69)	0.72(3.84)	0.59(3.05)	0.32(1.73)	0.30(1.45)	0.31(1.56)
8	2400	600	2.73(13)	2.08(9.53)	0.98(4.77)	0.96(4.36)	0.72(2.98)	0.41(1.98)	0.39(1.89)	0.41(2.06)
4	4800	1200	3.39(19)	2.67(13)	1.76(9.53)	1.20(5.92)	1.08(5.34)	0.81(4.37)	0.61(2.73)	0.45(2.63)
2	9600	2400	4.60(25)	4.26(19)	2.31(13)	1.98(12)	1.59(7.54)	1.17(6.25)	0.84(4.76)	0.70(4.62)
1	19200	4800	8.24(44)	6.29(27)	4.26(18)	2.67(15)	2.23(11)	1.56(7.54)	1.24(7.09)	0.98(4.49)

Table 2. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.38	2.34	24(23)	24(21.7)	24(21.7)	23.3(21)	22.7(20.3)	22.1(19.8)	21.4(18.8)	20.5(18.5)
1920	10	2.5	24(23)	24(22.4)	23.8(21.7)	23.6(21.2)	22.5(20.2)	22.2(19.8)	21.4(19.1)	20.6(18.3)
960	20	5	23.9(22)	23.7(21.4)	23.5(21.7)	22.6(20.1)	22.1(19.8)	21.7(19.6)	20.7(18.5)	19.8(17.4)
480	40	10	23.8(22)	23.3(21)	22.8(20.5)	22.2(19.8)	21.6(19.2)	21.1(18.9)	20.5(18.2)	19.6(17.3)
384	50	12.5	23.5(21.4)	23.2(21)	22.9(20.8)	22.5(20.1)	21.4(19.1)	21.1(18.8)	20.5(18.3)	19.5(17.2)
320	60	15	22.7(21.7)	22.9(20.3)	22.7(20.8)	21.8(19.6)	21.2(18.9)	20.8(18.4)	20.1(17.7)	19.2(17)
240	80	20	23.4(21)	22.7(20.3)	22.2(20.1)	21.7(19.5)	21.2(19)	20.5(18.1)	20(17.7)	19(16.7)
120	160	40	22.8(20.7)	22.3(20)	22.1(19.8)	21.4(19.2)	21(18.5)	20.4(18.1)	19.5(17.3)	18.5(16.2)
60	320	80	22.6(20.2)	21.8(19.6)	21.5(19)	20.7(18.4)	20.2(17.9)	19.7(17.3)	18.9(16.2)	18.2(15.9)
30	640	160	21.6(19.1)	21.2(19)	21(18.8)	20.4(18)	19.5(17.3)	19.2(16.9)	18.4(15.7)	17.7(15.4)
15	1280	320	21.3(19.2)	20.6(18.4)	20.5(18)	19.7(17.3)	19(16.6)	18.9(16.5)	18(15.7)	16.9(14.6)
8	2400	600	20.8(18.6)	20.2(18)	20.3(18)	19.3(17.1)	18.7(16.7)	18.5(16.3)	17.6(15.3)	16.5(14.2)
4	4800	1200	20.5(18)	19.8(17.6)	19.4(17)	19(16.7)	18.1(15.8)	17.6(15.1)	17(14.8)	16.4(13.9)
2	9600	2400	20.1(17.6)	19.2(17)	19(16.6)	18.3(15.7)	17.6(15.3)	17(14.6)	16.5(14)	15.8(13)
1	19200	4800	19.2(16.8)	18.6(16.5)	18.2(16.1)	17.8(15.4)	17.1(14.8)	16.6(14.3)	15.9(13.4)	15.3(13.1)

RMS NOISE AND RESOLUTION (continued)

Sinc^3

Table 3. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.38	2.34	0.26(1.19)	0.16(0.74)	0.082(0.30)	0.069(0.37)	0.049(0.22)	0.032(0.14)	0.031(0.15)	0.025(0.12)
1920	10	2.5	0.13(0.60)	0.14(0.60)	0.091(0.30)	0.064(0.26)	0.048(0.28)	0.032(0.15)	0.030(0.14)	0.029(0.14)
1280	15	3.75	0.32(0.89)	0.16(0.74)	0.13(0.67)	0.085(0.41)	0.066(0.35)	0.045(0.25)	0.038(0.20)	0.036(0.17)
640	30	7.5	0.43(1.49)	0.24(1.19)	0.16(0.60)	0.11(0.48)	0.087(0.41)	0.070(0.44)	0.054(0.26)	0.040(0.18)
384	50	12.5	0.50(2.38)	0.31(1.19)	0.19(0.89)	0.15(0.71)	0.12(0.60)	0.073(0.37)	0.071(0.37)	0.065(0.30)
320	60	15	0.42(1.49)	0.31(1.19)	0.21(0.82)	0.15(0.78)	0.13(0.56)	0.096(0.46)	0.059(0.29)	0.069(0.32)
160	120	30	0.79(4.17)	0.45(1.64)	0.28(1.42)	0.24(1.34)	0.17(0.82)	0.11(0.75)	0.093(0.38)	0.090(0.48)
80	240	60	0.94(5.66)	0.60(3.13)	0.42(2.01)	0.25(1.19)	0.25(1.62)	0.16(0.73)	0.13(0.82)	0.14(0.71)
40	480	120	1.36(7.45)	0.94(4.47)	0.67(3.43)	0.44(2.12)	0.35(1.97)	0.28(1.34)	0.23(1.08)	0.21(0.98)
20	960	240	1.78(9.83)	1.47(6.41)	0.87(4.84)	0.62(2.83)	0.51(2.22)	0.32(1.78)	0.30(1.45)	0.27(1.38)
10	1920	480	2.50(12)	1.94(9.68)	1.34(6.63)	0.97(5.07)	0.77(4.36)	0.51(2.18)	0.44(2.40)	0.37(1.98)
6	3200	800	3.46(18)	2.54(14)	1.54(9.16)	1.18(6.70)	0.93(4.17)	0.67(2.91)	0.51(2.64)	0.45(2.26)
3	6400	1600	4.98(31)	3.63(20)	2.38(9.98)	1.51(8.23)	1.27(5.94)	0.85(4.21)	0.72(3.30)	0.67(4.05)
2	9600	2400	7.50(35)	4.60(26)	2.97(13)	2.06(13)	1.42(8.94)	1.20(4.87)	0.94(5.51)	0.85(3.80)
1	19200	4800	40(191)	20(89)	9.85(54)	6.01(30)	3.51(17)	2.04(9.93)	1.37(6.55)	1.25(6.65)

Table 4. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Full Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	9.38	2.34	24(22)	23.9(21.7)	23.9(22)	23.1(20.7)	22.6(20.4)	22.2(20.1)	21.2(19)	20.6(18.3)
1920	10	2.5	24(23)	24(22)	23.7(22)	23.2(21.2)	22.6(20.1)	22.2(20)	21.3(19.1)	20.4(18.1)
1280	15	3.75	23.9(22.4)	23.9(21.7)	23.2(20.8)	22.8(20.5)	22.2(19.8)	21.7(19.2)	21(18.5)	20.1(17.9)
640	30	7.5	23.5(21.7)	23.3(21)	22.9(21)	22.4(20.3)	21.8(19.5)	21.1(18.4)	20.5(18.2)	19.9(17.7)
384	50	12.5	23.3(21)	22.9(21)	22.7(20.4)	22(19.8)	21.3(19)	21(18.7)	20.1(17.7)	19.2(17)
320	60	15	23.5(21.7)	23(21)	22.5(20.5)	22(19.6)	21.2(19.1)	20.6(18.4)	20.3(18)	19.1(16.9)
160	120	30	22.6(20.2)	22.4(20.5)	22.1(19.8)	21.3(18.8)	20.8(18.5)	20.4(17.7)	19.7(17.6)	18.7(16.3)
80	240	60	22.3(19.8)	22(19.6)	21.5(19.2)	21.2(19)	20.2(17.6)	19.9(17.7)	19.2(16.5)	18.1(15.8)
40	480	120	21.8(19.4)	21.3(19.1)	20.8(18.5)	20.4(18.2)	19.8(17.3)	19.1(16.8)	18.4(16.1)	17.5(15.3)
20	960	240	21.4(19)	20.7(18.6)	20.5(18)	19.9(17.8)	19.2(17.1)	18.9(16.4)	18(15.7)	17.1(14.8)
10	1920	480	20.9(18.7)	20.3(18)	19.8(17.5)	19.3(16.9)	18.6(16.1)	18.2(16.1)	17.4(15)	16.7(14.3)
6	3200	800	20.5(18.1)	19.9(17.5)	19.6(17.1)	19(16.5)	18.4(16.2)	17.8(15.7)	17.2(14.9)	16.4(14.1)
3	6400	1600	19.9(17.3)	19.4(16.9)	19(16.9)	18.7(16.2)	17.9(15.7)	17.5(15.2)	16.7(14.5)	15.8(13.2)
2	9600	2400	19.3(17.1)	19.1(16.5)	18.7(16.5)	18.2(15.6)	17.7(15.1)	17(15)	16.3(13.8)	15.5(13.3)
1	19200	4800	16.9(14.7)	16.9(14.8)	17(14.5)	16.7(14.3)	16.4(14.2)	16.2(13.9)	15.8(13.5)	14.9(12.5)

RMS NOISE AND RESOLUTION (continued)

Post Filters

Table 5. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	0.43(2.09)	0.28(1.19)	0.17(0.82)	0.13(0.56)	0.12(0.56)	0.077(0.37)	0.072(0.38)	0.055(0.27)
20	0.47(2.38)	0.31(1.49)	0.20(0.97)	0.12(0.56)	0.11(0.48)	0.095(0.39)	0.066(0.31)	0.064(0.35)
25	0.43(2.09)	0.32(1.49)	0.20(1.04)	0.14(0.63)	0.13(0.61)	0.082(0.38)	0.069(0.30)	0.050(0.28)
27.27	0.53(2.38)	0.33(1.64)	0.20(0.97)	0.15(0.71)	0.13(0.54)	0.087(0.42)	0.073(0.31)	0.064(0.34)

Table 6. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	23.5(21.2)	23.1(21)	22.8(20.5)	22.2(20.1)	21.3(19.1)	21(18.7)	20(17.6)	19.4(17.1)
20	23.3(21)	22.9(20.7)	22.6(20.3)	22.3(20.1)	21.4(19.3)	20.7(18.6)	20.2(18)	19.2(16.8)
25	23.5(21.2)	22.9(20.7)	22.6(20.2)	22.1(19.9)	21.2(19)	20.9(18.6)	20.1(18)	19.6(17.1)
27.27	23.2(21)	22.8(20.5)	22.5(20.3)	22(19.8)	21.2(19.1)	20.8(18.5)	20(17.9)	19.2(16.8)

Fast Settling Filter ($Sinc^4$ + $Sinc^1$)

Table 7. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	3.13	0.17(0.60)	0.11(0.45)	0.066(0.30)	0.046(0.26)	0.038(0.19)	0.028(0.14)	0.023(0.14)	0.019(0.091)
120	10	0.26(1.19)	0.18(0.89)	0.11(0.67)	0.089(0.45)	0.068(0.30)	0.047(0.22)	0.037(0.16)	0.035(0.20)
24	50	0.53(2.38)	0.36(1.79)	0.25(1.64)	0.18(1.08)	0.15(0.63)	0.095(0.47)	0.099(0.49)	0.081(0.44)
20	60	0.67(3.28)	0.46(2.38)	0.27(1.42)	0.19(1.01)	0.16(0.80)	0.11(0.58)	0.074(0.40)	0.077(0.34)
2	600	1.97(9.24)	1.50(7.75)	0.79(3.87)	0.59(3.17)	0.51(2.81)	0.37(2.09)	0.30(1.79)	0.27(1.60)
1	1200	2.40(13)	1.91(9.83)	1.18(5.66)	0.98(4.51)	0.80(4.19)	0.51(2.31)	0.44(2.15)	0.41(2.15)

Table 8. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	3.13	24(23)	24(22.4)	24(22)	23.7(21.2)	23(20.7)	22.4(20.1)	21.7(19.1)	21(18.7)
120	10	24(22)	23.7(21.4)	23.4(20.8)	22.7(20.4)	22.1(20)	21.7(19.4)	21(18.9)	20.1(17.5)
24	50	23.2(21)	22.7(20.4)	22.2(19.5)	21.8(19.1)	21(18.9)	20.7(18.4)	19.6(17.3)	18.9(16.4)
20	60	22.8(20.5)	22.4(20)	22.2(19.8)	21.6(19.2)	20.9(18.6)	20.4(18)	20(17.6)	19(16.8)
2	600	21.3(19)	20.7(18.3)	20.6(18.3)	20(17.6)	19.2(16.8)	18.7(16.2)	18(15.4)	17.1(14.6)
1	1200	21(18.6)	20.3(18)	20(17.8)	19.3(17.1)	18.6(16.2)	18.2(16)	17.4(15.1)	16.5(14.1)

RMS NOISE AND RESOLUTION (continued)

Fast Settling Filter ($Sinc^3$ + $Sinc^1$)

Table 9. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	3.13	0.22(0.89)	0.12(0.60)	0.062(0.22)	0.048(0.22)	0.041(0.26)	0.025(0.12)	0.026(0.14)	0.021(0.10)
120	10	0.25(1.19)	0.18(0.74)	0.11(0.52)	0.077(0.37)	0.056(0.24)	0.047(0.26)	0.039(0.20)	0.041(0.18)
24	50	0.54(2.38)	0.47(2.68)	0.30(1.71)	0.19(1.15)	0.15(0.73)	0.10(0.54)	0.078(0.46)	0.079(0.39)
20	60	0.59(3.28)	0.42(2.09)	0.26(1.42)	0.22(1.12)	0.16(0.89)	0.12(0.68)	0.093(0.49)	0.085(0.46)
2	600	1.92(8.94)	1.52(8.19)	0.73(3.95)	0.65(3.13)	0.50(2.50)	0.40(2.57)	0.30(1.46)	0.26(1.32)
1	1200	3.31(17)	2.33(11)	1.31(5.96)	0.94(3.65)	0.78(3.76)	0.50(2.78)	0.42(2.22)	0.38(1.84)

Table 10. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Full Power Mode (Average by 16)

Filter Word (Dec.)	Output Data Rate (SPS)	Gain = 1	Gain = 2	*Gain = 4*	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
384	3.13	24(22.4)	24(22)	24(22.4)	23.6(21.4)	22.9(20.2)	22.6(20.3)	21.5(19.1)	20.9(18.5)
120	10	24(22)	23.7(21.7)	23.4(21.2)	22.9(20.7)	22.4(20.3)	21.7(19.2)	20.9(18.5)	19.9(17.7)
24	50	23.1(21)	22.3(19.8)	22(19.5)	21.6(19)	21(18.7)	20.5(18.1)	19.9(17.4)	18.9(16.6)
20	60	23(20.5)	22.5(20.2)	22.2(19.8)	21.4(19.1)	20.9(18.4)	20.3(17.8)	19.7(17.3)	18.8(16.4)
2	600	21.3(19.1)	20.7(18.2)	20.7(18.3)	19.9(17.6)	19.3(16.9)	18.6(15.9)	18(15.7)	17.2(14.9)
1	1200	20.5(18.1)	20(17.7)	19.9(17.7)	19.3(17.4)	18.6(16.3)	18.3(15.8)	17.5(15.1)	16.7(14.4)

RMS NOISE AND RESOLUTION (continued)

Mid Power Mode

Sinc[4]

Table 11. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.59	0.21(0.89)	0.13(0.60)	0.080(0.45)	0.054(0.34)	0.038(0.24)	0.029(0.15)	0.022(0.12)	0.021(0.10)
1920	2.5	0.63	0.21(0.89)	0.12(0.74)	0.077(0.37)	0.046(0.22)	0.046(0.22)	0.029(0.17)	0.025(0.13)	0.020(0.098)
960	5	1.25	0.26(1.19)	0.18(0.74)	0.092(0.52)	0.083(0.37)	0.063(0.32)	0.040(0.20)	0.039(0.20)	0.033(0.17)
480	10	2.5	0.29(1.49)	0.30(1.34)	0.15(0.74)	0.11(0.52)	0.081(0.47)	0.061(0.27)	0.050(0.25)	0.047(0.23)
240	20	5	0.51(2.68)	0.35(1.64)	0.23(1.04)	0.15(0.71)	0.13(0.65)	0.080(0.45)	0.065(0.38)	0.058(0.29)
120	40	10	0.77(4.17)	0.49(2.38)	0.27(1.27)	0.25(1.19)	0.17(0.82)	0.11(0.49)	0.10(0.44)	0.085(0.44)
96	50	12.5	0.79(3.87)	0.50(2.38)	0.31(1.42)	0.23(1.27)	0.22(1.10)	0.11(0.49)	0.098(0.56)	0.083(0.44)
80	60	15	0.99(3.87)	0.58(2.53)	0.30(1.64)	0.24(1.12)	0.20(1.21)	0.16(0.69)	0.11(0.48)	0.092(0.49)
60	80	20	0.87(4.47)	0.67(3.43)	0.42(2.16)	0.32(1.79)	0.26(1.25)	0.18(0.88)	0.14(0.82)	0.11(0.66)
30	160	40	1.57(8.94)	1.03(5.51)	0.54(2.83)	0.45(2.23)	0.34(1.49)	0.21(0.93)	0.23(1.22)	0.17(0.88)
15	320	80	1.91(10)	1.27(5.96)	0.82(4.47)	0.59(2.23)	0.48(2.42)	0.34(1.80)	0.29(1.28)	0.24(1.27)
8	600	150	2.62(13)	1.72(7.90)	1.29(5.51)	0.89(4.36)	0.66(2.77)	0.43(1.89)	0.31(1.79)	0.33(1.46)
4	1200	300	3.68(16)	2.54(13)	1.62(8.71)	1.38(6.74)	0.89(3.37)	0.58(2.58)	0.48(2.33)	0.48(2.65)
2	2400	600	4.63(22)	3.24(14)	2.43(12)	1.78(7.52)	1.40(6.96)	0.94(3.98)	0.79(4.12)	0.69(2.98)
1	4800	1200	8.01(44)	6.37(38)	3.88(19)	2.56(13)	2.19(10)	1.36(6.75)	1.16(5.36)	1.05(5.44)

Table 12. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.59	24(22.4)	24(22)	23.9(21.4)	23.5(20.8)	23(20.3)	22.3(20)	21.8(19.4)	20.9(18.5)
1920	2.5	0.63	24(22.4)	24(21.7)	24(21.7)	23.7(21.4)	22.7(20.4)	22.4(19.8)	21.6(19.2)	20.9(18.6)
960	5	1.25	24(22)	23.7(21.7)	23.7(21.2)	22.8(20.7)	22.2(19.9)	21.9(19.6)	20.9(18.6)	20.2(17.8)
480	10	2.5	24(21.7)	23(20.8)	23(20.7)	22.5(20.2)	21.9(19.4)	21.3(19.1)	20.6(18.2)	19.7(17.4)
240	20	5	23.2(20.8)	22.8(20.5)	22.4(20.2)	22(19.8)	21.2(18.9)	20.9(18.4)	20.2(17.6)	19.4(17)
120	40	10	22.6(20.2)	22.3(20)	22.2(19.9)	21.3(19)	20.8(18.5)	20.4(18.3)	19.6(17.4)	18.8(16.4)
96	50	12.5	22.6(20.3)	22.3(20)	21.9(19.8)	21.3(18.9)	20.5(18.1)	20.5(18.3)	19.6(17.1)	18.8(16.5)
80	60	15	22.3(20.3)	22(19.9)	22(19.5)	21.3(19.1)	20.6(18)	19.9(17.8)	19.4(17.3)	18.7(16.3)
60	80	20	22.5(20.1)	21.8(19.5)	21.5(19.1)	20.9(18.4)	20.2(17.9)	19.7(17.4)	19.1(16.5)	18.4(15.9)
30	160	40	21.6(19.1)	21.2(18.8)	21.2(18.8)	20.4(18.1)	19.8(17.7)	19.5(17.4)	18.4(16)	17.8(15.4)
15	320	80	21.3(18.9)	20.9(18.7)	20.5(18.1)	20(18.1)	19.3(17)	18.8(16.4)	18(15.9)	17.3(14.9)
8	600	150	20.9(18.6)	20.5(18.3)	19.9(17.8)	19.4(17.1)	18.9(16.8)	18.5(16.3)	17.9(15.4)	16.9(14.7)
4	1200	300	20.4(18.3)	19.9(17.6)	19.6(17.1)	18.8(16.5)	18.4(16.5)	18(15.9)	17.3(15)	16.3(13.8)
2	2400	600	20(17.8)	19.6(17.4)	19(16.7)	18.4(16.3)	17.8(15.5)	17.3(15.3)	16.6(14.2)	15.8(13.7)
1	4800	1200	19.3(16.8)	18.6(16)	18.3(16)	17.9(15.5)	17.1(14.9)	16.8(14.5)	16(13.8)	15.2(12.8)

RMS NOISE AND RESOLUTION (continued)

Sinc^3

Table 13. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.59	0.23(1.19)	0.15(0.74)	0.086(0.37)	0.056(0.26)	0.041(0.20)	0.029(0.14)	0.026(0.12)	0.024(0.14)
960	5	1.25	0.24(1.19)	0.19(1.04)	0.12(0.52)	0.096(0.45)	0.074(0.39)	0.053(0.28)	0.039(0.18)	0.035(0.17)
480	10	2.5	0.30(1.79)	0.26(1.19)	0.15(0.74)	0.12(0.56)	0.085(0.35)	0.068(0.33)	0.051(0.29)	0.041(0.20)
320	15	3.75	0.48(2.38)	0.34(1.49)	0.24(1.19)	0.14(0.67)	0.11(0.60)	0.068(0.34)	0.053(0.26)	0.060(0.30)
160	30	7.5	0.66(2.38)	0.51(2.83)	0.28(1.19)	0.22(1.27)	0.17(0.86)	0.11(0.79)	0.079(0.42)	0.079(0.42)
96	50	12.5	0.75(3.87)	0.61(2.53)	0.42(2.01)	0.27(1.15)	0.23(0.97)	0.13(0.64)	0.11(0.66)	0.097(0.57)
80	60	15	0.98(5.07)	0.65(3.13)	0.42(2.16)	0.30(1.60)	0.23(1.12)	0.17(1.02)	0.12(0.66)	0.10(0.42)
40	120	30	1.42(5.96)	0.72(4.02)	0.54(2.16)	0.34(1.64)	0.30(1.84)	0.20(0.97)	0.17(0.88)	0.17(0.92)
20	240	60	1.61(9.53)	1.39(7.30)	0.90(4.69)	0.58(2.72)	0.42(1.88)	0.33(1.73)	0.25(1.24)	0.19(1.06)
10	480	120	2.66(13)	1.81(8.94)	1.16(7.08)	0.76(4.25)	0.59(3.20)	0.45(2.18)	0.36(1.76)	0.28(1.28)
5	960	240	3.40(15)	2.35(11)	1.63(7.90)	1.21(5.18)	0.88(4.47)	0.60(3.11)	0.49(2.80)	0.41(2.07)
3	1600	400	4.85(21)	3.53(18)	1.98(9.31)	1.54(9.05)	1.14(5.68)	0.77(4.08)	0.63(3.48)	0.50(2.98)
2	2400	600	7.33(35)	4.99(25)	2.91(13)	1.84(9.12)	1.42(5.87)	0.90(4.92)	0.82(3.50)	0.71(3.30)
1	4800	1200	40(203)	21(127)	9.17(44)	6.54(33)	3.47(17)	2.15(10)	1.29(6.95)	1.18(5.66)

Table 14. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	2.34	0.59	24(22)	24(21.7)	23.8(21.7)	23.4(21.2)	22.9(20.5)	22.4(20.1)	21.5(19.4)	20.6(18.1)
960	5	1.25	24(22)	23.6(21.2)	23.3(21.2)	22.6(20.4)	22(19.6)	21.5(19.1)	20.9(18.8)	20.1(17.8)
480	10	2.5	24(21.4)	23.2(21)	23(20.7)	22.3(20.1)	21.8(19.8)	21.1(18.9)	20.5(18)	19.9(17.6)
320	15	3.75	23.3(21)	22.8(20.7)	22.3(20)	22(19.8)	21.5(19)	21.1(18.8)	20.5(18.2)	19.3(17)
160	30	7.5	22.8(21)	22.2(19.8)	22.1(20)	21.4(18.9)	20.8(18.5)	20.4(17.6)	19.9(17.5)	18.9(16.5)
96	50	12.5	22.7(20.3)	22(19.9)	21.5(19.2)	21.2(19)	20.4(18.3)	20.2(17.9)	19.4(16.9)	18.6(16.1)
80	60	15	22.3(19.9)	21.9(19.6)	21.5(19.1)	21(18.6)	20.4(18.1)	19.8(17.2)	19.3(16.9)	18.5(16.5)
40	120	30	21.7(19.7)	21.7(19.2)	21.1(19.1)	20.8(18.5)	20(17.4)	19.6(17.3)	18.8(16.4)	17.8(15.4)
20	240	60	21.6(19)	20.8(18.4)	20.4(18)	20(17.8)	19.5(17.3)	18.8(16.5)	18.3(15.9)	17.6(15.2)
10	480	120	20.8(18.5)	20.4(18.1)	20(17.4)	19.6(17.2)	19(16.6)	18.4(16.1)	17.7(15.4)	17.1(14.9)
5	960	240	20.5(18.3)	20(17.8)	19.5(17.3)	19(16.9)	18.4(16.1)	18(15.6)	17.3(14.8)	16.5(14.2)
3	1600	400	20(17.9)	19.4(17.1)	19.3(17)	18.6(16.1)	18.1(15.7)	17.6(15.2)	16.9(14.5)	16.2(13.7)
2	2400	600	19.4(17.1)	18.9(16.6)	18.7(16.5)	18.4(16.1)	17.8(15.7)	17.4(15)	16.5(14.4)	15.7(13.5)
1	4800	1200	16.9(14.6)	16.9(14.3)	17.1(14.8)	16.5(14.2)	16.5(14.2)	16.1(13.9)	15.9(13.5)	15(12.8)

RMS NOISE AND RESOLUTION (continued)

Post Filters

Table 15. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Mid Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	0.79(5.07)	0.62(3.58)	0.39(1.71)	0.26(1.27)	0.21(0.99)	0.14(0.60)	0.11(0.66)	0.10(0.50)
20	0.82(4.47)	0.63(2.83)	0.39(2.09)	0.28(1.71)	0.20(1.10)	0.13(0.77)	0.11(0.52)	0.12(0.59)
25	0.93(5.07)	0.57(2.98)	0.33(2.01)	0.28(1.45)	0.26(1.30)	0.15(0.69)	0.11(0.64)	0.11(0.48)
27.27	0.87(4.47)	0.67(3.43)	0.40(1.86)	0.35(1.56)	0.22(1.23)	0.16(0.80)	0.11(0.50)	0.13(0.61)

Table 16. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	22.6(19.9)	21.9(19.4)	21.6(19.5)	21.2(18.9)	20.5(18.3)	20.1(18)	19.5(16.9)	18.6(16.3)
20	22.5(20.1)	21.9(19.8)	21.6(19.2)	21.1(18.5)	20.6(18.1)	20.2(17.6)	19.4(17.2)	18.3(16)
25	22.4(19.9)	22.1(19.7)	21.8(19.2)	21.1(18.7)	20.2(17.9)	20(17.8)	19.4(16.9)	18.5(16.3)
27.27	22.4(20.1)	21.8(19.5)	21.6(19.4)	20.8(18.6)	20.4(18)	19.9(17.6)	19.4(17.3)	18.2(16)

Fast Settling Filter ($Sinc^4$ + $Sinc^1$)

Table 17. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.13	0.27(1.49)	0.19(0.89)	0.13(0.67)	0.082(0.48)	0.068(0.32)	0.055(0.25)	0.042(0.23)	0.035(0.19)
30	10	0.46(2.38)	0.33(1.64)	0.20(1.04)	0.17(0.82)	0.11(0.61)	0.087(0.41)	0.065(0.36)	0.060(0.28)
6	50	1.03(4.47)	0.83(3.87)	0.44(2.09)	0.41(2.01)	0.29(1.30)	0.16(0.75)	0.15(0.73)	0.12(0.61)
5	60	1.23(5.96)	0.93(5.81)	0.52(2.76)	0.34(1.64)	0.29(1.64)	0.22(1.15)	0.17(0.91)	0.13(0.64)
2	150	1.54(7.75)	1.50(7.00)	0.80(4.69)	0.65(2.79)	0.48(2.90)	0.35(1.64)	0.27(1.32)	0.21(1.18)
1	300	2.10(11)	1.91(9.09)	1.12(5.74)	0.87(3.95)	0.78(3.59)	0.41(1.93)	0.39(1.85)	0.34(1.56)

Table 18. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.13	24(21.7)	23.7(21.4)	23.2(20.8)	22.9(20.3)	22.1(19.9)	21.4(19.2)	20.8(18.4)	20.1(17.7)
30	10	23.4(21)	22.8(20.5)	22.6(20.2)	21.8(19.5)	21.4(19)	20.8(18.5)	20.2(17.7)	19.3(17.1)
6	50	22.2(20.1)	21.5(19.3)	21.4(19.2)	20.6(18.2)	20(17.9)	19.9(17.7)	19(16.7)	18.3(16)
5	60	22(19.7)	21.4(18.7)	21.2(18.8)	20.8(18.5)	20(17.5)	19.5(17.1)	18.8(16.4)	18.2(15.9)
2	150	21.6(19.3)	20.7(18.4)	20.6(18)	19.9(17.8)	19.3(16.7)	18.8(16.5)	18.2(15.9)	17.5(15)
1	300	21.2(18.8)	20.3(18.1)	20.1(17.7)	19.5(17.3)	18.6(16.4)	18.5(16.3)	17.6(15.4)	16.8(14.6)

RMS NOISE AND RESOLUTION (continued)

Fast Settling Filter ($Sinc^3$ + $Sinc^1$)

Table 19. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.13	0.30(1.79)	0.18(0.74)	0.11(0.52)	0.090(0.52)	0.067(0.34)	0.046(0.23)	0.039(0.16)	0.032(0.17)
30	10	0.54(2.68)	0.34(1.79)	0.22(0.97)	0.16(0.82)	0.12(0.65)	0.083(0.49)	0.073(0.32)	0.064(0.35)
6	50	1.22(5.96)	0.83(4.77)	0.45(2.53)	0.39(2.09)	0.24(1.38)	0.19(0.93)	0.16(0.96)	0.15(0.87)
5	60	1.23(7.15)	0.85(4.47)	0.54(2.61)	0.39(1.71)	0.31(1.79)	0.21(1.01)	0.17(0.88)	0.14(0.79)
2	150	1.89(9.24)	1.29(5.21)	0.73(4.32)	0.59(3.39)	0.44(2.14)	0.33(1.50)	0.30(1.35)	0.23(1.32)
1	300	3.33(20)	2.04(9.24)	1.38(7.00)	0.81(4.84)	0.66(3.07)	0.41(1.76)	0.42(2.25)	0.35(1.82)

Table 20. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Mid Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.13	24(21.4)	23.7(21.7)	23.5(21.2)	22.7(20.2)	22.2(19.8)	21.7(19.4)	20.9(18.9)	20.2(17.9)
30	10	23.1(20.8)	22.8(20.4)	22.4(20.3)	21.9(19.5)	21.3(18.9)	20.8(18.3)	20(17.9)	19.2(16.8)
6	50	22(19.7)	21.5(19)	21.4(18.9)	20.6(18.2)	20.3(17.8)	19.7(17.4)	18.9(16.3)	18(15.4)
5	60	22(19.4)	21.5(19.1)	21.1(18.9)	20.6(18.5)	20(17.4)	19.5(17.2)	18.8(16.4)	18.1(15.6)
2	150	21.3(19)	20.9(18.9)	20.7(18.1)	20(17.5)	19.4(17.2)	18.8(16.7)	18(15.8)	17.4(14.9)
1	300	20.5(18)	20.2(18)	19.8(17.4)	19.6(17)	18.8(16.6)	18.5(16.4)	17.5(15.1)	16.8(14.4)

RMS NOISE AND RESOLUTION (continued)

Low Power Mode

Sinc[4]

Table 21. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.29	0.21(0.60)	0.14(0.60)	0.080(0.37)	0.058(0.26)	0.046(0.19)	0.028(0.17)	0.022(0.11)	0.021(0.098)
1920	1.25	0.31	0.30(0.60)	0.15(0.89)	0.085(0.30)	0.058(0.26)	0.043(0.22)	0.023(0.12)	0.019(0.093)	0.019(0.10)
960	2.5	0.63	0.29(1.19)	0.16(0.89)	0.12(0.60)	0.073(0.37)	0.072(0.41)	0.041(0.20)	0.035(0.16)	0.028(0.14)
480	5	1.25	0.41(1.79)	0.26(1.19)	0.14(0.67)	0.12(0.56)	0.086(0.41)	0.059(0.32)	0.042(0.21)	0.040(0.25)
496	4.84	1.21	0.26(1.49)	0.29(1.34)	0.16(0.82)	0.11(0.56)	0.086(0.41)	0.051(0.25)	0.040(0.20)	0.038(0.17)
120	20	5	0.61(2.68)	0.48(2.23)	0.27(1.19)	0.25(1.23)	0.18(0.80)	0.12(0.54)	0.097(0.47)	0.084(0.42)
60	40	10	0.84(3.87)	0.71(3.43)	0.43(2.16)	0.35(1.75)	0.25(1.23)	0.16(0.78)	0.13(0.66)	0.12(0.56)
48	50	12.5	1.08(4.47)	0.73(4.02)	0.53(2.83)	0.33(1.71)	0.26(1.34)	0.18(0.97)	0.13(0.66)	0.11(0.53)
40	60	15	1.05(5.07)	0.84(3.72)	0.47(2.23)	0.35(1.79)	0.35(1.55)	0.22(1.22)	0.13(0.59)	0.14(0.58)
30	80	20	1.46(7.15)	0.96(4.02)	0.50(2.38)	0.40(1.75)	0.37(1.75)	0.23(1.12)	0.19(0.89)	0.14(0.72)
15	160	40	1.63(9.24)	1.62(7.60)	0.89(4.47)	0.63(3.69)	0.46(2.10)	0.34(1.68)	0.26(1.19)	0.23(1.06)
8	300	75	2.61(13)	2.08(11)	1.38(7.08)	0.99(5.18)	0.73(3.37)	0.42(1.69)	0.34(2.03)	0.33(1.59)
4	600	150	3.59(19)	2.98(17)	1.64(7.08)	1.30(7.11)	0.94(5.36)	0.54(2.78)	0.46(2.63)	0.48(2.23)
2	1200	300	5.34(25)	4.62(22)	2.36(13)	1.67(8.71)	1.40(7.93)	0.82(5.65)	0.65(3.43)	0.71(3.45)
1	2400	600	9.09(41)	7.21(40)	3.49(21)	2.98(15)	2.37(13)	1.47(6.26)	1.08(5.21)	1.07(4.49)

Table 22. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.29	24(23)	24(22)	23.9(21.7)	23.4(21.2)	22.7(20.7)	22.4(19.8)	21.7(19.5)	20.9(18.6)
1920	1.25	0.31	24(23)	24(21.4)	23.8(22)	23.4(21.2)	22.8(20.4)	22.7(20.3)	22(19.7)	21(18.6)
960	2.5	0.63	24(22)	23.9(21.4)	23.3(21)	23(20.7)	22(19.5)	21.9(19.5)	21.1(18.9)	20.4(18.1)
480	5	1.25	23.5(21.4)	23.2(21)	23.1(20.8)	22.3(20.1)	21.8(19.5)	21.3(18.9)	20.8(18.5)	19.9(17.3)
496	4.84	1.21	24(21.7)	23(20.8)	22.9(20.5)	22.4(20.1)	21.8(19.5)	21.5(19.2)	20.9(18.6)	20(17.8)
120	20	5	23(20.8)	22.3(20.1)	22.1(20)	21.2(19)	20.7(18.6)	20.4(18.1)	19.6(17.3)	18.8(16.5)
60	40	10	22.5(20.3)	21.8(19.5)	21.5(19.1)	20.8(18.4)	20.2(18)	19.9(17.6)	19.2(16.9)	18.3(16.1)
48	50	12.5	22.1(20.1)	21.7(19.2)	21.2(18.8)	20.8(18.5)	20.2(17.8)	19.7(17.3)	19.2(16.9)	18.5(16.2)
40	60	15	22.2(19.9)	21.5(19.4)	21.4(19.1)	20.8(18.4)	19.8(17.6)	19.5(17)	19.2(17)	18.1(16)
30	80	20	21.7(19.4)	21.3(19.2)	21.3(19)	20.6(18.4)	19.7(17.4)	19.4(17.1)	18.6(16.4)	18.1(15.7)
15	160	40	21.6(19)	20.6(18.3)	20.4(18.1)	19.9(17.4)	19.4(17.2)	18.8(16.5)	18.2(16)	17.4(15.2)
8	300	75	20.9(18.6)	20.2(17.8)	19.8(17.4)	19.3(16.9)	18.7(16.5)	18.5(16.5)	17.8(15.2)	16.9(14.6)
4	600	150	20.4(18)	19.7(17.1)	19.5(17.4)	18.9(16.4)	18.3(15.8)	18.1(15.8)	17.4(14.9)	16.3(14.1)
2	1200	300	19.8(17.6)	19(16.8)	19(16.6)	18.5(16.1)	17.8(15.3)	17.5(14.8)	16.9(14.5)	15.8(13.5)
1	2400	600	19.1(16.9)	18.4(15.9)	18.4(15.9)	17.7(15.3)	17(14.5)	16.7(14.6)	16.1(13.9)	15.2(13.1)

RMS NOISE AND RESOLUTION (continued)

Sinc^3

Table 23. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.29	0.19(0.89)	0.13(0.60)	0.075(0.45)	0.059(0.34)	0.045(0.22)	0.034(0.20)	0.025(0.13)	0.021(0.098)
480	5	1.25	0.31(1.79)	0.26(1.34)	0.14(0.82)	0.12(0.56)	0.089(0.48)	0.056(0.32)	0.051(0.26)	0.044(0.20)
240	10	2.5	0.51(2.68)	0.33(1.64)	0.22(1.04)	0.18(0.82)	0.13(0.63)	0.095(0.54)	0.064(0.34)	0.061(0.26)
160	15	3.75	0.74(3.58)	0.48(1.94)	0.29(1.34)	0.21(0.89)	0.16(0.78)	0.095(0.48)	0.077(0.36)	0.078(0.40)
80	30	7.5	0.87(4.17)	0.55(3.28)	0.37(1.64)	0.27(1.30)	0.25(1.15)	0.15(0.76)	0.12(0.50)	0.11(0.47)
48	50	12.5	1.16(5.36)	0.88(4.62)	0.50(2.76)	0.34(1.45)	0.27(1.27)	0.20(0.87)	0.14(0.63)	0.14(0.71)
40	60	15	1.32(7.45)	0.95(4.32)	0.60(3.05)	0.49(2.76)	0.31(1.32)	0.22(1.19)	0.17(0.84)	0.11(0.51)
20	120	30	1.90(8.94)	1.13(4.32)	0.75(3.43)	0.65(3.35)	0.49(2.76)	0.28(1.17)	0.24(1.08)	0.22(1.07)
10	240	60	2.70(14)	1.68(9.39)	1.07(5.29)	0.74(3.58)	0.52(2.94)	0.48(2.51)	0.33(1.64)	0.29(1.64)
5	480	120	3.16(15)	2.70(12)	1.62(8.49)	1.21(5.77)	0.82(3.71)	0.57(2.64)	0.53(2.34)	0.39(1.88)
3	800	200	4.26(20)	3.38(17)	2.23(12)	1.63(11)	1.09(5.55)	0.73(3.59)	0.65(3.38)	0.61(2.70)
2	1200	300	8.12(44)	5.30(28)	3.21(15)	2.00(9.91)	1.59(8.34)	0.97(5.51)	0.75(4.15)	0.67(3.60)
1	2400	600	39(203)	22(146)	9.07(48)	6.06(32)	3.09(14)	1.95(10)	1.22(5.95)	1.16(5.95)

Table 24. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate, Low Power Mode

Filter Word (Dec.)	Output Data Rate (SPS)	Output Data Rate (Zero Latency Mode) (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
2047	1.17	0.29	24(22.4)	24(22)	24(21.4)	23.3(20.8)	22.7(20.4)	22.1(19.5)	21.6(19.2)	20.8(18.6)
480	5	1.25	23.9(21.4)	23.2(20.8)	23.1(20.5)	22.4(20.1)	21.7(19.3)	21.4(18.9)	20.5(18.2)	19.8(17.6)
240	10	2.5	23.2(20.8)	22.8(20.5)	22.4(20.2)	21.7(19.5)	21.2(18.9)	20.6(18.1)	20.2(17.8)	19.3(17.2)
160	15	3.75	22.7(20.4)	22.3(20.3)	22.1(19.8)	21.5(19.4)	20.9(18.6)	20.6(18.3)	20(17.7)	18.9(16.6)
80	30	7.5	22.5(20.2)	22.1(19.5)	21.7(19.5)	21.2(18.9)	20.2(18)	20(17.6)	19.3(17.2)	18.4(16.3)
48	50	12.5	22(19.8)	21.4(19)	21.3(18.8)	20.8(18.7)	20.2(17.9)	19.6(17.5)	19.1(16.9)	18.1(15.8)
40	60	15	21.9(19.4)	21.3(19.1)	21(18.6)	20.3(17.8)	20(17.9)	19.4(17)	18.8(16.5)	18.4(16.2)
20	120	30	21.3(19.1)	21.1(19.1)	20.7(18.5)	19.9(17.5)	19.3(16.8)	19.1(17)	18.3(16.1)	17.4(15.2)
10	240	60	20.8(18.5)	20.5(18)	20.2(17.9)	19.7(17.4)	19.2(16.7)	18.3(15.9)	17.9(15.5)	17(14.5)
5	480	120	20.6(18.3)	19.8(17.7)	19.6(17.2)	19(16.7)	18.5(16.4)	18.1(15.9)	17.2(15)	16.6(14.3)
3	800	200	20.2(17.9)	19.5(17.2)	19.1(16.7)	18.6(15.8)	18.1(15.8)	17.7(15.4)	16.9(14.5)	16(13.8)
2	1200	300	19.2(16.8)	18.8(16.5)	18.6(16.4)	18.3(15.9)	17.6(15.2)	17.3(14.8)	16.7(14.2)	15.8(13.4)
1	2400	600	17(14.6)	16.8(14.1)	17.1(14.7)	16.7(14.3)	16.6(14.4)	16.3(13.9)	16(13.7)	15(12.7)

RMS NOISE AND RESOLUTION (continued)

Post Filters

Table 25. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	1.00(5.07)	0.68(4.02)	0.50(2.98)	0.38(2.05)	0.29(1.69)	0.17(0.76)	0.15(0.77)	0.12(0.69)
20	1.09(5.36)	0.86(4.02)	0.47(2.31)	0.37(1.64)	0.26(1.34)	0.19(0.91)	0.15(0.66)	0.14(0.77)
25	1.24(5.96)	0.90(4.32)	0.58(2.46)	0.49(2.20)	0.35(1.81)	0.16(0.71)	0.16(0.83)	0.16(0.71)
27.27	1.18(5.36)	0.97(4.92)	0.61(3.50)	0.42(2.01)	0.32(1.73)	0.22(1.11)	0.18(0.86)	0.14(0.68)

Table 26. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode

Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
16.67	22.3(19.9)	21.8(19.2)	21.3(18.7)	20.7(18.2)	20.1(17.5)	19.8(17.6)	19(16.6)	18.3(15.8)
20	22.1(19.8)	21.5(19.2)	21.3(19)	20.7(18.5)	20.2(17.8)	19.6(17.4)	19(16.9)	18.1(15.6)
25	21.9(19.7)	21.4(19.1)	21(19)	20.3(18.1)	19.8(17.4)	19.9(17.8)	18.9(16.5)	17.9(15.8)
27.27	22(19.8)	21.3(19)	21(18.4)	20.5(18.2)	19.9(17.5)	19.4(17.1)	18.7(16.5)	18.1(15.8)

Fast Settling Filter ($Sinc^4$ + $Sinc^1$)

Table 27. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.57	0.42(2.09)	0.31(1.49)	0.16(0.82)	0.13(0.60)	0.096(0.50)	0.069(0.32)	0.045(0.23)	0.044(0.23)
30	11.43	0.64(3.28)	0.50(2.23)	0.34(1.79)	0.24(1.30)	0.16(0.82)	0.11(0.55)	0.083(0.45)	0.090(0.47)
6	57.14	1.38(6.85)	1.06(5.51)	0.61(2.90)	0.46(2.31)	0.40(2.18)	0.24(1.10)	0.20(1.02)	0.19(1.04)
5	68.57	1.62(8.64)	1.11(6.55)	0.81(4.62)	0.57(2.53)	0.45(2.23)	0.28(1.39)	0.22(1.10)	0.17(0.74)
2	171.43	2.53(13)	1.96(9.68)	1.18(5.51)	0.92(4.21)	0.66(3.80)	0.45(2.17)	0.33(1.62)	0.30(1.64)
1	342.86	4.09(21)	2.74(16)	1.78(9.09)	1.34(6.70)	0.92(4.54)	0.67(3.58)	0.47(2.74)	0.37(2.03)

Table 28. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.57	23.5(21.2)	22.9(20.7)	22.9(20.5)	22.2(20)	21.6(19.2)	21.1(18.9)	20.7(18.4)	19.8(17.4)
30	11.43	22.9(20.5)	22.3(20.1)	21.8(19.4)	21.3(18.9)	20.9(18.5)	20.4(18.1)	19.8(17.4)	18.7(16.3)
6	57.14	21.8(19.5)	21.2(18.8)	21(18.7)	20.4(18)	19.6(17.1)	19.3(17.1)	18.6(16.2)	17.7(15.2)
5	68.57	21.6(19.1)	21.1(18.5)	20.6(18)	20.1(17.9)	19.4(17.1)	19.1(16.8)	18.4(16.1)	17.8(15.7)
2	171.43	20.9(18.5)	20.3(18)	20(17.8)	19.4(17.2)	18.9(16.3)	18.4(16.1)	17.8(15.6)	17(14.5)
1	342.86	20.2(17.8)	19.8(17.3)	19.4(17.1)	18.8(16.5)	18.4(16.1)	17.8(15.4)	17.4(14.8)	16.7(14.2)

RMS NOISE AND RESOLUTION (continued)

Fast Settling Filter ($Sinc^3$ + $Sinc^1$)

Table 29. RMS Noise (Peak-to-Peak Noise) vs. Gain and Output Data Rate (μV), Low Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.57	0.42(1.49)	0.31(1.64)	0.16(0.74)	0.13(0.63)	0.094(0.45)	0.070(0.42)	0.045(0.20)	0.047(0.23)
30	11.43	0.61(2.68)	0.50(2.38)	0.27(1.34)	0.23(1.01)	0.17(0.78)	0.11(0.54)	0.10(0.53)	0.084(0.34)
6	57.14	1.51(7.45)	1.16(5.07)	0.65(4.17)	0.59(2.76)	0.39(1.92)	0.26(1.18)	0.20(0.95)	0.19(0.97)
5	68.57	1.50(8.64)	1.11(5.96)	0.75(3.35)	0.54(2.64)	0.38(1.73)	0.28(1.32)	0.23(1.04)	0.20(0.99)
2	171.43	2.59(13)	1.89(12)	1.12(6.11)	0.94(3.91)	0.67(3.43)	0.44(2.52)	0.33(1.60)	0.29(1.38)
1	342.86	4.69(24)	3.27(15)	1.78(8.34)	1.41(8.12)	0.95(5.96)	0.68(3.17)	0.50(2.38)	0.47(2.21)

Table 30. Effective Resolution (Peak-to-Peak Resolution) vs. Gain and Output Data Rate (Bits), Low Power Mode (Average by 16)

Filter Word (Dec.)	Output Date Rate (SPS)	Gain = 1	Gain = 2	Gain = 4	Gain = 8	Gain = 16	Gain = 32	Gain = 64	Gain = 128
96	3.57	23.5(21.7)	23(20.5)	22.9(20.7)	22.2(19.9)	21.7(19.4)	21.1(18.5)	20.7(18.5)	19.7(17.4)
30	11.43	23(20.8)	22.3(20)	22.2(19.8)	21.3(19.2)	20.9(18.6)	20.4(18.1)	19.5(17.2)	18.8(16.8)
6	57.14	21.7(19.4)	21(18.9)	20.9(18.2)	20(17.8)	19.6(17.3)	19.2(17)	18.6(16.3)	17.7(15.3)
5	68.57	21.7(19.1)	21.1(18.7)	20.7(18.5)	20.1(17.9)	19.7(17.5)	19.1(16.9)	18.4(16.2)	17.6(15.3)
2	171.43	20.9(18.5)	20.3(17.7)	20.1(17.6)	19.3(17.3)	18.8(16.5)	18.4(15.9)	17.8(15.6)	17(14.8)
1	342.86	20(17.7)	19.5(17.3)	19.4(17.2)	18.8(16.2)	18.3(15.7)	17.8(15.6)	17.3(15)	16.3(14.1)

REGISTERS MAPS

Table 31. Register Maps

Addr.	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x00	Communications	nWEN	R/$\overline{W}$	RS[5:0]						0x00	W
0x00	Status	nRDY	ERROR_FLAG	0	POR_FLAG	CH_ACTIVE[3:0]				0x00	R
0x01	ADC_CONTROL	0			DOUT_nRDY_DEL	CONT_READ	DATA_STATUS	nCS_EN	REF_EN	0x0000	R/W
		POWER_MODE[1:0]		Mode[3:0]				CLK_SEL[1:0]			
0x02	Data	Data[23:16]								0x000000	R
		Data[15:8]									
		Data[7:0]									
0x03	IO_CONTROL_1	GPIO_DAT4	GPIO_DAT3	GPIO_DAT2	GPIO_DAT1	GPIO_CTRL4	GPIO_CTRL3	GPIO_CTRL2	GPIO_CTRL1	0x000000	R/W
		PDSW	0	IOUT1[2:0]		IOUT0[2:0]					
		IOUT1_CH[3:0]				IOUT0_CH[3:0]					
0x04	IO_CONTROL_2	VBIAS15	VBIAS14	VBIAS13	VBIAS12	VBIAS11	VBIAS10	VBIAS9	VBIAS8	0x0000	R/W
		VBIAS7	VBIAS6	VBIAS5	VBIAS4	VBIAS3	VBIAS2	VBIAS1	VBIAS0		
0x05	ID	DEVICE_ID[3:0]				SILICON_REVISION[3:0]				0x18	R
0x06	Error	0				LDO_CAP_ERR	ADC_CAL_ERR	ADC_CONV_ERR	ADC_SAT_ERR	0x000000	R
		AINP_OV_ERR	AINP_UV_ERR	AINM_OV_ERR	AINM_UV_ERR	REF_DET_ERR	0	DLDO_PSM_ERR	0		
		ALDO_PSM_ERR	SPI_IGNORE_ERR	SPI_SCLK_CNT_ERR	SPI_READ_ERR	SPI_WRITE_ERR	SPI_CRC_ERR	MM_CRC_ERR	ROM_CRC_ERR		
0x07	ERROR_EN	0	MCLK_CNT_EN	LDO_CAP_CHK_TEST_EN	LDO_CAP_CHK[1:0]		ADC_CAL_ERR_EN	ADC_CONV_ERR_EN	ADC_SAT_ERR_EN	0x000040	R/W
		AINP_OV_ERR_EN	AINP_UV_ERR_EN	AINM_OV_ERR_EN	AINM_UV_ERR_EN	REF_DET_ERR_EN	DLDO_PSM_TRIP_TEST_EN	DLDO_PSM_ERR_EN	ALDO_PSM_TRIP_TEST_EN		
		ALDO_PSM_ERR_EN	SPI_IGNORE_ERR_EN	SPI_SCLK_CNT_ERR_EN	SPI_READ_ERR_EN	SPI_WRITE_ERR_EN	SPI_CRC_ERR_EN	MM_CRC_ERR_EN	ROM_CRC_ERR_EN		
0x08	MCLK_COUNT	MCLK_COUNT[7:0]								0x00	R
0x09 to 0x18	CHANNEL_0 to CHANNEL_15	Enable	Setup[2:0]			0		AINP[4:3]		0x8001 (1)	R/W
		AINP[2:0]			AINM[4:0]						
0x19 to 0x20	CONFIG_0 to CONFIG_7	0				Bipolar	Burnout[1:0]		REF_BUFP	0x0860	R/W
		REF_BUFM	AIN_BUFP	AIN_BUFM	REF_SEL[1:0]		PGA[2:0]				
0x21 to 0x28	FILTER_0 to FILTER_7	Filter[2:0]			REJ60	POST_FILTER[2:0]			SINGLE_CYCLE	0x060180	R/W
		0					FS[10:8]				
		FS[7:0]									
0x29 to 0x30	OFFSET_0 to OFFSET_7	Offset[23:16]								0x800000	R/W
		Offset[15:8]									
		Offset[7:0]									
0x31 to 0x38	GAIN_0 to GAIN_7	Gain[23:16]								0x5XXXXX	R/W
		Gain[15:8]									
		Gain[7:0]									

NOTE:

1. The CHANNEL_0 register is reset to 0x8001. All the other channels are reset to 0x0001.

REGISTER MAPS (continued)

Communications Register (RS[5:0] = 000000, Reset = 0x00)

Table 32. Communications Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[7]	nWEN	W	Write Enable Bit This bit must be set to 0, so that a write operation to the communication registers to actually take place. If a value of 1 is initially written, the device will not clock in any subsequent bits into the register; it will remain latched at this bit until a value of 0 is written. Once a value of 0 is written to the nWEN bit, the subsequent 7 bits are then loaded into the communication register.
D[6]	R/$\overline{W}$	W	0 = The next operation is a write to a specified register 1 = The next operation is a read from the designated register
D[5:0]	RS[5:0]	W	Register Address Bits These bits select which ADC registers are being selected during this serial interface communication. Refer to Table 31.

Status Register (RS[5:0] = 000000, Power-On/Reset = 0x00)

Table 33. Status Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[7]	nRDY	R	Ready Bit for the ADC The bit clears when data is written to the ADC data register. The nRDY bit sets automatically in three cases: 1) after the ADC data register is read. 2) a while before the register gets new conversion data (to warn against reading). 3) when the device enters power-down/standby mode. The DOUT/nRDY pin also signals conversion end, serving as an alternative to the status register for monitoring ADC conversion data.
D[6]	ERROR_FLAG	R	ADC Error Bit This bit shows if any error bit in the error register is asserted. It is high when one or more error bits are set, and clears upon reading the error register.
D[5]	0	R	The bit is set to 0.
D[4]	POR_FLAG	R	Power-On Reset Flag This bit indicates a power-on reset, which happens on power-up, when supply voltage drops below threshold, during reset execution, or when exiting power-down mode. The bit clears only after reading the status register.
D[3:0]	CH_ACTIVE[3:0]	R	These bits identify the channel that the ADC is converting. 0000 = Channel 0 0001 = Channel 1 0010 = Channel 2 0011 = Channel 3 0100 = Channel 4 0101 = Channel 5 0110 = Channel 6 0111 = Channel 7 1000 = Channel 8 1001 = Channel 9 1010 = Channel 10 1011 = Channel 11 1100 = Channel 12 1101 = Channel 13 1110 = Channel 14 1111 = Channel 15

REGISTER MAPS (continued)

ADC_CONTROL Register (RS[5:0] = 000001, Power-On/Reset = 0x0000)

Table 34. ADC Control Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[15:13]	000	R/W	These bits must be set to 0.
D[12]	DOUT_nRDY_DEL	R/W	The bit controls the SCLK inactive edge to DOUT_nRDY high time. 0 = The delay is 10ns minimum 1 = The delay is increased to 100ns minimum This function is useful when nCS is tied low (nCS_EN bit is set to 0).
D[11]	CONT_READ	R/W	Data Register Continuous Read When this bit is set to 1 (with data register selected), the serial interface enables continuous reading of the data register. Specifically, after nRDY goes low (indicating conversion completion), SCLK pulses will automatically put the data register contents on the DOUT pin. No rewrite to the communications register is needed for subsequent data reads. - Enable continuous read: Set the CONT_READ bit. - Disable continuous read: Write a read data command while DOUT/nRDY is low. With continuous read enabled, the ADC monitors DIN for the disable instruction. Also, 64 consecutive 1s on DIN trigger a reset—keep DIN low until an instruction is written.
D[10]	DATA_STATUS	R/W	This bit enables status register transmission post each data register read. When DATA_STATUS is set, status register contents are sent with every data register read. This function benefits multi-channel selection, as the status register identifies which channel the data register value corresponds to.
D[9]	nCS_EN	R/W	This bit controls the operation of the DOUT/nRDY pin during data read operations. 0 = The DOUT pin returns to being an nRDY pin within nanoseconds of the SCLK inactive edge (the delay is determined by the DOUT_nRDY_DEL bit) 1 = Continue to output the LSB of the register being read until nCS is taken high When nCS_EN is set, all read operations must be framed by nCS. nCS_EN must be set to use diagnostic functions: SPI_WRITE_ERR, SPI_READ_ERR, and SPI_SCLK_CNT_ERR.
D[8]	REF_EN	R/W	Internal Reference Voltage Enable 0 = The internal reference is disabled 1 = The internal reference is enabled and available at the REFOUT pin
D[7:6]	POWER_MODE[1:0]	R/W	Power Mode Select 00 = Low power 01 = Mid power 10 = Full power 11 = Full power Current consumption and output data rate ranges depend on power mode.
D[5:2]	Mode[3:0]	R/W	ADC Operation Mode Control Bit See Table 35.
D[1:0]	CLK_SEL[1:0]	R/W	ADC Clock Source Select 00 = Internal 614.4kHz clock. The internal clock is not available at the CLK pin 01 = Internal 614.4kHz clock. This clock is available at the CLK pin 10 = External 614.4kHz clock 11 = External clock. The external clock is divided by 4 within the SGM52421R8/SGM52421R8A The SGM52421R8/SGM52421R8A support either its on-chip 614.4kHz clock or an external clock. An external clock enables synchronization of multiple such devices and improves 50Hz/60Hz rejection when driving the ADC accurately.

REGISTER MAPS (continued)

Table 35. Operating Modes

Mode[3:0] Bits	Description
0000	Continuous Conversion Mode (default). In continuous conversion mode, the ADC runs conversions nonstop and stores results in the data register; nRDY goes low upon conversion completion. Users can read results in two ways: - Enter continuous read mode, where SCLK pulses auto-place conversions on DOUT. - Write to the communications register to trigger ADC output. After power-on reset, or ADC reconfiguration, the filter needs full settling time for the first valid conversion. Subsequent conversions follow the selected output data rate (dependent on filter choice).
0001	Single Conversion Mode. In single conversion mode, the ADC powers up, runs one conversion on the selected channel (needing full filter settling time), then stores the result in the data register. nRDY goes low, and the ADC returns to standby mode. The result stays in the data register, and nRDY remains low until the data is read or a new conversion starts.
0010	Standby Mode. In standby mode, all SGM52421R8/SGM52421R8A sections power down except LDOs. The internal reference, on-chip oscillator, low-side power switch, and bias voltage generator can be enabled/disabled here; on-chip registers retain contents. Enabled diagnostics stay active (and can be toggled) in standby mode. However, diagnostics needing the master clock (reference detect, UV/OV detection, LDO trip tests, memory map CRC, MCLK counter) must be enabled in continuous conversion or idle mode—they won't work if enabled in standby.
0011	Power-Down Mode. In power-down mode, all SGM52421R8/SGM52421R8A circuits power down, including current sources, power switch, burnout currents, bias generator, clock circuitry, and LDOs. On-chip registers lose their contents, requiring full reprogramming when exiting this mode.
0100	Idle Mode. In idle mode, the ADC filter and modulator are held in a reset state even though the modulator clocks continue to be provided. In idle mode, the ADC filter and modulator stay reset, though modulator clocks persist.
0101	Internal Zero-Scale (Offset) Calibration. An internal short auto-connects to the input. nRDY goes high on calibration start and low when done. Post-calibration, the ADC enters idle mode. The measured offset coefficient is stored in the selected channel's offset register. Select only one channel for zero-scale calibration, which takes one settling period.
0110	Internal Full-Scale (Gain) Calibration. A full-scale input voltage auto-connects to the selected analog input for calibration. nRDY goes high on calibration start and low when complete. Post-calibration, the ADC enters idle mode, and the measured full-scale coefficient is stored in the selected channel's gain register. Full-scale calibration is required after a channel's gain change to minimize full-scale error; select only one channel. The SGM52421R8/SGM52421R8A are factory-calibrated at gain 1, with no support for further calibrations at this gain. Internal full-scale calibration (gain > 1) takes four settling periods and is unavailable in full power mode—switch to mid/low power mode for it (calibration remains valid in full power mode due to shared reference/gain). Internal full-scale calibration must precede zero-scale calibration. Thus, write 0x800000 to the offset register to reset it before any full-scale calibration.
0111	System Zero-Scale (Offset) Calibration. Connect the system zero-scale input to the selected channel's input pins. nRDY goes high on calibration start and low when complete. Post-calibration, the ADC enters idle mode, and the measured offset coefficient is stored in the channel's offset register. System zero-scale calibration is required after a channel's gain change. Select only one channel. It takes one settling period.
1000	System Full-Scale (Gain) Calibration. Connect the system full-scale input to the selected channel's input pins. nRDY goes high on calibration start and low when complete. Post-calibration, the ADC enters idle mode, and the measured full-scale coefficient is stored in the channel's gain register. System full-scale calibration is required after a channel's gain change. Select only one channel. It takes one settling period.
1001 to1111	Reserved.

REGISTER MAPS (continued)

Data Register (RS[5:0] = 000010, Power-On/Reset = 0x000000)

The data register is used to store the conversion results of the ADC. It is a read-only register. When the read operation from this register is complete, the nRDY bit/pin is set.

IO_CONTROL_1 Register (RS[5:0] = 000011, Power-On/Reset = 0x000000)

Table 36. IO_CONTROL_1 Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[23]	GPIO_DAT4	R/W	Digital Output P4 When GPIO_CTRL4 is set, GPIO_DAT4 determines P4's output: high for high P4, low for low P4. Reading IO_CONTROL_1 then shows P4's status via GPIO_DAT4.
D[22]	GPIO_DAT3	R/W	Digital Output P3 When GPIO_CTRL3 is set, GPIO_DAT3 determines P3's output: high for high P3, low for low P3. Reading IO_CONTROL_1 then shows P3's status via GPIO_DAT3.
D[21]	GPIO_DAT2	R/W	Digital Output P2 When GPIO_CTRL2 is set, GPIO_DAT2 determines P2's output: high for high P2, low for low P2. Reading IO_CONTROL_1 then shows P2's status via GPIO_DAT2.
D[20]	GPIO_DAT1	R/W	Digital Output P1 When GPIO_CTRL1 is set, GPIO_DAT1 determines P1's output: high for high P1, low for low P1. Reading IO_CONTROL_1 then shows P1's status via GPIO_DAT1.
D[19]	GPIO_CTRL4	R/W	Digital Output P4 Enable 0 = Pin acts as analog input AIN5. 1 = Digital output P4 is active.
D[18]	GPIO_CTRL3	R/W	Digital Output P3 Enable 0 = Pin acts as analog input AIN4. 1 = Digital output P3 is active.
D[17]	GPIO_CTRL2	R/W	Digital Output P2 Enable 0 = Pin acts as analog input AIN3. 1 = Digital output P2 is active.
D[16]	GPIO_CTRL1	R/W	Digital Output P1 Enable 0 = Pin acts as analog input AIN2. 1 = Digital output P1 is active.
D[15]	PDSW	R/W	Bridge Power-Down Switch Control Bit Set this bit to close bridge power-down switch PDSW to AGND (sinks up to 30mA). Clear to open it. PDSW stays active when ADC is in standby.
D[14]	0	R/W	This bit must be set to 0.

REGISTER MAPS (continued)

Table 36. IO_CONTROL_1 Register Details (continued)

BITS	BIT NAME	TYPE	DESCRIPTION
D[13:11]	IOUT1[2:0]	R/W	Set the value of the excitation current for IOUT1. 000 = Off 001 = 50μA 010 = 100μA 011 = 250μA 100 = 500μA 101 = 750μA 110 = 1000μA 111 = 0.1μA
D[10:8]	IOUT0[2:0]	R/W	Set the value of the excitation current for IOUT0. 000 = Off 001 = 50μA 010 = 100μA 011 = 250μA 100 = 500μA 101 = 750μA 110 = 1000μA 111 = 0.1μA
D[7:4]	IOUT1_CH[3:0]	R/W	Channel select bits for the excitation current for IOUT1. 0000 = IOUT1 is available on the AIN0 pin 0001 = IOUT1 is available on the AIN1 pin 0010 = IOUT1 is available on the AIN2 pin 0011 = IOUT1 is available on the AIN3 pin 0100 = IOUT1 is available on the AIN4 pin 0101 = IOUT1 is available on the AIN5 pin 0110 = IOUT1 is available on the AIN6 pin 0111 = IOUT1 is available on the AIN7 pin 1000 = IOUT1 is available on the AIN8 pin 1001 = IOUT1 is available on the AIN9 pin 1010 = IOUT1 is available on the AIN10 pin 1011 = IOUT1 is available on the AIN11 pin 1100 = IOUT1 is available on the AIN12 pin 1101 = IOUT1 is available on the AIN13 pin 1110 = IOUT1 is available on the AIN14 pin 0111 = IOUT1 is available on the AIN15 pin
D[3:0]	IOUT0_CH[3:0]	R/W	Channel select bits for the excitation current for IOUT0. 0000 = IOUT0 is available on the AIN0 pin 0001 = IOUT0 is available on the AIN1 pin 0010 = IOUT0 is available on the AIN2 pin 0011 = IOUT0 is available on the AIN3 pin 0100 = IOUT0 is available on the AIN4 pin 0101 = IOUT0 is available on the AIN5 pin 0110 = IOUT0 is available on the AIN6 pin 0111 = IOUT0 is available on the AIN7 pin 1000 = IOUT0 is available on the AIN8 pin 1001 = IOUT0 is available on the AIN9 pin 1010 = IOUT0 is available on the AIN10 pin 1011 = IOUT0 is available on the AIN11 pin 1100 = IOUT0 is available on the AIN12 pin 1101 = IOUT0 is available on the AIN13 pin 1110 = IOUT0 is available on the AIN14 pin 1111 = IOUT0 is available on the AIN15 pin

REGISTER MAPS (continued)

IO_CONTROL_2 Register (RS[5:0] = 000100, Power-On/Reset = 0x0000)

Table 37. IO_CONTROL_2 Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[15]	VBIAS15	R/W	Enable the bias voltage on the AIN15 channel. The internal bias voltage is available on AIN15 when the bit is set.
D[14]	VBIAS14	R/W	Enable the bias voltage on the AIN14 channel. The internal bias voltage is available on AIN14 when the bit is set.
D[13]	VBIAS13	R/W	Enable the bias voltage on the AIN13 channel. The internal bias voltage is available on AIN13 when the bit is set.
D[12]	VBIAS12	R/W	Enable the bias voltage on the AIN12 channel. The internal bias voltage is available on AIN12 when the bit is set.
D[11]	VBIAS11	R/W	Enable the bias voltage on the AIN11 channel. The internal bias voltage is available on AIN11 when the bit is set.
D[10]	VBIAS10	R/W	Enable the bias voltage on the AIN10 channel. The internal bias voltage is available on AIN10 when the bit is set.
D[9]	VBIAS9	R/W	Enable the bias voltage on the AIN9 channel. The internal bias voltage is available on AIN9 when the bit is set.
D[8]	VBIAS8	R/W	Enable the bias voltage on the AIN8 channel. The internal bias voltage is available on AIN8 when the bit is set.
D[7]	VBIAS7	R/W	Enable the bias voltage on the AIN7 channel. The internal bias voltage is available on AIN7 when the bit is set.
D[6]	VBIAS6	R/W	Enable the bias voltage on the AIN6 channel. The internal bias voltage is available on AIN6 when the bit is set.
D[5]	VBIAS5	R/W	Enable the bias voltage on the AIN5 channel. The internal bias voltage is available on AIN5 when the bit is set.
D[4]	VBIAS4	R/W	Enable the bias voltage on the AIN4 channel. The internal bias voltage is available on AIN4 when the bit is set.
D[3]	VBIAS3	R/W	Enable the bias voltage on the AIN3 channel. The internal bias voltage is available on AIN3 when the bit is set.
D[2]	VBIAS2	R/W	Enable the bias voltage on the AIN2 channel. The internal bias voltage is available on AIN2 when the bit is set.
D[1]	VBIAS1	R/W	Enable the bias voltage on the AIN1 channel. The internal bias voltage is available on AIN1 when the bit is set.
D[0]	VBIAS0	R/W	Enable the bias voltage on the AIN0 channel. The internal bias voltage is available on AIN0 when the bit is set.

ID Register (RS[5:0] = 000101, Power-On/Reset = 0x18)

The ID register is used to store the identification number of the device. It is a read-only register.

REGISTER MAPS (continued)

Error Register (RS[5:0] = 000110, Power-On/Reset = 0x000000)

Table 38. Error Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[23:20]	0000	R	These bits must be set to 0.
D[19]	LDO_CAP_ERR	R	Analog/Digital LDO Decoupling Capacitor Check This flag sets if analog/digital LDO decoupling capacitors aren't connected to SGM52421R8/ SGM52421R8A. Missing capacitors may reset the ADC but are system-detectable.
D[18]	ADC_CAL_ERR	R	Calibration Check This flag sets if calibration starts but doesn't complete, indicating an error. The related calibration register remains updated.
D[17]	ADC_CONV_ERR	R	This bit indicates conversion validity. It sets if a conversion error occurs.
D[16]	ADC_SAT_ERR	R	ADC Saturation Flag This flag sets if the modulator saturates during conversion.
D[15]	AINP_OV_ERR	R	Over-Voltage Detection on AINP.
D[14]	AINP_UV_ERR	R	Under-Voltage Detection on AINP.
D[13]	AINM_OV_ERR	R	Over-Voltage Detection on AINM.
D[12]	AINM_UV_ERR	R	Under-Voltage Detection on AINM.
D[11]	REF_DET_ERR	R	Reference Detection This flag indicates if the ADC's external reference is open-circuited or below 0.7V.
D[10]	0	R	This bit must be set to 0.
D[9]	DLDO_PSM_ERR	R	Digital LDO error. This flag sets if a digital LDO error is detected.
D[8]	0	R	This bit must be set to 0.
D[7]	ALDO_PSM_ERR	R	Analog LDO Error This flag sets if an error is detected with the analog LDO voltage.
D[6]	SPI_IGNORE_ERR	R	During power-on reset and calibrations, on-chip registers are unwritable—user write instructions are ignored by the ADC. This bit sets to indicate the ADC is busy and the write instruction was ignored. The SPI_IGNORE_ERR bit clears when read.
D[5]	SPI_SCLK_CNT_ERR	R	All serial communications use multiples of eight bits. This bit sets when the number of SCLK cycles is not a multiple of eight.
D[4]	SPI_READ_ERR	R	This bit sets when an error occurs during an SPI read operation.
D[3]	SPI_WRITE_ERR	R	This bit sets when an error occurs during an SPI write operation.
D[2]	SPI_CRC_ERR	R	This bit sets if an error occurs in the CRC check of the serial communications.
D[1]	MM_CRC_ERR	R	Memory Map Error A CRC calculation runs on the memory map whenever registers are written to. Periodic CRC checks then occur on on-chip registers. If register contents change, the MM_CRC_ERR bit sets.
D[0]	ROM_CRC_ERR	R	ROM Error A CRC calculation is performed on the ROM contents (which store default register values) during power-up. If the ROM contents have changed, the ROM_CRC_ERR bit is set.

REGISTER MAPS (continued)

ERROR_EN Register (RS[5:0] = 000111, Power-On/Reset = 0x000040)

Table 39. ERROR_EN Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[23]	0	R/W	This bit must be set to 0.
D[22]	MCLK_CNT_EN	R/W	Master Clock Counter When set, this bit enables the master clock counter, whose result is reported in the MCLK_COUNT register. The counter monitors the ADC's master clock—external if used, or the on-chip oscillator if selected as the source.
D[21]	LDO_CAP_CHK_TEST_EN	R/W	Test of Analog/Digital LDO Decoupling Capacitor Check When set, this bit internally disconnects the decoupling capacitor from the LDO, forcing a fault. This lets users test the analog/digital LDO decoupling capacitor check circuitry.
D[20:19]	LDO_CAP_CHK[1:0]	R/W	Analog/Digital LDO Decoupling Capacitor Check These bits enable the capacitor check. When enabled, the ADC verifies the external decoupling capacitor on the selected supply. Post-check, the LDO_CAP_CHK bits reset to 0. A missing capacitor may reset the ADC but is easily detectable system-level. 00 = Check is not enabled 01 = Check the analog LDO capacitor 10 = Check the digital LDO capacitor 11 = Check is not enabled
D[18]	ADC_CAL_ERR_EN	R/W	When set, this bit enables the calibration fail check.
D[17]	ADC_CONV_ERR_EN	R/W	When set, this bit monitors conversions and sets the ADC_CONV_ERR bit on failure.
D[16]	ADC_SAT_ERR_EN	R/W	When set, this bit enables the ADC modulator saturation check.
D[15]	AINP_OV_ERR_EN	R/W	When set, this bit enables the over-voltage monitor on all active AINP channels.
D[14]	AINP_UV_ERR_EN	R/W	When set, this bit enables the under-voltage monitor on all active AINP channels.
D[13]	AINM_OV_ERR_EN	R/W	When set, this bit enables the over-voltage monitor on all active AINM channels.
D[12]	AINM_UV_ERR_EN	R/W	When set, this bit enables the under-voltage monitor on all active AINM channels.
D[11]	REF_DET_ERR_EN	R/W	When set, this bit continuously monitors the ADC's external reference, flagging errors for open circuits or values < 0.7V.
D[10]	DLDO_PSM_TRIP_TEST_EN	R/W	Checks the digital LDO monitoring test mechanism. When set, this bit ties the test circuit input to DGND (instead of LDO output) and sets the DLDO_PSM_ERR bit in the error register.
D[9]	DLDO_PSM_ERR_ERR_EN	R/W	When set, this bit continuously monitors the digital LDO voltage, setting the DLDO_PSM_ERR bit in the error register if the output is out of specification.
D[8]	ALDO_PSM_TRIP_TEST_EN	R/W	Checks the analog LDO monitoring test mechanism. When set, this bit ties the test circuit input to AV_{SS} (instead of LDO output) and sets the ALDO_PSM_ERR bit in the error register.
D[7]	ALDO_PSM_ERR_EN	R/W	When set, this bit continuously monitors the analog LDO voltage, setting the ALDO_PSM_ERR bit in the error register if the output is out of specification.
D[6]	SPI_IGNORE_ERR_EN	R/W	During power-on reset and calibrations, on-chip registers are unwritable (ADC ignores user writes). Set this bit to have the SPI_IGNORE_ERR bit in the error register notify users of ignored writes.
D[5]	SPI_SCLK_CNT_ERR_EN	R/W	When set, this bit enables the SCLK counter. All ADC read/write operations use 8-bit multiples. The counter tracks SCLK pulses per serial communication, framed by CS. If pulses aren't 8-bit multiples, the SPI_SCLK_CNT_ERR bit sets (e.g., for SCLK glitches causing excess pulses). nCS_EN in ADC_CONTROL must be 1 when using this function.
D[4]	SPI_READ_ERR_EN	R/W	When set, this bit triggers the SPI_READ_ERR bit in the error register on read errors (e.g., reading invalid addresses). nCS_EN in ADC_CONTROL must be 1 when using this function.
D[3]	SPI_WRITE_ERR_EN	R/W	When set, this bit triggers the SPI_WRITE_ERR bit in the error register on write errors (e.g., writing to invalid addresses or read-only registers). nCS_EN in ADC_CONTROL must be 1 when using this function.
D[2]	SPI_CRC_ERR_EN	R/W	When set, this bit enables CRC checking for all read and write operations. The SPI_CRC_ERR bit in the error register is set upon CRC check failure. Additionally, an 8-bit CRC word is appended to all data read from the SGM52421R8/SGM52421R8A.
D[1]	MM_CRC_ERR_EN	R/W	When set, this bit triggers a CRC calculation on the memory map each time registers are written to, followed by periodic CRC checks on on-chip registers. The MM_CRC_ERR bit is set if register contents change.
D[0]	ROM_CRC_ERR_EN	R/W	When set, this bit initiates a CRC calculation on ROM contents during power-on. The ROM_CRC_ERR bit is set if ROM contents have changed.

REGISTER MAPS (continued)

MCLK_COUNT Register (RS[5:0] = 001000, Power-On/Reset = 0x00)

Table 40. MCLK_COUNT Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[7:0]	MCLK_COUNT[7:0]	R	This register enables users to determine the frequency of the internal/external oscillator. Internally, a clock counter increments every 131 pulses of the sampling clock (614.4kHz in full power mode, 153.6kHz in mid power mode, and 768kHz in low power mode). The 8-bit counter overflows when reaching its maximum value, and its output is readable via this register. Note that register incrementation is asynchronous to read operations. If a read coincides with an increment, an invalid value may be returned. To prevent this: 1. Read the register four times consecutively 2. Repeat the four-read sequence at a later point 3. Compare the two sets of readings to identify valid values at both timing instants

Channel Registers (RS[5:0] = 001001 to 011000, Power-On/Reset = 0x8001 for CHANNEL_0, All Other Channel Registers are Set to 0x0001)

Table 41. Channel Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[15]	Enable	R/W	Channel Enable Bit Setting this bit enables the channel for conversion. By default, only Channel 0 is enabled. Conversions start at the lowest enabled channel, cycle upward, then wrap to the lowest. When the ADC outputs a channel's result, the status register's 4 LSBs show its number (0-15) for identification. With the ADC_CONTROL register's DATA_STATUS bit set, the status register's contents are appended to each read result—use this to match values to channels when multiple are enabled.
D[14:12]	Setup[2:0]	R/W	Setup Select These bits select one of eight setups to configure the ADC for the channel. A setup includes four registers: analog config, output data rate/filter, offset, and gain. All active channels can share a setup (same 3-bit value) or up to eight channels can have unique configurations.
D[11:10]	00	R/W	These bits must be set to 0.
D[9:5]	AINP[4:0]	R/W	Positive Analog Input AINP Input Select These bits select the analog input connected to the channel's positive input. 00000 = AIN0 (default) 00001 = AIN1 00010 = AIN2 00011 = AIN3 00100 = AIN4 00101 = AIN5 00110 = AIN6 00111 = AIN7 01000 = AIN8 01001 = AIN9 01010 = AIN10 01011 = AIN11 01100 = AIN12 01101 = AIN13 01110 = AIN14 01111 = AIN15 10000 = Temperature sensor 10001 = AV_{SS} 10010 = Internal reference 10011 = DGND 10100 = (AV_{DD} - AV_{SS})/6+. Use in conjunction with (AV_{DD} - AV_{SS})/6- to monitor supply AV_{DD} - AV_{SS} 10101 = (AV_{DD} - AV_{SS})/6-. Use in conjunction with (AV_{DD} - AV_{SS})/6+ to monitor supply AV_{DD} - AV_{SS} 10110 = (IOV_{DD} - DGND)/6+. Use in conjunction with (IOV_{DD} - DGND)/6- to monitor IOV_{DD} - DGND 10111 = (IOV_{DD} - DGND)/6-. Use in conjunction with (IOV_{DD} - DGND)/6+ to monitor IOV_{DD} - DGND 11000 = (ALDO - AV_{SS})/6+. Use in conjunction with (ALDO - AV_{SS})/6- to monitor the analog LDO 11001 = (ALDO - AV_{SS})/6-. Use in conjunction with (ALDO - AV_{SS})/6+ to monitor the analog LDO 11010 = (DLDO - DGND)/6+. Use in conjunction with (DLDO - DGND)/6- to monitor the digital LDO 11011 = (DLDO - DGND)/6-. Use in conjunction with (DLDO - DGND)/6+ to monitor the digital LDO 11100 = V_20MV_P. Use in conjunction with V_20MV_M to apply a 20mVp-p signal to the ADC 11101 = V_20MV_M. Use in conjunction with V_20MV_P to apply a 20mVp-p signal to the ADC 11110 = Reserved 11111 = Reserved

REGISTER MAPS (continued)

Table 41. Channel Register Details (continued)

BITS	BIT NAME	TYPE	DESCRIPTION
D[4:0]	AINM[4:0]	R/W	Negative Analog Input AINM Input Select These bits select the analog input connected to the channel's negative input. 00000 = AIN0 00001 = AIN1 (default) 00010 = AIN2 00011 = AIN3 00100 = AIN4 00101 = AIN5 00110 = AIN6 00111 = AIN7 01000 = AIN8 01001 = AIN9 01010 = AIN10 01011 = AIN11 01100 = AIN12 01101 = AIN13 01110 = AIN14 01111 = AIN15 10000 = Temperature sensor 10001 = AV_{SS} 10010 = Internal reference 10011 = DGND 10100 = (AV_{DD} - AV_{SS})/6+. Use in conjunction with (AV_{DD} - AV_{SS})/6- to monitor supply AV_{DD} - AV_{SS} 10101 = (AV_{DD} - AV_{SS})/6-. Use in conjunction with (AV_{DD} - AV_{SS})/6+ to monitor supply AV_{DD} - AV_{SS} 10110 = (IOV_{DD} - DGND)/6+. Use in conjunction with (IOV_{DD} - DGND)/6- to monitor IOV_{DD} - DGND 10111 = (IOV_{DD} - DGND)/6-. Use in conjunction with (IOV_{DD} - DGND)/6+ to monitor IOV_{DD} - DGND 11000 = (ALDO - AV_{SS})/6+. Use in conjunction with (ALDO - AV_{SS})/6- to monitor the analog LDO 11001 = (ALDO - AV_{SS})/6-. Use in conjunction with (ALDO - AV_{SS})/6+ to monitor the analog LDO 11010 = (DLDO - DGND)/6+. Use in conjunction with (DLDO - DGND)/6- to monitor the digital LDO 11011 = (DLDO - DGND)/6-. Use in conjunction with (DLDO - DGND)/6+ to monitor the digital LDO 11100 = V_20MV_P. Use in conjunction with V_20MV_M to apply a 20mVp-p signal to the ADC 11101 = V_20MV_M. Use in conjunction with V_20MV_P to apply a 20mVp-p signal to the ADC 11110 = Reserved 11111 = Reserved

REGISTER MAPS (continued)

Configuration Registers (RS[5:0] = 011001 to 100000, Power-On/Reset = 0x0860)

Table 42. Configuration Register Details

BITS	BIT NAME	TYPE	DESCRIPTION
D[15:12]	0000	R/W	These bits must be set to 0.
D[11]	Bipolar	R/W	Polarity Select Bit Setting this bit selects bipolar operation; clearing it selects unipolar operation.
D[10:9]	Burnout[1:0]	R/W	These bits select the magnitude of the sensor burnout detect current source. 00 = Burnout current source off (default) 01 = Burnout current source on, 0.5μA 10 = Burnout current source on, 2μA 11 = Burnout current source on, 4μA
D[8]	REF_BUFP	R/W	Buffer Enable on REFINx(+) Setting this bit buffers the positive reference input (internal/external). Clearing it leaves it unbuffered.
D[7]	REF_BUFM	R/W	Buffer Enable on REFINx(-) Setting this bit buffers the negative reference input (internal/external). Clearing it leaves it unbuffered.
D[6]	AIN_BUFP	R/W	Buffer Enable on AINP Setting this bit buffers the selected positive analog input pin. Clearing it leaves it unbuffered.
D[5]	AIN_BUFM	R/W	Buffer Enable on AINM Setting this bit buffers the selected negative analog input pin. Clearing it leaves it unbuffered.
D[4:3]	REF_SEL[1:0]	R/W	Reference Source Select Bits These bits determine the reference source utilized for conversions on all channels that rely on this configuration register. 00 = REFIN1(+)/REFIN1(-) 01 = REFIN2(+)/REFIN2(-) 10 = internal reference 11 = AV_{DD}
D[2:0]	PGA[2:0]	R/W	Gain Select Bits These bits select the gain for conversions on all channels using this configuration register.

PGA[2:0]	Gain	Input Range When V_{REF} = 2.5V (Bipolar Mode)
000	1	±2.5V
001	2	±1.25V
010	4	± 625mV
011	8	±312.5mV
100	16	±156.25mV
101	32	±78.125mV
110	64	±39.06mV
111	128	±19.53mV

REGISTER MAPS (continued)

Filter Registers (RS[5:0] = 100001 to 101000, Power-On/Reset = 0x060180)

Table 43. Filter Register Details

<table>
<tr><th>BITS</th><th>BIT NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>D[23:21]</td><td>Filter[2:0]</td><td>R/W</td><td>Filter Type Select Bits
These bits select the filter type.
000 = Sinc^4 filter (default)
001 = Reserved
010 = Sinc^3 filter
011 = Reserved
100 = Fast settling with sinc^4 filter, followed by an averaging block (settling time = conversion time). Averages by 16 in full/mid power modes, 8 in low power mode
101 = Fast settling with sinc^3 filter, followed by an averaging block (settling time = conversion time). Averages by 16 in full/mid power modes, 8 in low power mode
110 = Reserved
111 = Post filter enabled

The SGM52421R8/SGM52421R8A have selectable post filters (via POST_FILTER[2:0] bits). They feature single-cycle settling (far better than basic sinc^3/sinc^4 filters) and excellent 50Hz/60Hz rejection.</td></tr>
<tr><td>D[20]</td><td>REJ60</td><td>R/W</td><td>Setting this bit adds a 60Hz first-order notch when the sinc filter's first notch is at 50Hz, enabling simultaneous 50Hz/60Hz rejection.</td></tr>
<tr><td rowspan="10">D[19:17]</td><td rowspan="10">POST_FILTER[2:0]</td><td rowspan="10">R/W</td><td>Post Filter Type Select Bits
When filter bits = 1, the sinc^3 filter is followed by a post filter with good 50Hz/60Hz rejection and near-zero latency at output data rates.</td></tr>
<tr><td><table>
<tr><th>POST_FILTER[2:0]</th><th>Output Data Rate (SPS)</th><th>Rejection at 50Hz and 60Hz ± 1Hz (dB)</th></tr>
<tr><td>000</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>010</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>010</td><td>27.27</td><td>47</td></tr>
<tr><td>011</td><td>25</td><td>62</td></tr>
<tr><td>100</td><td>Reserved</td><td>Not applicable</td></tr>
<tr><td>101</td><td>20</td><td>86</td></tr>
<tr><td>110</td><td>16.7</td><td>92</td></tr>
<tr><td>111</td><td>Reserved</td><td>Not applicable</td></tr>
</table></td></tr>
<tr><td>D[16]</td><td>SINGLE_CYCLE</td><td>R/W</td><td>Single Cycle Conversion Enable Bit
Setting this bit makes the SGM52421R8/SGM52421R8A settle in one conversion cycle, acting as a zero-latency ADC. It has no effect with multiple enabled channels, single conversion mode, or fast filters.</td></tr>
<tr><td>D[15:11]</td><td>00000</td><td>R/W</td><td>These bits must be set to 0.</td></tr>
<tr><td>D[10:0]</td><td>FS[10:0]</td><td>R/W</td><td>Filter Output Data Rate Select Bits
These bits set the output data rate for sinc^3, sinc^4, and fast settling filters. They also affect the sinc filter's first notch position, cutoff frequency, and (with gain selection) output noise—thus determining effective resolution (see noise tables). FS ranges 1 to 2047.</td></tr>
</table>

REGISTER MAPS (continued)

Offset Registers (RS[5:0] = 101001 to 110000, Power-On/Reset = 0x800000)

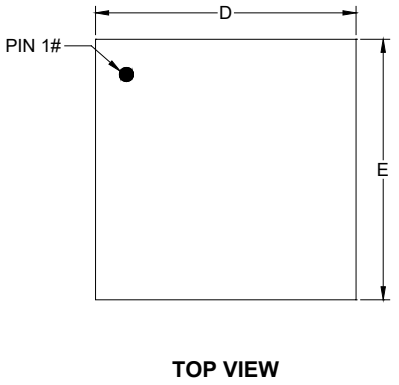
The SGM52421R8/SGM52421R8A feature eight offset registers, labeled OFFSET_0 through OFFSET_7. Each offset register corresponds to a specific setting, where OFFSET_x is associated with setting x. These offset registers are 24-bit read/write registers that store the offset calibration factor for the ADC, with a default power-on reset value of 0x800000. The offset registers function in conjunction with their corresponding gain registers to form register pairs. If the user initiates either an internal or system zero-scale calibration, the power-on reset value will be automatically overwritten. When writing to the offset register, it is necessary to place the ADC in standby or idle mode.

Gain Registers (RS[5:0] = 110001 to 111000, Power-On/Reset = 0x5XXXXX)

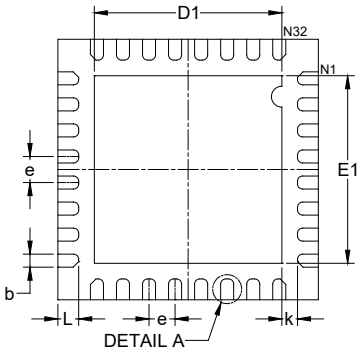
The SGM52421R8/SGM52421R8A feature eight gain registers, labeled GAIN_0 through GAIN_7. Each gain register corresponds to a specific setting, where GAIN_x is associated with setting x. These gain registers are 24-bit and store the full-scale calibration coefficient for the analog-to-digital converter (ADC). The SGM52421R8/SGM52421R8A undergo factory calibration to a gain of 1. Upon power-on or after a reset, the gain registers contain the factory-calibrated value. These registers are both readable and writable. However, when writing to these registers, the ADC must be placed in either standby mode or idle mode. Additionally, the default value will be automatically overwritten if an internal or system full-scale calibration is initiated by the user or if the full-scale registers are modified.

PACKAGE OUTLINE DIMENSIONS

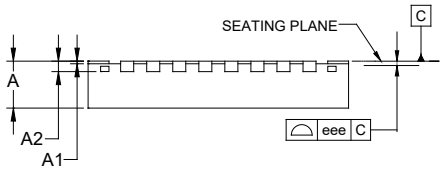
TQFN-5×5-32IL



TOP VIEW

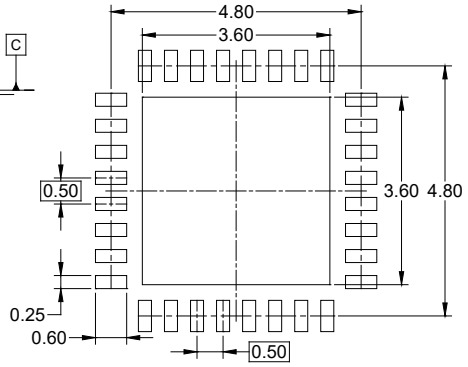


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



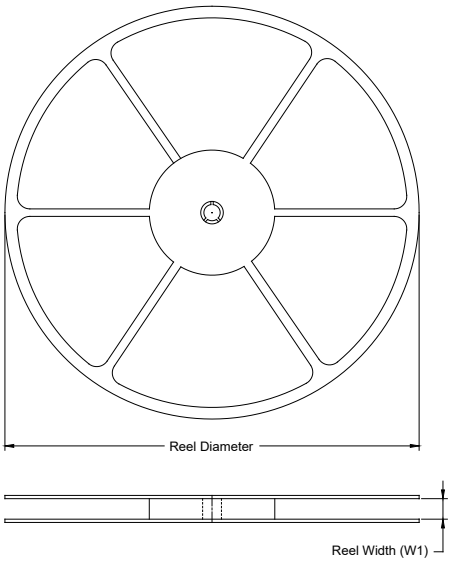
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.850	-	0.950
A1	0.000	-	0.050
A2	0.200 REF		
b	0.200	-	0.300
D	4.900	-	5.100
E	4.900	-	5.100
D1	3.500	-	3.700
E1	3.500	-	3.700
e	0.500 BSC		
L	0.300	-	0.500
k	0.200 MIN		
eee	0.080		

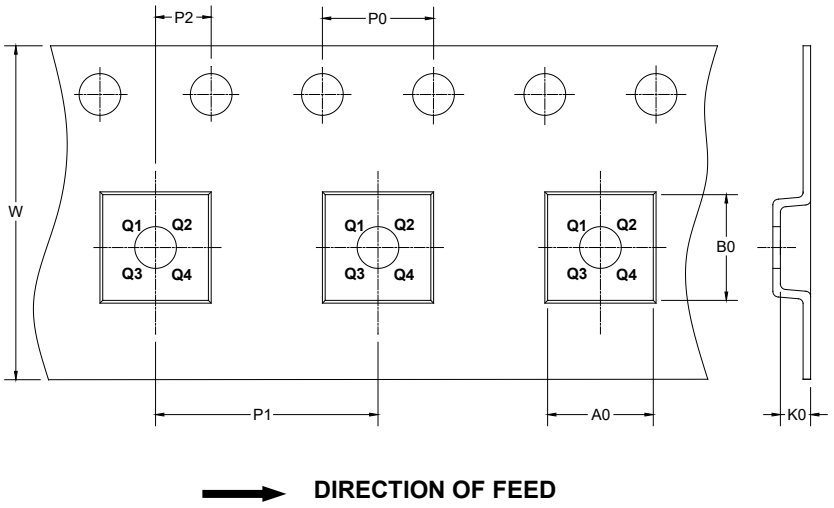
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



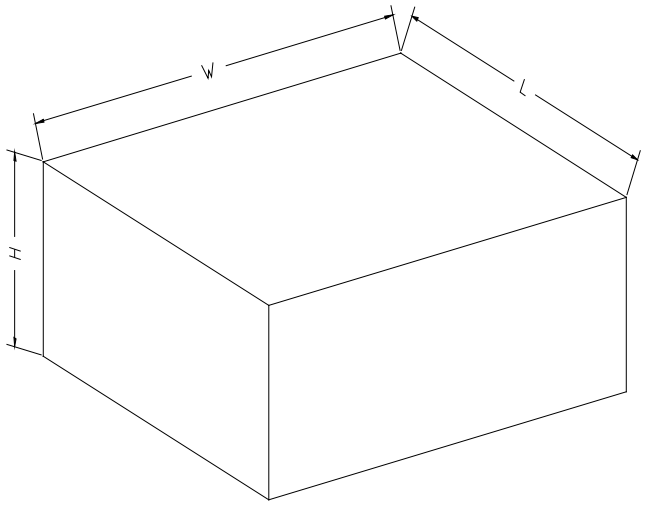
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×5-32IL	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002