SGMM2042
3A Continuous (4A Peak), 2.2MHz 2.4V to 5.5V, 3D Buck PowerSoC

GENERAL DESCRIPTION

SGMM2042 is a high frequency synchronous Buck PowerSoC with an input voltage range from 2.4V to 5.5V and a wide output current range, optimized for compact solutions. For SGMM2042A, to keep the high efficiency in the whole load range, the device operates in pulse width modulation (PWM) mode at normal load and automatically enters the power-save mode (PSM) at light loads. The minimum static current is only 5.7μA to maintain its high efficiency. For SGMM2042B, the device operates in force PWM mode at light and heavy loads.

With its adaptive hysteresis and pseudo-constant on time control (AHP-COT) architecture, the load transient performance is excellent and achieves V_{OUT} regulation accuracy.

The compact and low profile device is in a package of 2mm × 2.5mm × 1.27mm, allowing the system to achieve high density.

The SGMM2042 is available in a Green EMSIP-2×2.5-10L package.

FEATURES

- **AHP-COT Architecture for Fast Transient Regulation**
- **3D Integrated SoC Device with Power IC, Power Inductor**
- **2.4V to 5.5V Input Voltage Range**
- **0.6V to 4V Wide Output Voltage Range**
- **3A Continuous Output Current**
- **4A Peak Output Current**
- **Low Quiescent Current: 5.7μA (SGMM2042A)**
- **Switching Frequency: 2.2MHz**
- **100% Duty Cycle for the Lowest Dropout**
- **Power-Save Mode at Light Loads: SGMM2042A**
- **Force PWM Mode: SGMM2042B**
- **Output Discharge Function**
- **Power Good Output**
- **Thermal Shutdown**
- **Hiccup Short-Circuit Protection**
- **Available in a Green EMSIP-2×2.5-10L Package**

APPLICATIONS

Optical Modules
Battery-Powered Applications
Point-of-Load
Processor Power Supplies
Hard Disk Drives (HDD)/Solid State Drives (SSD)

SIMPLIFIED SCHEMATIC

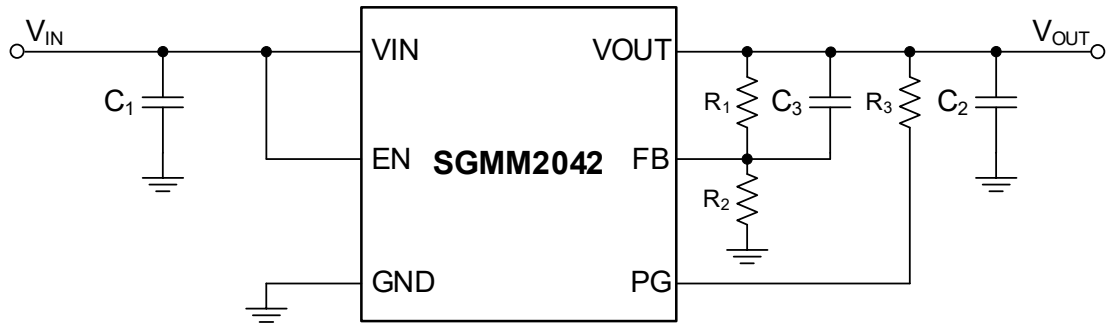
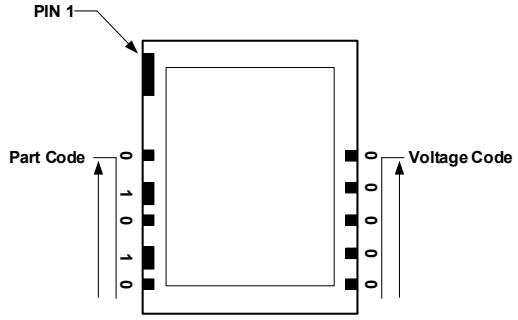


Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKING OPTION
SGMM2042A	EMSIP-2×2.5-10L	-40℃ to +125℃	SGMM2042AXESAA10G/TR	Tape and Reel, 3000
SGMM2042B	EMSIP-2×2.5-10L	-40℃ to +125℃	SGMM2042BXESAA10G/TR	Tape and Reel, 3000

PACKAGE MARKING INFORMATION



Silkscreen Marking Descriptions				
Part Name	Part Code		Voltage Code	
	Code	Binary System	Code	Binary System
SGMM2042	A	01010	0	00000

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltages Referred to GND

VIN, FB, EN, PG ..... -0.3V to 6V

VOUT ..... -0.3V to V_{IN} + 0.3V

Package Thermal Resistance

EMSIP-2×2.5-10L, θ_{JA} ..... 105.8℃/W

EMSIP-2×2.5-10L, θ_{JB} ..... 18.9℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (1) (2)

HBM ..... ±4000V

CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ..... 2.4V to 5.5V

Output Voltage Range, V_{OUT} ..... 0.6V to 4.0V

Output Current Range, I_{OUT} ..... 0A to 3A (4A Peak)

Sink Current at PG Pin, I_{SINK_PG} 1mA

Pull-Up Resistor Voltage, V_{PG} 5.5V

Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

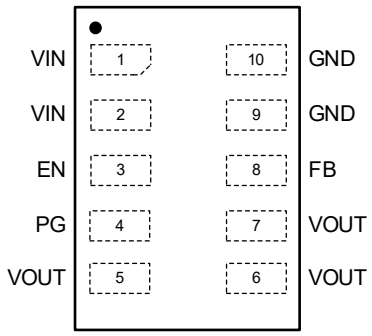
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



EMSIP-2×2.5-10L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1, 2	VIN	P	Input Voltage Pin.
3	EN	I	Active High Enable Input. Logic high sets the device active. Logic low disables it and turns it into shutdown mode. Do not leave this pin floating.
4	PG	O	Power Good Open-Drain Output. If the output voltage is less than the regulation limit, this pin is pulled low. Leave this pin floating when not in use.
5, 6, 7	VOUT	O	Output Voltage Pin.
8	FB	I	Feedback Input. An external feedback divider is needed for setting the output voltage.
9, 10	GND	G	Ground Pin.

NOTE: I = input, O = output, I/O = input/output, P = power, G = ground.

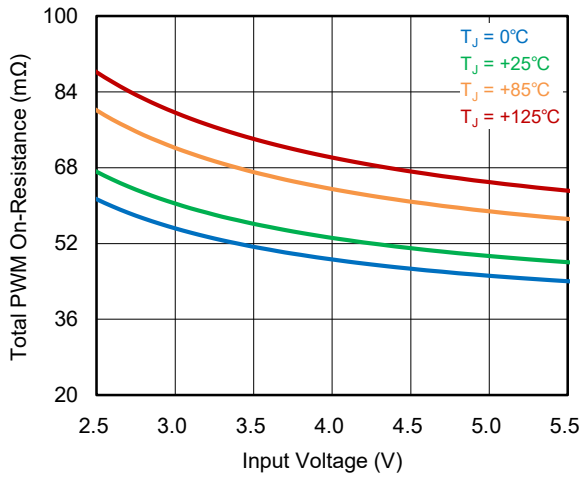
ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃ and V_{IN} = 2.4V to 5.5V. Typical values are measured at T_J = +25℃ and V_{IN} = 5V, unless otherwise noted.)

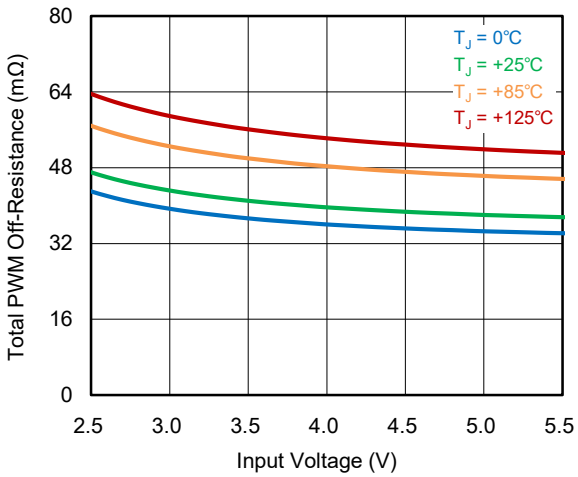
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply							
Device Input Current	I_Q	EN = high, no load, device not switching,	SGMM2042A		5.7	12	μA
			SGMM2042B		400	500	
Shutdown Current	I_{SD}	EN = low, T_J = -40℃ to +85℃			0.05	2	μA
		EN = low, T_J = -40℃ to +125℃				12	
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} falling		2.1	2.2	2.3	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}	V_{IN} rising			160		mV
Thermal Shutdown Threshold	T_{SD}	T_J rising			150		℃
Thermal Shutdown Hysteresis	T_{HYS}	T_J falling			18		℃
Logic Interface EN							
High-Level Threshold Voltage	V_{IH}			1.02			V
Low-Level Threshold Voltage	V_{IL}					0.35	
Input Leakage Current into EN Pin	I_{EN_LKG}	EN = high			0.01	0.1	μA
Soft-Start, Power Good							
Soft-Start Time	t_{SS}	Time from EN high to 95% of V_{OUT} nominal			1.4		ms
Power Good Lower Threshold	V_{PG}	V_{FB} referenced to V_{FB} nominal	V_{PG} rising	94	96	98.5	%
			V_{PG} falling	89	92	94	
Power Good Upper Threshold			V_{PG} rising	102	105	107	
			V_{PG} falling	107	110	112	
Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA				0.4	V
Input Leakage Current into PG Pin	I_{PG_LKG}	V_{PG} = 5.0V			0.01	0.15	μA
Power Good Deglitch Delay	t_{PG_DLY}	PG rising edge			100		μs
		PG falling edge			18		
Output							
Feedback Regulation Voltage	V_{FB}	PWM mode	V_{IN} = 5V, T_J = +25℃	594	600	606	mV
				588		612	
Feedback Input Leakage Current	I_{FB_LKG}	V_{FB} = 0.6V			0.01	0.05	μA
Output Discharge Current	I_{DIS}	V_{SW} = 0.4V, EN = low		33	77		mA
Inductor	L	At 500kHz			450		nH
Power Switch							
Total PWM-On Resistance	R_{PWM_ON}	PWM on, resistance from VIN to VOUT			50	105	mΩ
Total PWM-Off Resistance	R_{PWM_OFF}	PWM off, resistance from VOUT to GND			40	75	
High-side FET Switch Current Limit, DC	I_{LM}			4.4	6.1	7.4	A
Low-side FET Current Limit, DC				4.2	5.5	7.1	
Low-side FET Negative Current Limit, DC					-1.6		
Frequency		I_{OUT} = 1A, V_{OUT} = 1.8V			2.2		MHz

TYPICAL PERFORMANCE CHARACTERISTICS

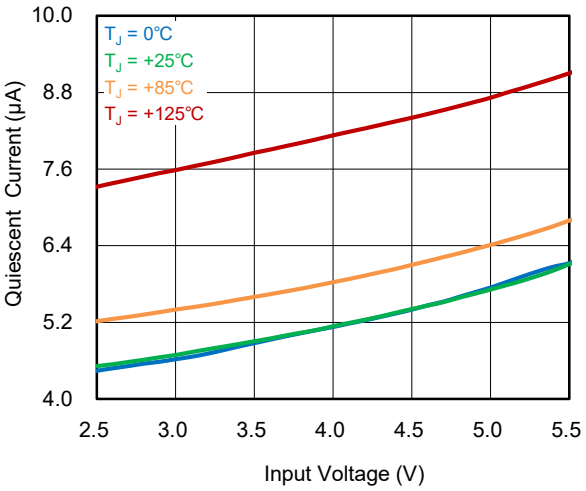
Total PWM-On Resistance vs. Input Voltage



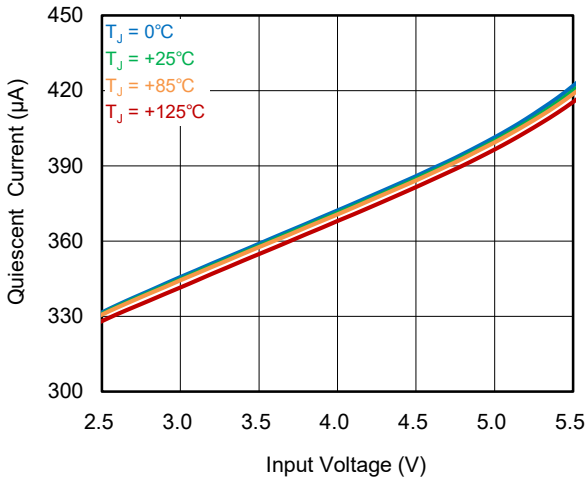
Total PWM-Off Resistance vs. Input Voltage



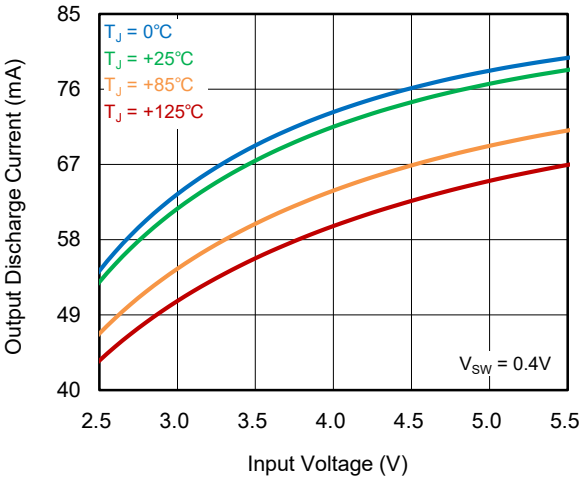
Quiescent Current vs. Input Voltage (SGMM2042A)



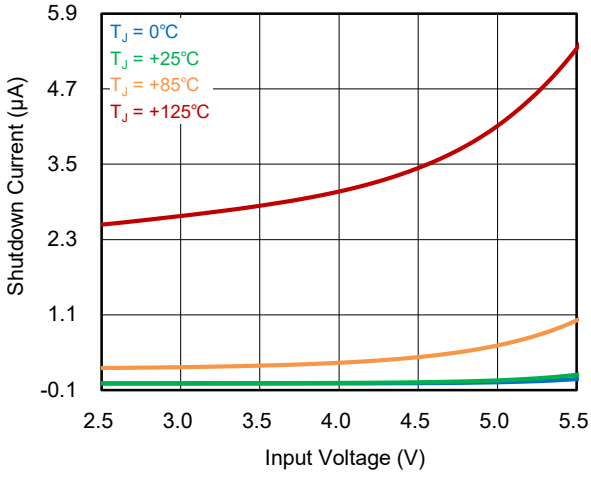
Quiescent Current vs. Input Voltage (SGMM2042B)



Output Discharge Current vs. Input Voltage



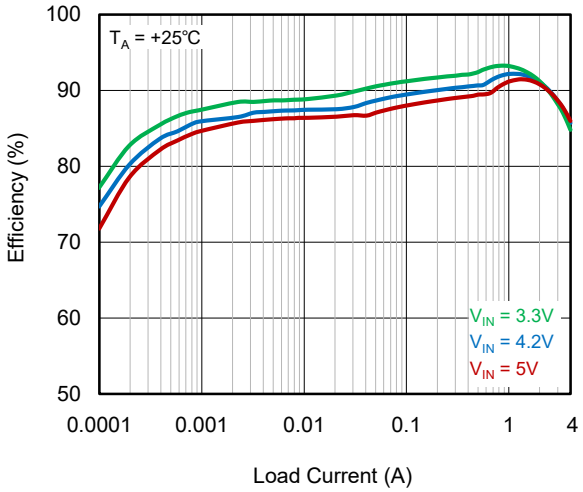
Shutdown Current vs. Input Voltage



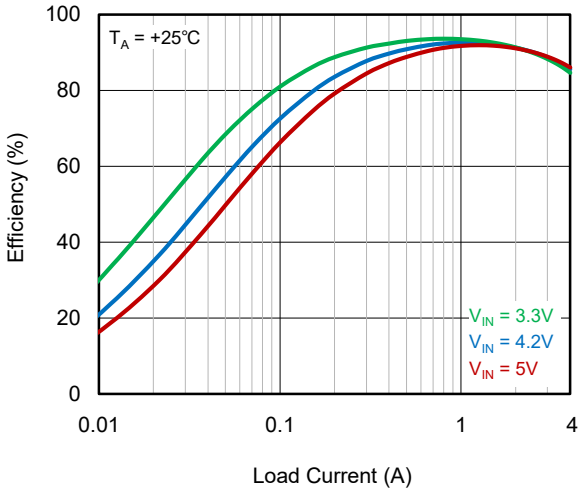
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.3V, V_{OUT} = 1.8V, and C_{OUT} = 2 × 22μF, unless otherwise noted.

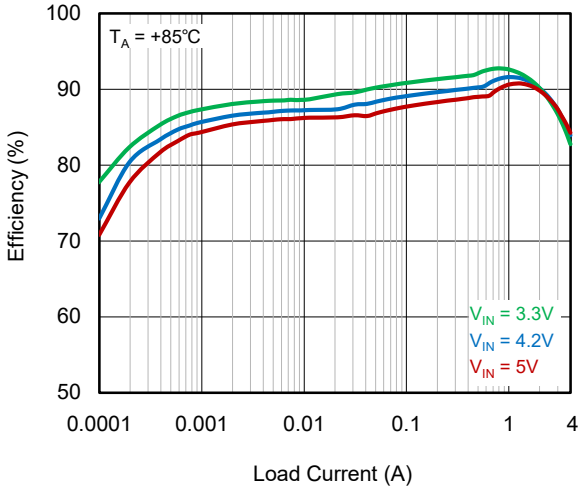
Efficiency vs. Load Current (SGMM2042A)



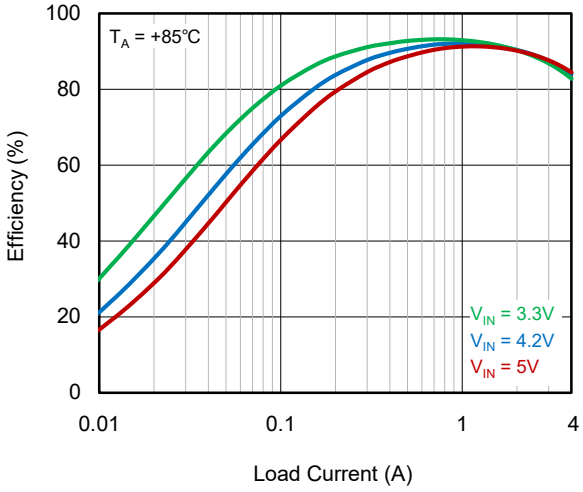
Efficiency vs. Load Current (SGMM2042B)



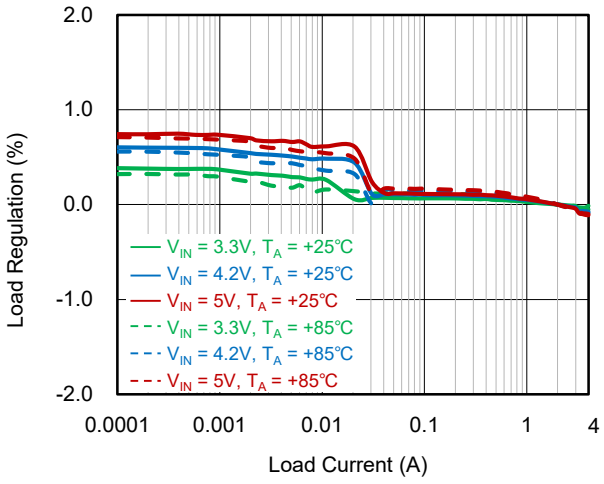
Efficiency vs. Load Current (SGMM2042A)



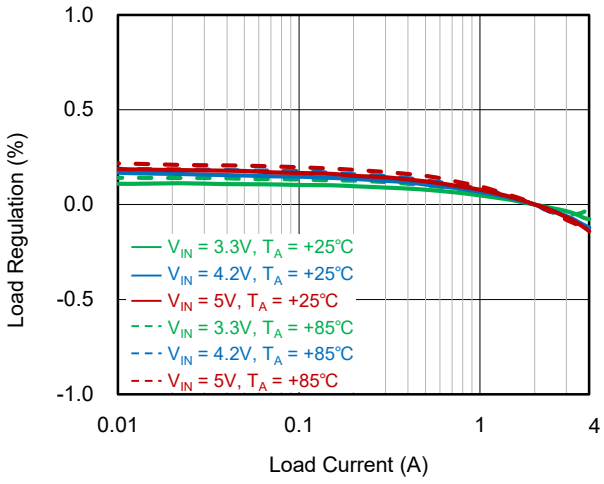
Efficiency vs. Load Current (SGMM2042B)



Load Regulation (SGMM2042A)



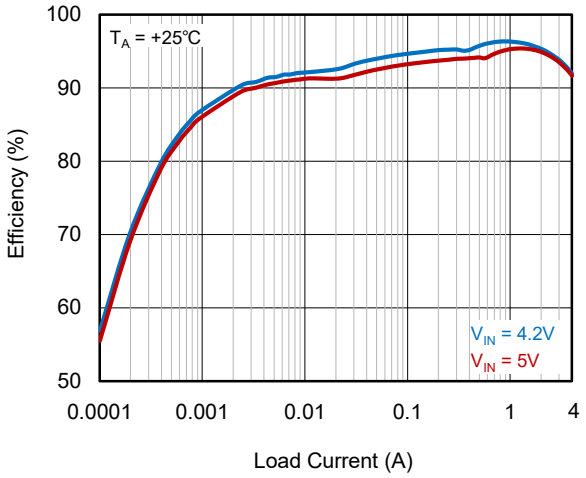
Load Regulation (SGMM2042B)



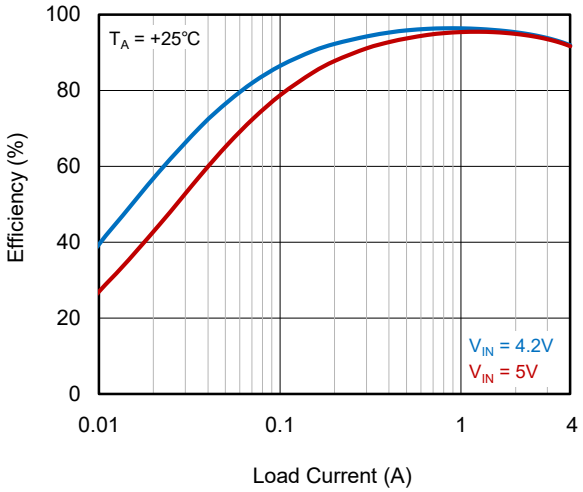
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5.0V, V_{OUT} = 3.3V, and C_{OUT} = 2 × 22μF, unless otherwise noted.

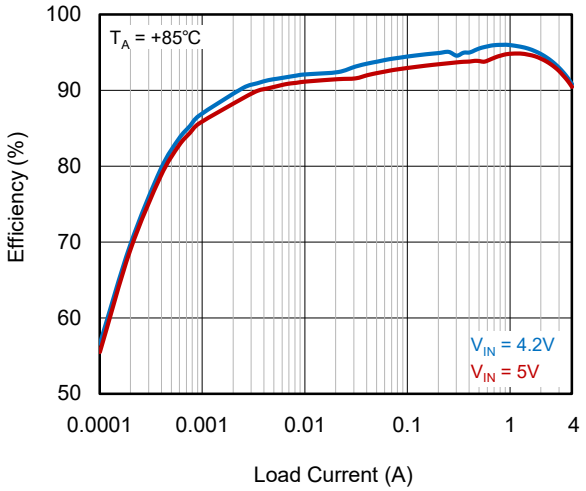
Efficiency vs. Load Current (SGMM2042A)



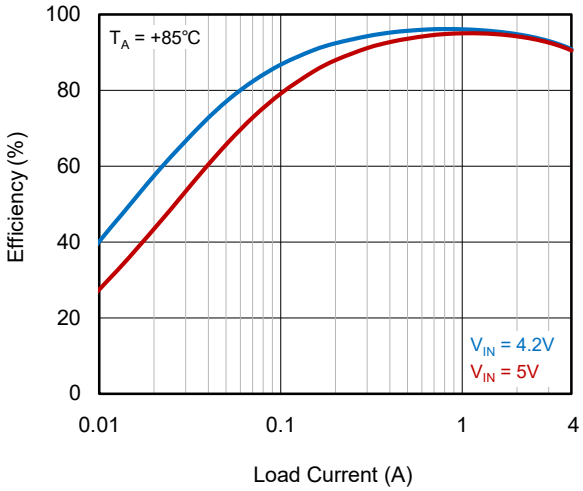
Efficiency vs. Load Current (SGMM2042B)



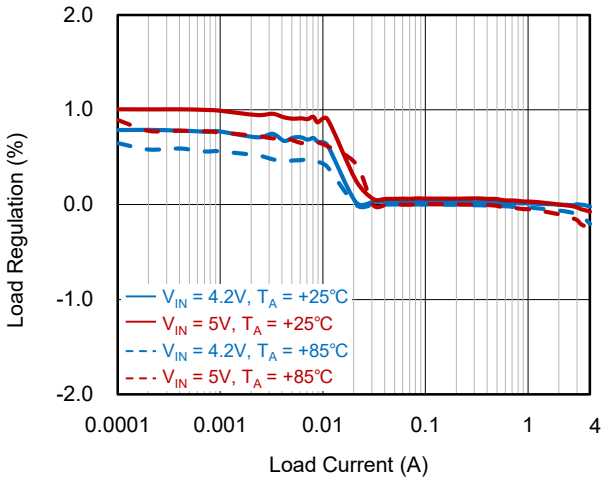
Efficiency vs. Load Current (SGMM2042A)



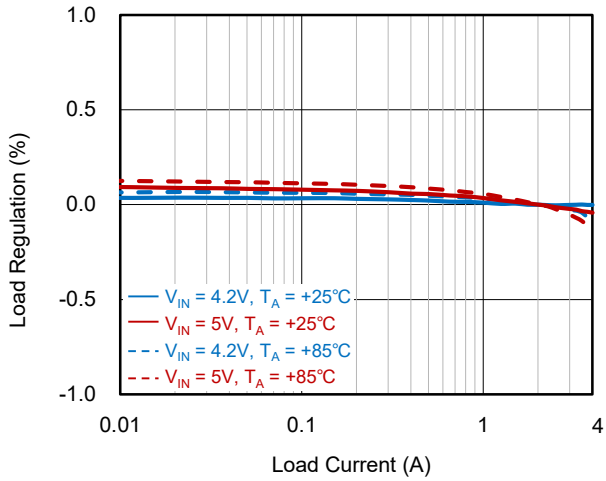
Efficiency vs. Load Current (SGMM2042B)



Load Regulation (SGMM2042A)



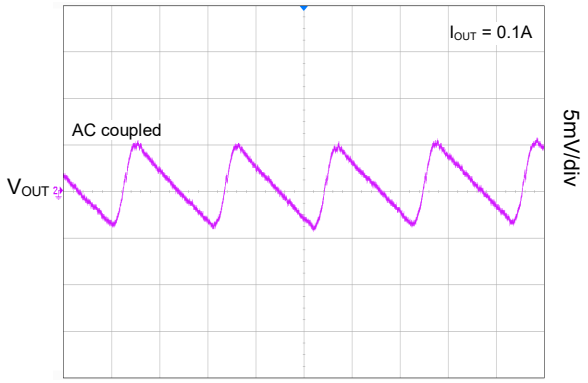
Load Regulation (SGMM2042B)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

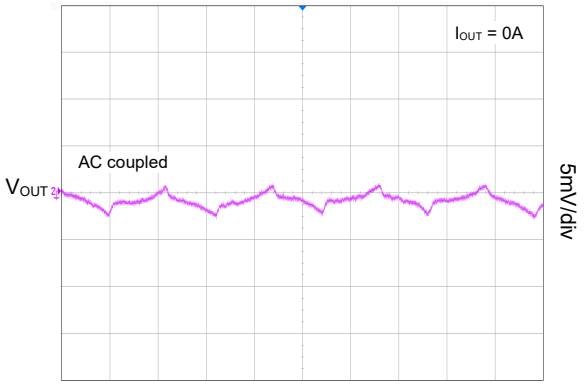
V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{IN} = 4.7μF, C_{OUT} = 2 × 22μF, and T_A = +25℃, unless otherwise noted.

Output Ripple (SGMM2042A)



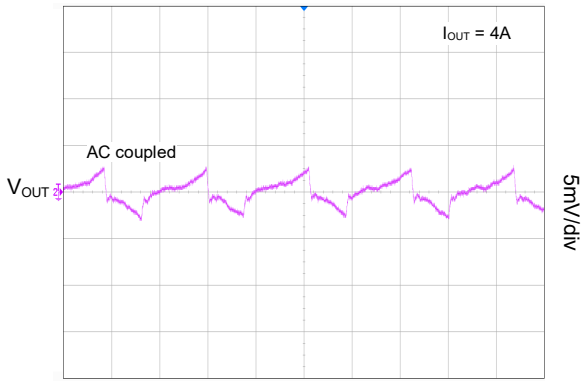
Time (1μs/div)

Output Ripple (SGMM2042B)



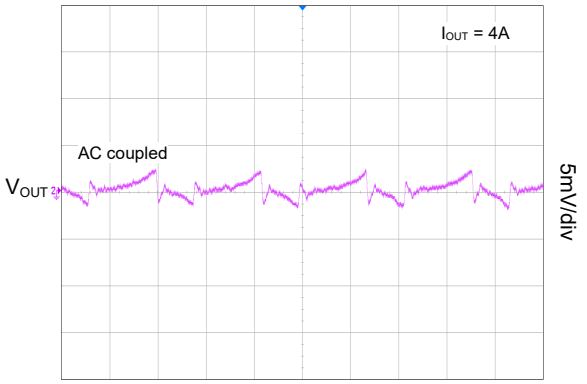
Time (200ns/div)

Output Ripple (SGMM2042A)



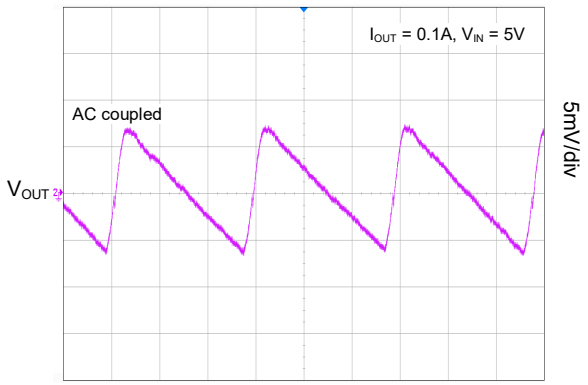
Time (200ns/div)

Output Ripple (SGMM2042B)



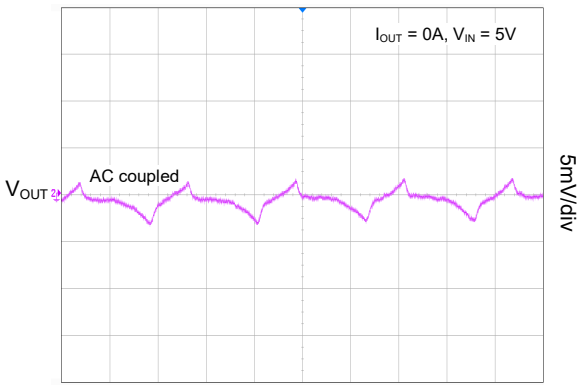
Time (200ns/div)

Output Ripple (SGMM2042A)



Time (1μs/div)

Output Ripple (SGMM2042B)

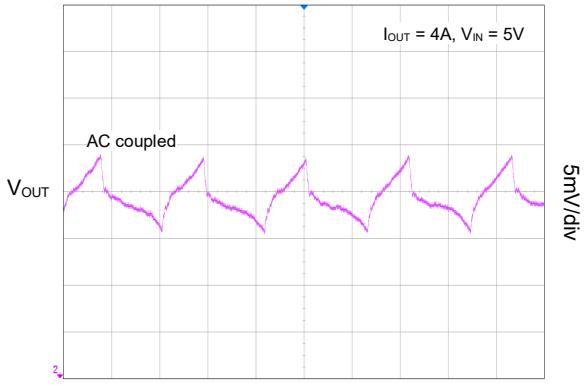


Time (200ns/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

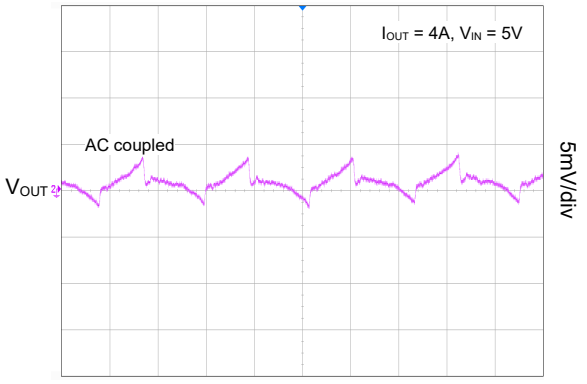
V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{IN} = 4.7μF, C_{OUT} = 2 × 22μF, and T_A = +25℃, unless otherwise noted.

Output Ripple (SGMM2042A)



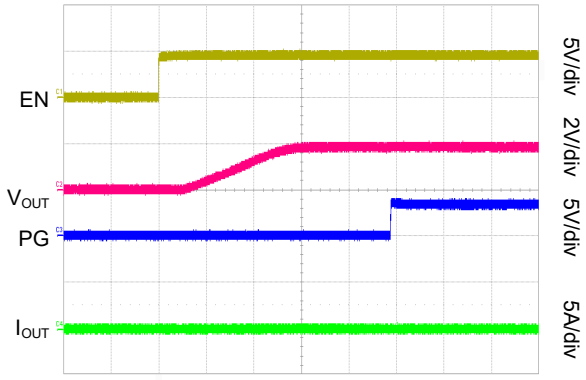
Time (200ns/div)

Output Ripple (SGMM2042B)



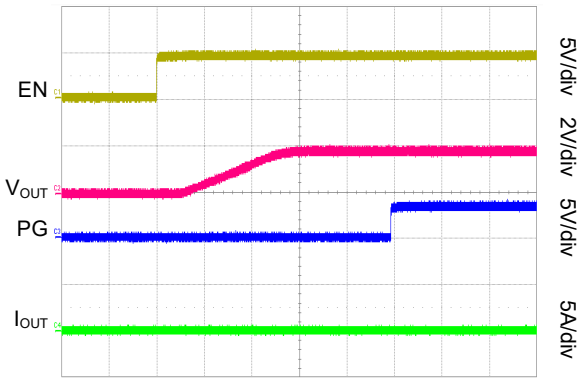
Time (200ns/div)

Startup without Load (SGMM2042A)



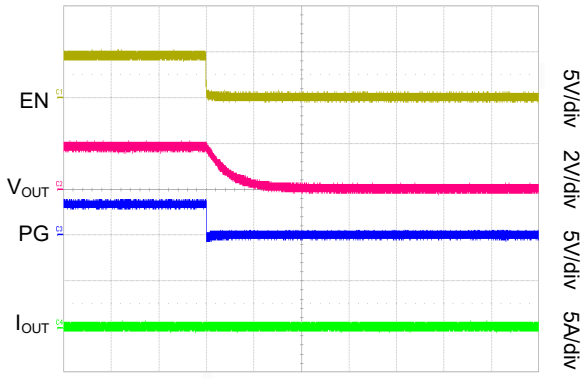
Time (500μs/div)

Startup without Load (SGMM2042B)



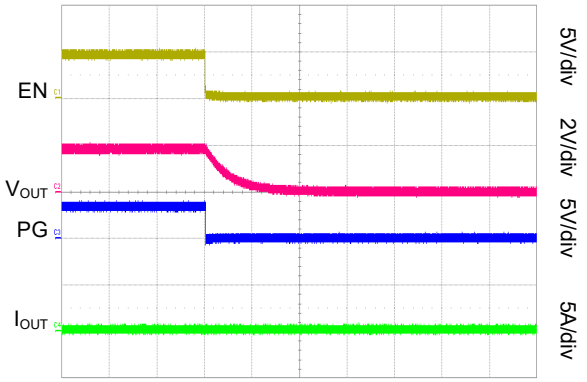
Time (500μs/div)

Shutdown without Load (SGMM2042A)



Time (500μs/div)

Shutdown without Load (SGMM2042B)

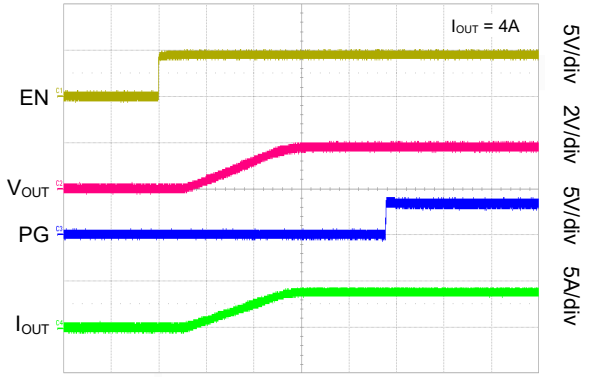


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

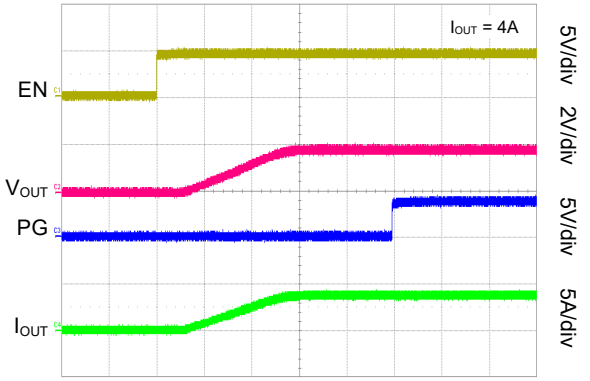
V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{IN} = 4.7μF, C_{OUT} = 2 × 22μF, and T_A = +25℃, unless otherwise noted.

Startup with Load (SGMM2042A)



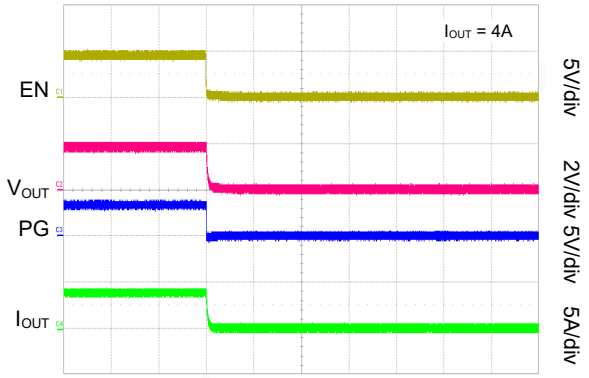
Time (500μs/div)

Startup with Load (SGMM2042B)



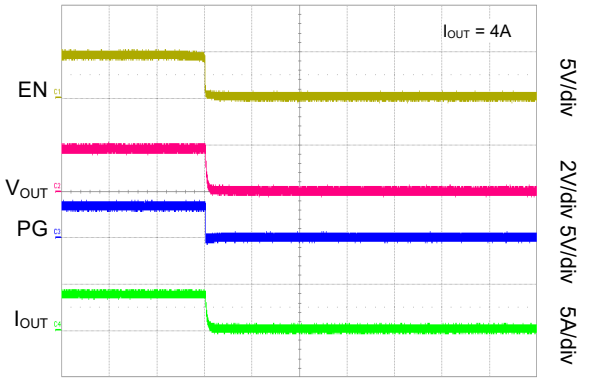
Time (500μs/div)

Shutdown with Load (SGMM2042A)



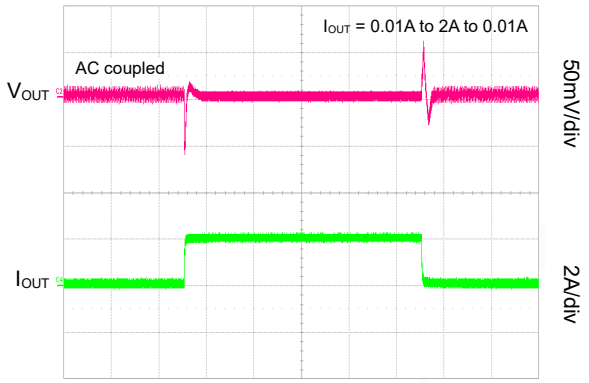
Time (500μs/div)

Shutdown with Load (SGMM2042B)



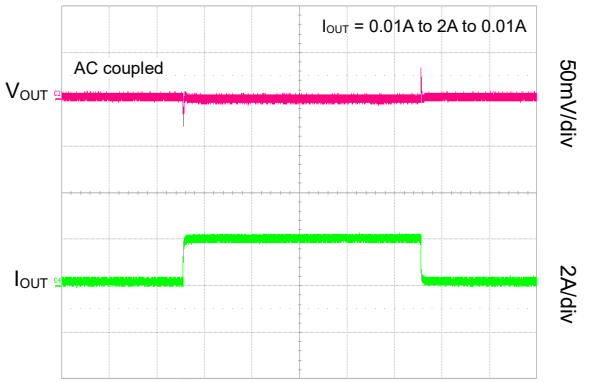
Time (500μs/div)

Load Transient (SGMM2042A)



Time (200μs/div)

Load Transient (SGMM2042B)

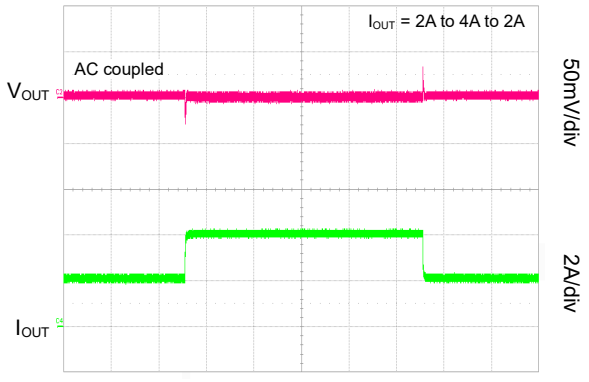


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

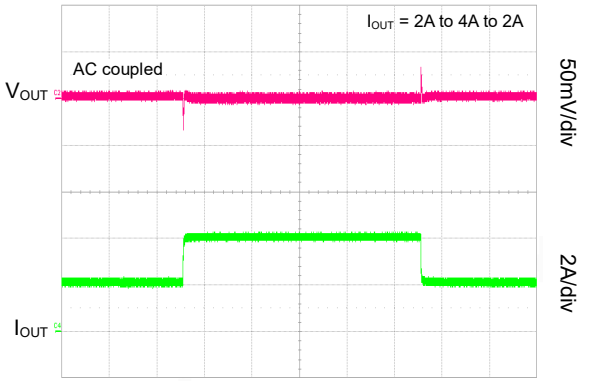
V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{IN} = 4.7μF, C_{OUT} = 2 × 22μF, and T_A = +25℃, unless otherwise noted.

Load Transient (SGMM2042A)



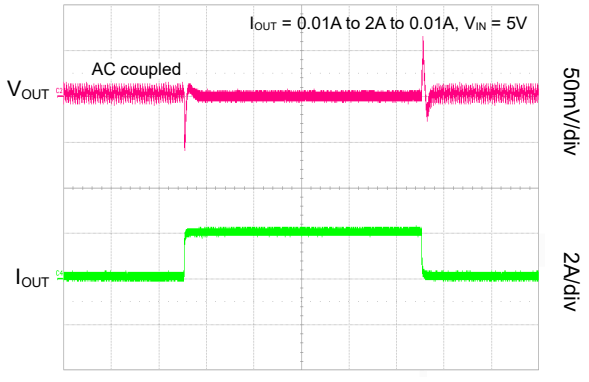
Time (200μs/div)

Load Transient (SGMM2042B)



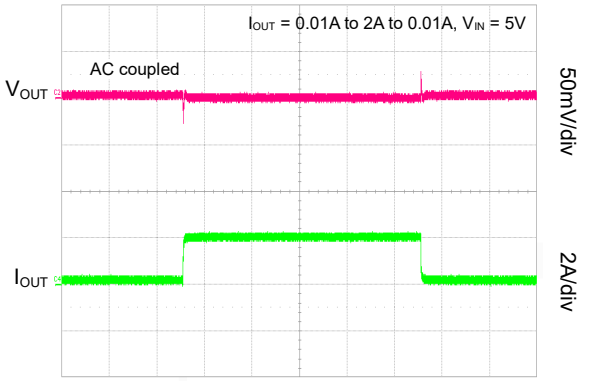
Time (200μs/div)

Load Transient (SGMM2042A)



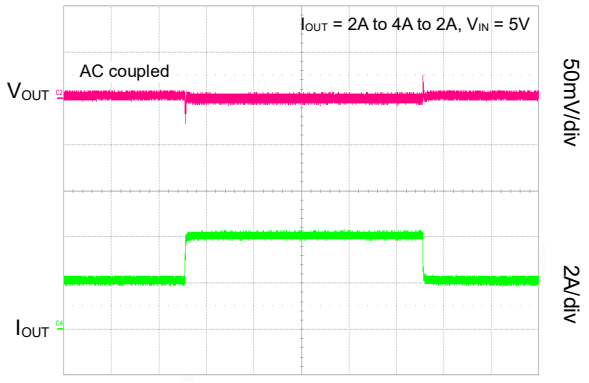
Time (200μs/div)

Load Transient (SGMM2042B)



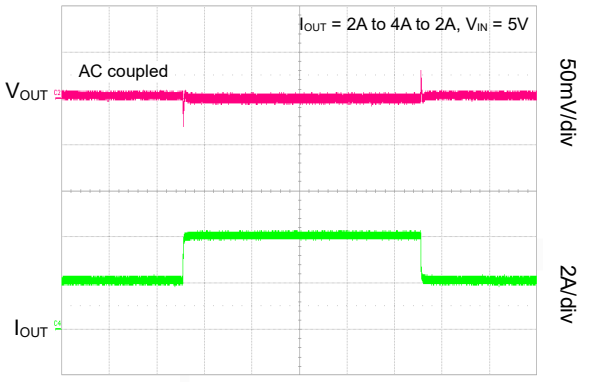
Time (200μs/div)

Load Transient (SGMM2042A)



Time (200μs/div)

Load Transient (SGMM2042B)

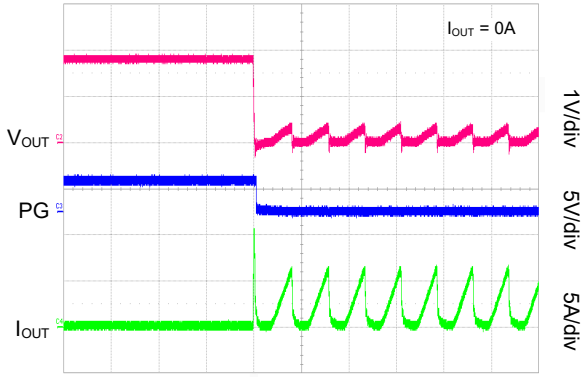


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

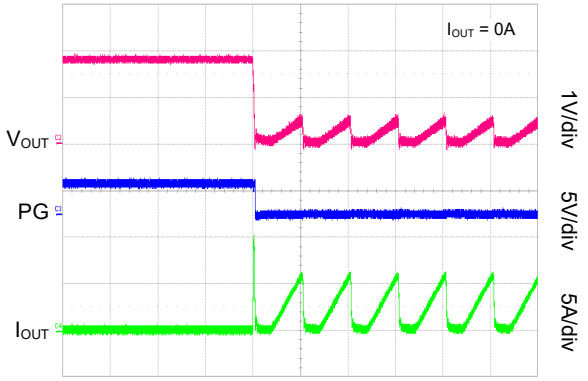
V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{IN} = 4.7μF, C_{OUT} = 2 × 22μF, and T_A = +25℃, unless otherwise noted.

Short-Circuit, Entry (SGMM2042A)



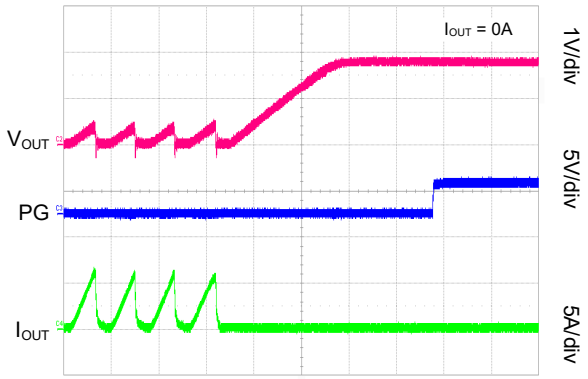
Time (500μs/div)

Short-Circuit, Entry (SGMM2042B)



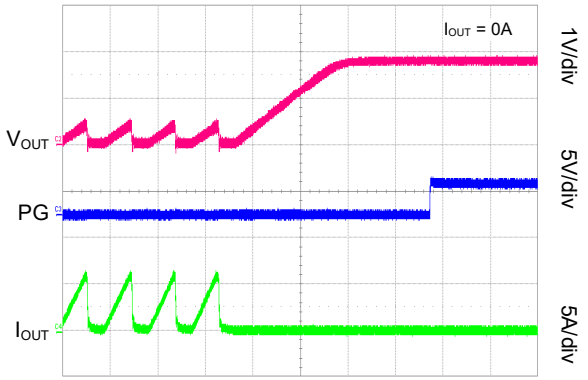
Time (500μs/div)

Short-Circuit, Recovery (SGMM2042A)



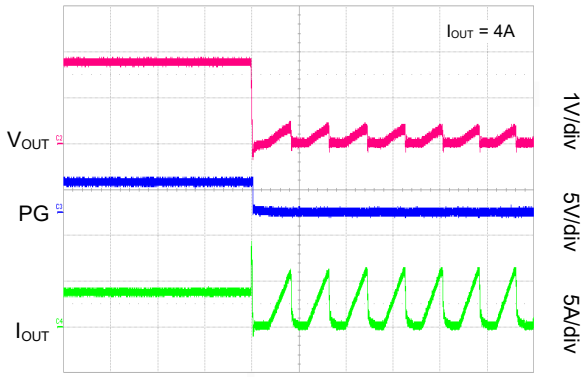
Time (500μs/div)

Short-Circuit, Recovery (SGMM2042B)



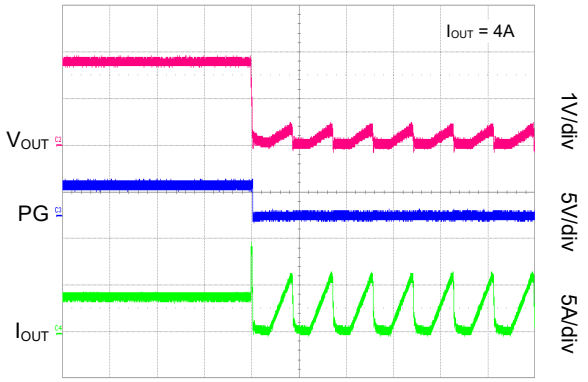
Time (500μs/div)

Short-Circuit, Entry (SGMM2042A)



Time (500μs/div)

Short-Circuit, Entry (SGMM2042B)

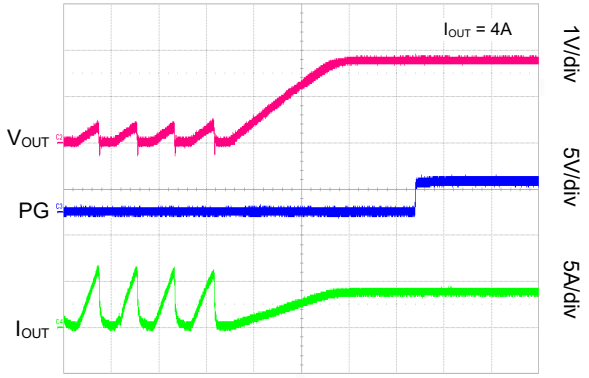


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

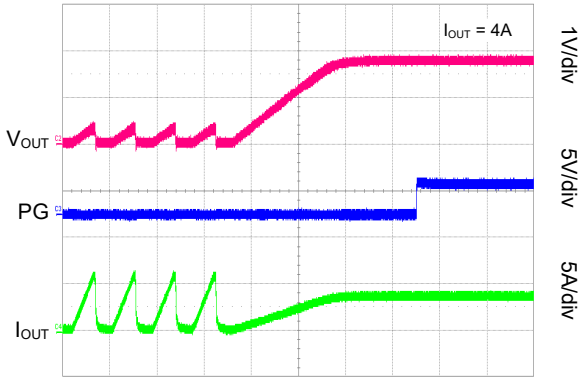
V_{IN} = 3.3V, V_{OUT} = 1.8V, C_{IN} = 4.7μF, C_{OUT} = 2 × 22μF, and T_A = +25℃, unless otherwise noted.

Short-Circuit, Recovery (SGMM2042A)



Time (500μs/div)

Short-Circuit, Recovery (SGMM2042B)



Time (500μs/div)

FUNCTIONAL BLOCK DIAGRAM

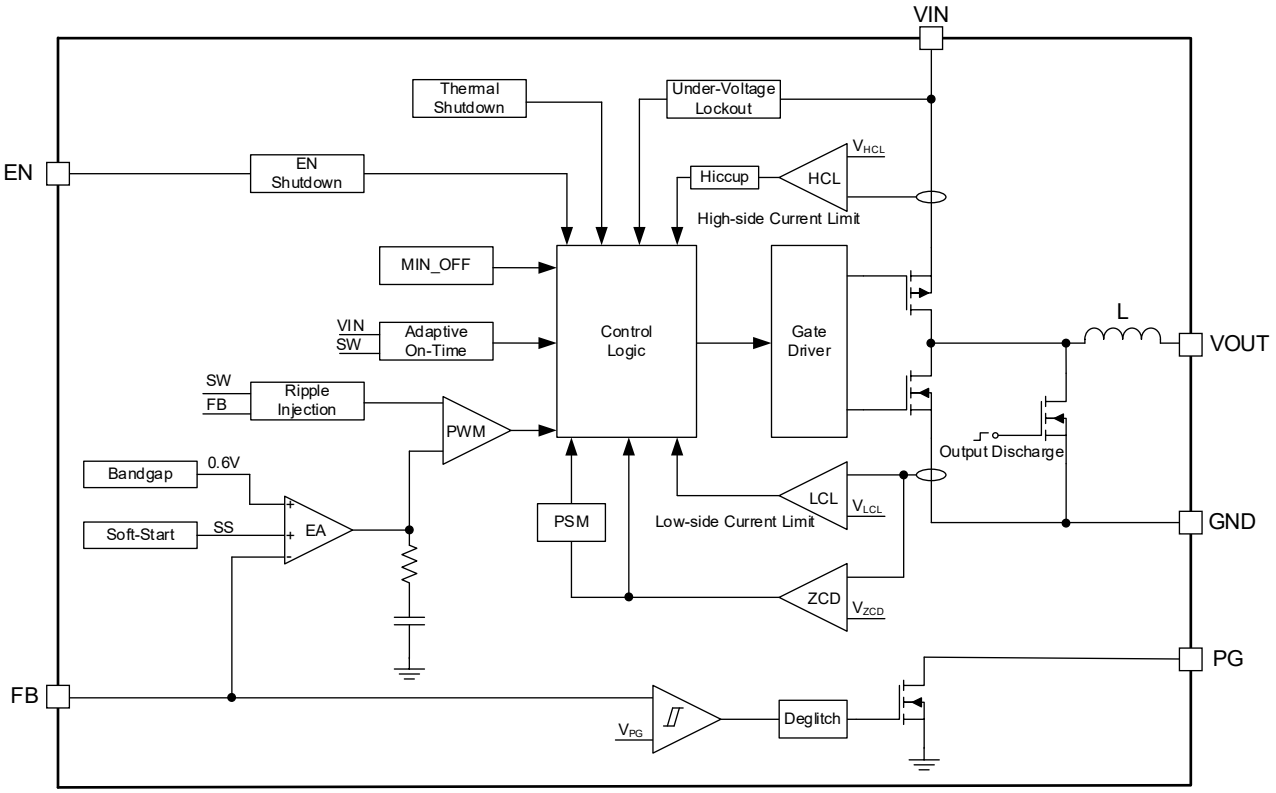


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

SGMM2042 is a high frequency synchronous Buck PowerSoC with AHP-COT architecture and advanced regulation topology.

For SGMM2042A, the device works in pulse width modulation (PWM) mode at medium to heavy loads. When the load current falls, it transitions seamlessly from PWM mode to pulse frequency modulation (PFM) once the inductor current becomes discontinuous. At lighter load conditions, it shifts to the power-save mode (PSM) to minimize the losses. It also shuts down most of the internal circuits in power-save mode. In this mode, one or few PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume. If the load is still low, the output will go slightly higher than normal value again and the switches will be turned off. In power-save mode, the output voltage is slightly higher than nominal output voltage.

For SGMM2042B, the device works in force PWM mode at full load range. In PWM mode, the device works with a nominal switching frequency of 2.2MHz.

Under-Voltage Lockout (UVLO)

The device implements the under-voltage lockout (UVLO) with a 160mV hysteresis. When the input voltage falls below the V_{UVLO}, it shuts down the device.

Device Enable and the Output Discharge FET

When the input voltage is valid, pulling the EN input to logic high to enable the device and pulling it low to shut it down. In the shutdown mode, the switches and all control circuits are turned off to reduce the device current to 0.05μA. During shutdown, an internal FET is turned on and connects the SW pin to the GND for smooth discharge of the output.

Soft-Start and Pre-biased Output

When EN is set to logic high and after internal delay, the device starts switching and V_{OUT} increases with 1.4ms internal soft-start circuit. The soft-start is critical to prevent excessive inrush currents and to avoid triggering of the output over-current protection to provide a smooth output rise. It also prevents extreme input voltage drops due to large inrush current over the high-impedance batteries and input sources that can interrupt the power-up. The device is also capable of starting with a pre-biased output capacitor when it is powered up or enabled. When the device is turned on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off period and the device must restart under pre-biased output condition. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value. Without the pre-biased capability, the device may not be able to start up properly.

Power Good (PG)

There is the PG function inside the device. PG is an open-drain output with 1mA sinking capability. This pin should be pulled up with an external resistor to a logic high rail which is no more than 5.5V unless it is not used. The PG signal is in high-impedance state when the output voltage is in regulation range. Table 1 shows how the PG state is changed in different conditions. PG remains low until V_{OUT} comes up to 96% to 105% of its nominal (set) value. PG function has hysteresis effect. When PG is high, it will go low if V_{OUT} changes down to 92% or up to 110% of its nominal (set) value. When the device is disabled, under-voltage lockout or in thermal shutdown, the PG pin is driven to low.

The PG output is useful for power supply sequencing as well. Usually, the multiple power rails of a system need to be powered in a specific sequence for proper startup. The PG output of the leading power supply is connected to the EN input of the subsequent power supply to implement such sequencing. If not used, the PG pin needs to keep floating. The PG signal has a rise delay of 100μs and a fall delay of 18μs.

Table 1. PG Output State in Different Conditions

Reason	Condition(s)	PG State	
		High-Z	Low
Enable (EN = High)	$V_{FB} \geq 0.576V$	√	
	$V_{FB} \leq 0.552V$		√
	$V_{FB} \leq 0.63V$	√	
	$V_{FB} \geq 0.66V$		√
Shutdown by EN	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$1.4V < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 1.4V$	Uncertain	

DETAILED DESCRIPTION (continued)

Pulse Width Modulation (PWM) Operation

In the condition of continuous conduction mode (CCM), which occurs at medium to heavy load or the force PWM mode, the device works in pulse width modulation (PWM) operation. The switching frequency is slightly affected by VIN, VOUT and load condition. Then a fixed on-time architecture is activated and for SGMM2042B, the typical on-time is t_{ON} = 455ns × (V_{OUT}/V_{IN}). For SGMM2042A, it automatically exits PWM mode when the inductor current is discontinuous.

Power-Save Mode (PSM) at Light Loads: SGMM2042A

Once the load current decreases, the SGMM2042A will enter power-save mode. Then, the device has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency. In power-save mode, the inductor current is discontinuous and the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

Minimum Duty Cycle and 100% Duty Cycle

Due to the reduction of the switching frequency for regulation, the device has no minimum duty cycle set. When the input voltage gradually drops to the regulation output voltage, the device can operate at 100% duty cycle and keep the high-side MOSFET continuously on for minimal input-to-output voltage difference. The low-side MOSFET is kept off.

In this mode, the lowest input voltage for keeping the output regulated is determined by load current and the resistive drops from the input to the output as given in Equation 1:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times R_{PWM\_ON} \quad (1)$$

where:

V_{IN_MIN} is the minimum input voltage to maintain output voltage in regulation.

I_{OUT_MAX} is the maximum output current.

R_{PWM_ON} is PWM on, Resistance from VIN to VOUT

Switch Current Limits and Short-Circuit Protection (Hiccup)

Limiting the switch current protects the switch itself and prevents over-current of the source and the inductor. If the high-side (HS) switch current exceeds the ILIM threshold, HS switch is turned off and the low-side (LS) switch is turned on to reduce the inductor current and limit the peak current. If 32 cycles consecutive repetition of this event occur, the device stops switching. A new startup is initiated automatically (hiccup) after 200μs. The hiccup repeats until the overload or short-circuit fault is cleared. LS switch current limit is also integrated in the device. Each cycle, the HS switch is not allowed to turn on until the LS current is below the low-side FET current limit.

Thermal Shutdown

Thermal protection is included to protect the die against overheating damage. If the junction temperature exceeds T_{SD} threshold, the switching is stopped and the device is shut down. An automatic recovery with a soft-start begins when the junction cools down for 18℃ below the T_{SD} limit.

APPLICATION INFORMATION

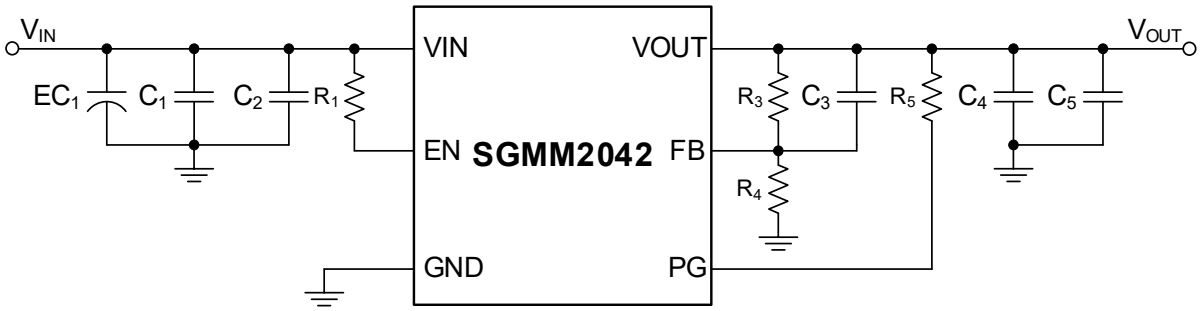


Figure 3. Application Circuit

Table 2. Selected Components for the Design Example

Output Voltage (V)	Part	Value	Package
1.8	C_1	Optional	
	EC_1	Optional	
	C_2	4.7μF, 10V, X5R, 10% GRM188Z71A475KE15D	0603
	C_3	10pF, 50V, C0G, 5% GRM1885C1H100JA01D	0603
	C_4, C_5	22μF,10V, X5R, 20% GRM188R61A226ME15D	0603
	R_1, R_4, R_5	100kΩ, 0.1W, ±1%	0603
	R_3	200kΩ, 0.1W, ±1%	0603

Output Voltage Adjustment

Use Equation 1 for selecting the feedback resistors (R_3 and R_4) in Figure 3 to set the desired output voltage. First choose R_4 value below 100kΩ to avoid high noise sensitivity on the FB pin. Do not choose a very small value for R_4 otherwise the loss will be increased on this resistor that reduces the light load efficiency.

$$R_3 = R_4 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R_4 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (1)$$

A feed-forward capacitor improves transient response to the load steps and reduces the output ripple in PSM.

Output Capacitor Selection

For output capacitor design, output ripple, transient response and loop stability should be considered. Choosing ceramic capacitor with X5R or better dielectric is very important for temperature characteristics. Bias voltage can cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value. For this example, the output capacitance is recommended to use 2 × 22μF.

Thermal Considerations

Especial care must be taken for power dissipation and thermal relief in high power density designs. The SGMM2042 is a low-profile and fine-pitch surface-mount package that is typically used in a small area or volume. Thermal coupling, airflow and heat sinking must be considered in the system level and the space between heat generating elements must be managed properly.

To enhance the thermal performance, the PCB itself has a significant role and to help transfer the heat away by using large copper traces/planes that are connected to the device pins (and thermal pads if present). Considering a proper airflow in the system can complete the thermal relief for reliable operation of the power supply.

LAYOUT GUIDELINES

A critical component of a high frequency switching power supply is the PCB layout. A good layout can improve the overall performance of the system and a poor layout can result in stability issues and EMI problems. The following guidelines are provided for designing a power supply layout with the SGMM2042.

• Place the input/output capacitors as close as possible to the IC pins and keep the power traces short. Use direct and wide traces for routing power paths to assure low trace parasitic resistance and inductance.

• Connect the ground returns of the input and output capacitors close to the GND pin and at the same point to avoid a ground potential shift and to minimize high frequency current path.

• Keep the output voltage sense trace and FB pin connections away from the high frequency and noisy power traces to avoid magnetic and electric noise coupling.

• Use GND planes in mid-layers for shielding and minimizing the ground potential drifts.

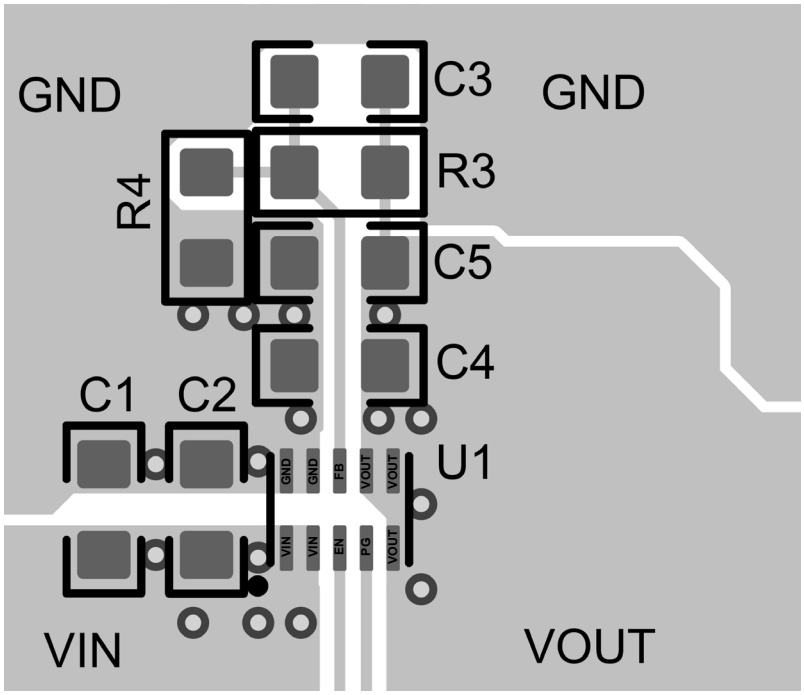


Figure 4. PCB Example-Top Layer

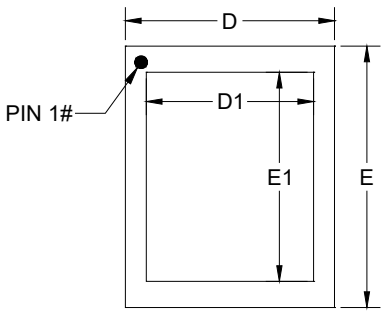
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

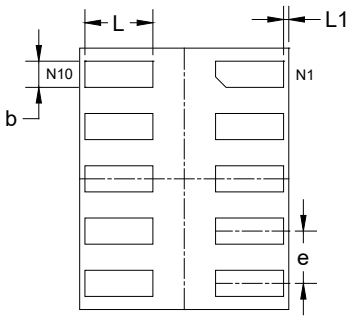
Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

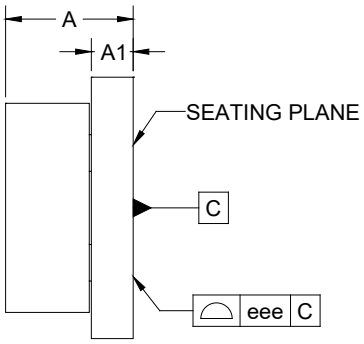
EMSIP-2×2.5-10L



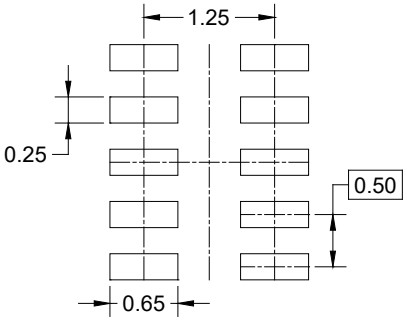
TOP VIEW



BOTTOM VIEW



SIDE VIEW



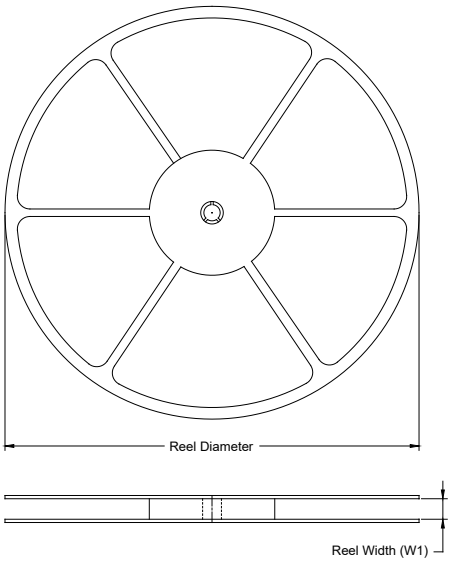
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.270
A1		0.400 REF	
b	0.200	-	0.300
D	1.900	-	2.100
D1		1.600 REF	
E	2.400	-	2.600
E1		2.000 REF	
e		0.500 BSC	
L	0.600	-	0.700
L1		0.050 REF	
eee		0.100	

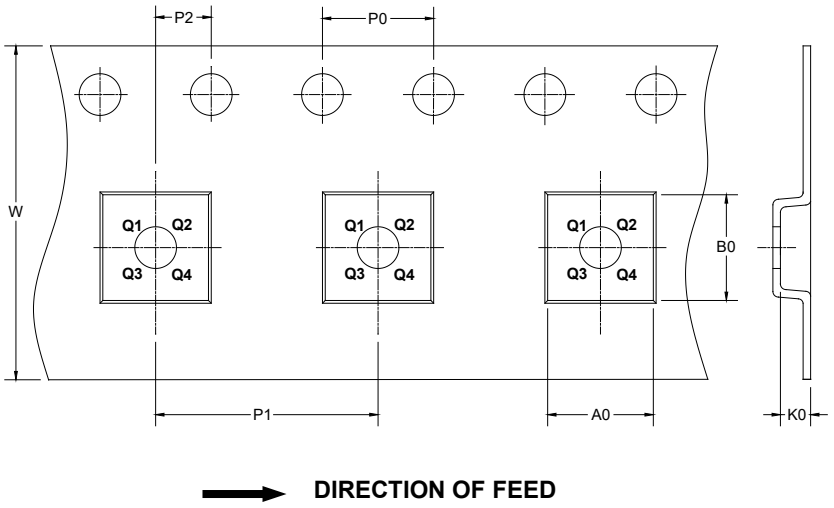
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



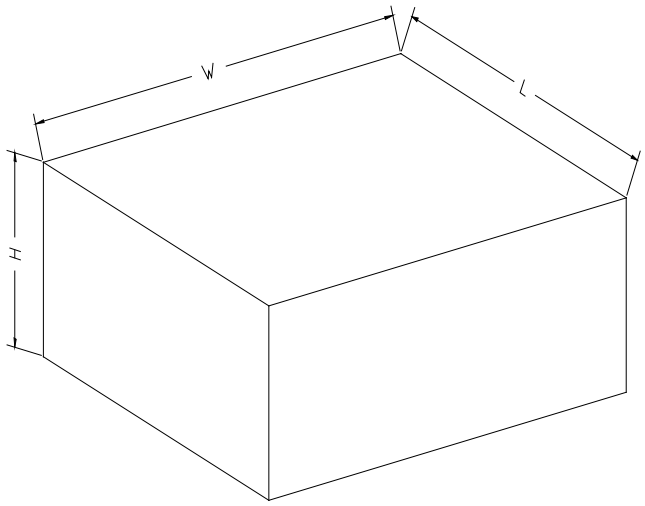
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
EMSIP-2×2.5-10L	13"	12.4	2.20	2.70	1.40	4.00	4.00	2.00	12.00	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002